Resonant Multilevel Modular Boost Inverters for Single-Phase Transformerless Photovoltaic Systems

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***Abstract*—This paper presents two novel single-phase resonant multilevel modular boost inverters based on resonant switched capacitor cells and a partial power processed voltage regulator. Compared with other multilevel boost inverters applied in PV systems, one remarkable advantage of the proposed topologies is that the bulky AC filtering inductor is replaced by a smaller-size one in the partial power processed buck converter. Constant duty cycle PWM method is attractive for the multilevel inverter controller design. GaN Enhancement Mode Power Transistors help both the modular resonant switched capacitor cells and the full-bridge unfolder be realized in a small size with high power density. The clamp capacitors in the resonant switched capacitor cells effectively alleviate the switch voltage spikes. These two inverter topologies are analyzed and simulated in PLECS. Simulation results verify the validity of boost inverter function. Stress analysis shows that the inverter has relatively small total normalized switch conduction power stress and total normalized switch stress ratio. Relative total semiconductor chip area comparison results reflect that the proposed topology achieves more efficient semiconductor utilization compared with typical non-resonant multilevel modular switched capacitor boost inverters. Test results indicate that the proposed topology can be used for single-phase non-isolated PV boost inverter applications with small ground leakage current, high voltage conversion ratio, small volume and potential high efficiency.**

Keywords—resonant switched capacitor, partial power processing, multilevel inverter, boost inverter, PV inverter, GaN FET, ZCS, single-phase transformerless photovoltaic system

I. INTRODUCTION

In low-power low-voltage grid-connected applications, since no mandatory isolation is required in most countries [1], transformerless Photovoltaic (PV) inverters are preferred due to higher efficiency, lower cost and smaller volume [1]–[3] compared with isolated topologies. However, in this type of structures, when the PV panel frame grounding is necessary, inherent parasitic capacitance exists between the PV panels and ground [4]. Due to the inverter high-frequency switching, the common-mode potential difference is formed on this parasitic capacitance [5][6]. As a result, the capacitive leakage ground current is injected into the circuit and causes electromagnetic inference, unexpected power loss and output power quality deterioration [7]. To solve this challenge, dc-link capacitor midpoint can be connected to the neutral point of load [8]. Another common alternative is to disconnect the PV panel and the load by using bidirectional switches on the inverter dc side [9] or ac side [6][10].

Another challenge in single-phase transformerless PV inverters is to find a high-efficiency, compact-size topology with high voltage conversion ratio and easily-realizable control. Multilevel inverters are prospective candidates due to lower output voltage and input current distortion [11][12], smaller volume [12] and more balanced voltage sharing among active switches [12][13] compared with two-level inverters. These days, switched capacitor multilevel converters and inverters have been well researched due to the modular structure, possible ZCS [14][15] and ZVS [16] soft switching, high voltage conversion ratio [17], high power density [18]–[20] and high efficiency [21]. A modular DC/DC switched capacitor boost converter cascaded with a full-bridge unfolder is proposed in [22]. But big electrolyte capacitors, MOSFETs, diodes and output filtering inductor worsen both the overall efficiency and power density. A flying-capacitor-clamped five-level inverter is analyzed in [23]. However, the flying capacitor and output filtering inductor are bulky. The capacitor voltage balancing method increases the control complexity. Basically, these topologies tend to use large AC-side inductors to make the staircase waveform closer to sinusoidal. The semiconductor chip die sizes are also relatively big. Therefore, both the power density and chip die utilization are not optimized.

More challenges exist for the single-phase PV inverters such as the widely studied power decoupling methods [24]–[29] and the reliability related lifetime prediction [30]. But they will not be addressed here. In this paper, two new resonant multilevel modular boost inverters based on a resonant switched capacitor topology are proposed. Different from unipolar SPWM in [31], a constant duty cycle control in the switched capacitor converter switches is applied without using extreme values of duty cycle. The voltage stress of all the switches in the resonant switched capacitor cells of the proposed inverter is equal to the input voltage. With a small clamp capacitor, the transient voltage spike of wing-side switches is alleviated. Compared with other switched capacitor inverters [22][23], zero level is not necessary in this topology because of the voltage regulation of the partial power processing circuit. Small inductance in the partial power processing circuit makes it unnecessary to use a bulky filtering inductive component on the AC output side. This is an impressive improvement when compared with other multilevel boost inverter topologies where large inductors are always essential, such as the multilevel dc-link inverter [12], the flying capacitor inverter [23], the switched capacitor inverter [31], and the differential-mode switched capacitor boost inverter [32]. By taking advantage of the resonance among the resonant inductors and resonant capacitors, soft switching can be realized and thus the switching loss is decreased, which could increase overall efficiency. This resonant multilevel modular boost inverter is especially useful in non-isolated applications with low input voltage, high input current and high voltage conversion ratio. Further through the common-mode voltage and ground

leakage current analysis, it is a promising candidate for the single-phase transformerless PV inverter applications.

Based on the proposed resonant switched capacitor cell with voltage clamping and the voltage regulator with partial power processing, the operation principle of the topology cascading a resonant switched capacitor multilevel modular boost converter with a full-bridge inverter will be analyzed in Part II. The common-mode voltage and ground leakage current analysis will be demonstrated. Based on the same resonant switched capacitor cells, another derived topology including dual differential-mode boost converters will also be discussed in Part III. The PLECS simulation results will be given to verify the validity of these two topologies in Part IV. Besides, the comparison of total normalized conduction power stress, total normalized switch stress ratio and relative total semiconductor chip area will be made. The test prototype, overall platform and some preliminary test results will be shown in Part V. Finally, the conclusion and future work will be described in Part VI.

II. Operation Principles of The Resonant Multilevel Modular Boost Inverter With An Unfolder

A generalized resonant multilevel modular boost inverter with an unfolder is shown in Fig. 1 based on the resonant switched capacitor cell with voltage clamping, as highlighted in the green shaded box. In each resonant switched capacitor cell, there are four same switching devices (Q_{bi}, Q_{bi}' – bridge-side switches, Q_{wi}, Q_{wi}' – wing-side switches), one clamp capacitor (C_{ci}), one resonant capacitor (C_{ri}) and one resonant inductor (L_{ri}). To realize the

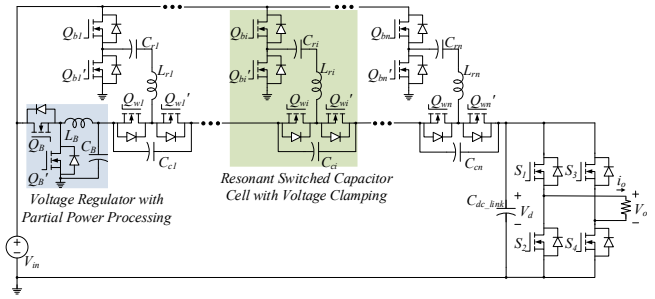


Fig. 1. Proposed resonant multilevel modular boost inverter with a full-bridge unfolder

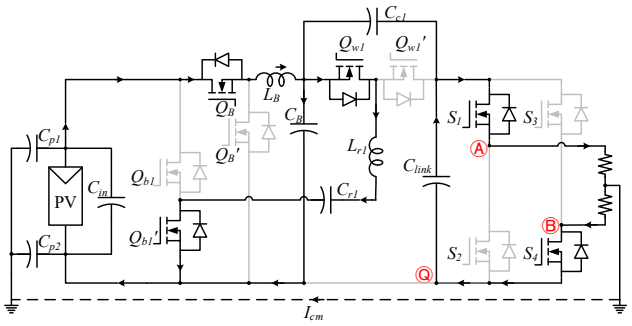
voltage regulation without full power processing, a buck converter is placed between the first cell and the input voltage source, as shown in the light blue shaded box. Q_B, Q_B' are the buck converter switches. L_B, C_B are buck converter inductor and output capacitor, respectively. By processing partial power, it decreases the volume of both the device wafer and heatsink. The inductor in this topology can be decreased obviously compared with the AC-side inductors in other multilevel boost inverters. All the switches Q_{bi}, Q_{bi}', Q_{wi}, Q_{wi}' in the resonant switched capacitor cells work at the switching frequency equal to resonant frequency so that the Zero Current Switching can be achieved. The duty cycles of these switches are equal to 0.5. The switches Q_B, Q_B' in the buck converter voltage regulator are controlled with the modulation waveforms shown as *Control_Buck* in Fig. 4. The four switches $S_1 \sim S_4$ in the full-bridge unfolder operates at 60Hz line frequency.

To illustrate that this topology can help decrease the leakage ground current, four operating equivalent circuits are drawn in Fig. 2. C_{p1} and C_{p2} are parasitic capacitors between PV panel positive, negative terminals and grounded frame, respectively. Take one switched capacitor cell as an example. When S_1 and S_4 are ON, the common-mode voltage V_{CM} can be found by Eq. (1) [6]:

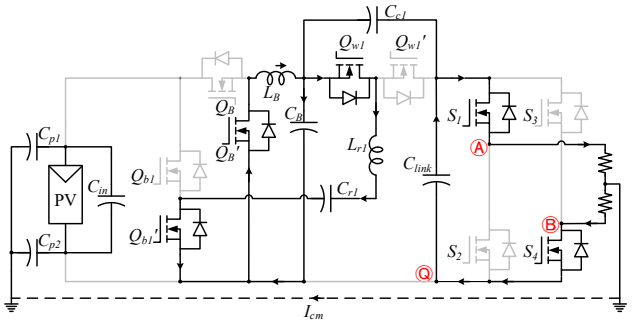
$$V_{CM} = \left(V_{AQ} + V_{BQ}\right)/2 \tag{1}$$

In Mode 1 and 2, the circuit operates at 1:1 voltage conversion ratio and $V_{CM} = (V_{in}+0)/2 = V_{in}/2$. In Mode 3 and 4, it works at 1:2 voltage conversion ratio and $V_{CM} = (2V_{in}+0)/2 = V_{in}$. When the voltage conversion ratio is fixed, the common-mode voltage is constant. So, the ground leakage current would be small [6].

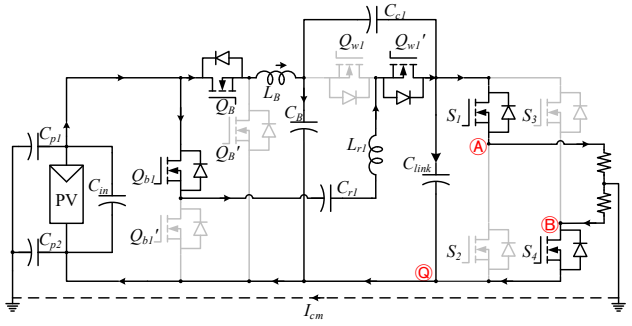
To explain operation principles of the proposed resonant multilevel modular boost inverters, three switched capacitor



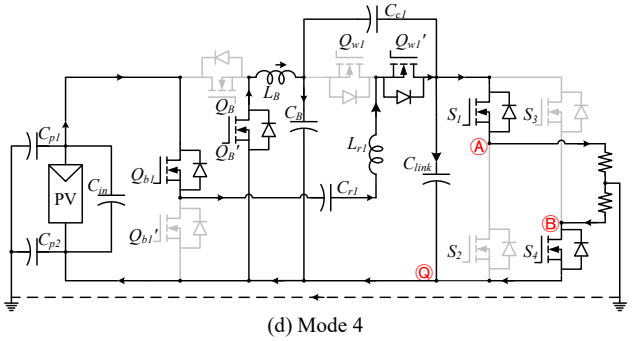
(a) Mode 1



(b) Mode 2



(c) Mode 3



(d) Mode 4

Fig. 2. Equivalent circuits of the proposed 6-level inverter (S_1, S_4 ON)

cells are used. The control logic is presented in Fig. 3. The key control signals are shown in Fig. 4. There are 4 steps in the DC staircase waveform. The Fourier series of an *n*-step staircase waveform [33] is given in Eq. (2):

$$V(\omega t)=\frac{4V_{in}}{\pi}\sum_{k=1,3,5\cdots}\left\{\left[\cos(k\theta_1)+\cos(k\theta_2)+\cdots \quad :\theta_n)\right]\cdot\frac{\sin(k\omega t)}{k}\right\} \quad (2)$$

where, n is the number of steps, i.e. 4 in this case. To minimize the total voltage harmonic distortion, the 7th and 11th harmonics can be eliminated by calculating suitable conduction angles, i.e. θ_1, θ_2, θ_3 in the 4-step staircase.

$$\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)=0 \quad (3)$$

$$\cos(11\theta_1)+\cos(11\theta_2)+\cos(11\theta_3)=0 \quad (4)$$

$$\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)=3m_a \quad (5)$$

where, m_a is the modulation index. By combining the three equations (3), (4) and (5), three conducting angles can be calculated.

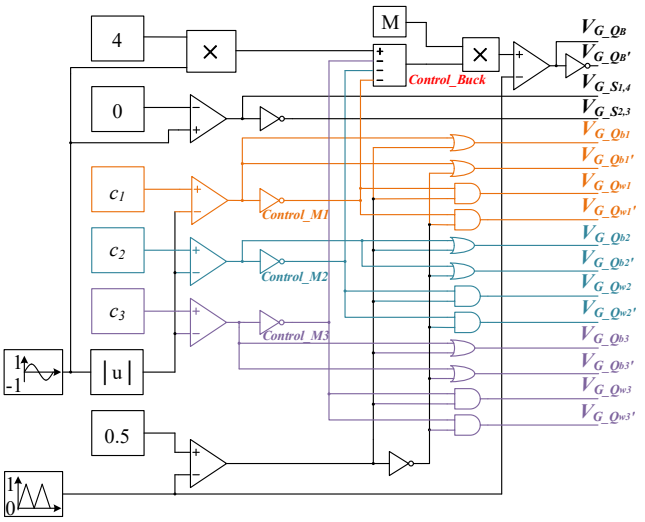


Fig. 3. Control logic of the proposed resonant 8-level modular boost inverter with a full-bridge unfolder

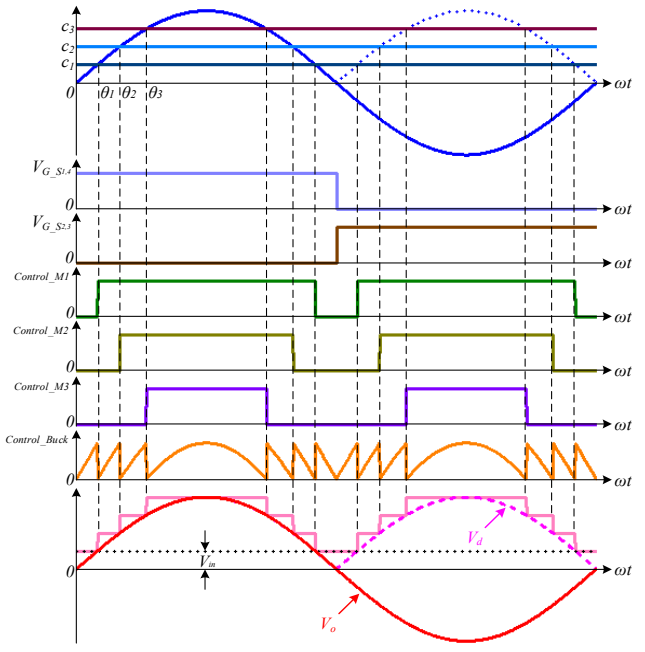


Fig. 4. Key control waveforms of the proposed resonant 8-level modular boost inverter with a full-bridge unfolder

III. Operation Principles of The Differential-Mode Resonant Multilevel Modular Boost Inverter

The differential-mode resonant multilevel modular boost inverter also based on the resonant switched capacitor cell is shown in Fig. 5. One significant difficulty in the differential-mode inverters is how to avoid the output capacitors of the two DC/DC converters from charging and discharging with each other [32][34][35]. In traditional differential-mode boost inverters, both two converters are controlled to work in full cycle, which increases the total switch conduction and switching loss. In this paper, a half cycle modulation method is proposed as Fig. 6 shows. By switching on the wing-side

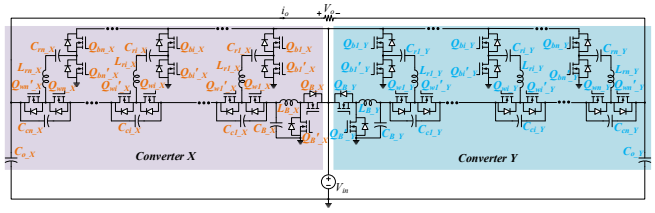


Fig. 5. Proposed differential-mode resonant multilevel boost inverter

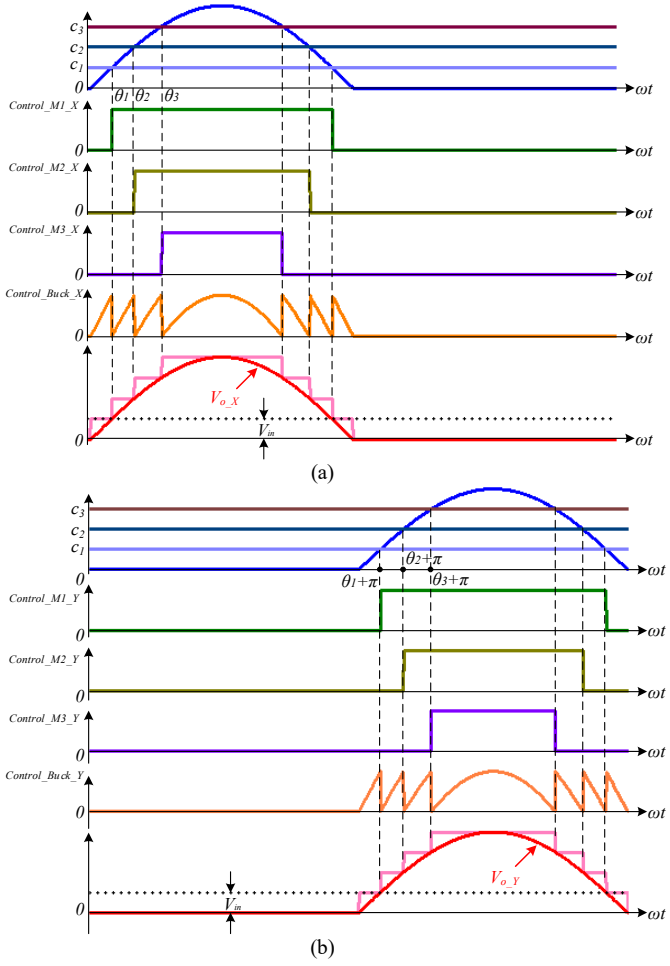


Fig. 6. Control waveforms for (a) Converter X and (b) Converter Y in the differential-mode resonant 8-level modular boost inverter

switches and the buck converter lower-side switch in the inactive converter, the output capacitor of the working converter wouldn't charge the output capacitor of the inactive converter. When one converter is working, the output capacitor of the other converter is resonating with the buck converter inductor and capacitor by keeping the buck converter lower-side switch staying ON. For example, when

the Converter X is working, the buck converter switch $Q_{B'\_Y}$ and all the wing-side switches of Converter Y are turned on so that the output capacitor C_{o_Y} of the converter Y will not be charged by the output capacitor C_{o_X} of the converter X while C_{o_Y} is resonant with L_{B_Y} and C_{B_Y}.

IV. Simulation, Analysis and Comparison

In this paper, 48V input voltage is used to represent the solar panels. Seven resonant switches-capacitor cells are used to realize 8 times voltage conversion ratio. The ideal output voltage peak value is 384V. To make this inverter adaptable to the 240V RMS AC output voltage requirement, the modulation index M is calculated in Eq. (6):

$$M = 240/(384/\sqrt{2}) = 0.88388 \quad (6)$$

The designed key components are shown in Table I. The corresponding parameters are applied in the simulation.

TABLE I. Key components of resonant 16-level modular boost inverter with an unfolder

Name	Symbol	Part Number	Company	Key Parameters
Resonant inductor	L_{ri}	SLC1049-101	Coilcraft	105nH, I_{sat} = 50A
Resonant capacitor	C_{ri}	GRM32D7U2E473JW31#	Murata	U2J / 47nF, 20 pcs per cell
Switches in resonant converter	Q_{wi}, Q_{wi}', Q_{bi}, Q_{bi}'	EPC2022	EPC	V_{dss} 100V, I_d 90A
Switches in buck regulator	Q_B, Q_B'			
Inductor in buck regulator	L_B	XAL1350-302	Coilcraft	3μH, I_{sat} = 37A, 2 pcs in series
Switches in full-bridge unfolder	S_1~S_4	GS66508B	Gan Systems	V_{dss} 650V, I_d 30A
Gate driver for EPC2022	GD	LM5113	TI	Peak source/sink current: 1.2/5A

A. Simulation and Analysis

The simulation is conducted in PLECS. Input voltage is 48V. Resistive load is 17.56Ω. The Buck converter inductance is 5μH. The corresponding results are shown in Fig. 7 for the 4kW resonant 16-level modular boost inverter with an unfolder. The top five waveforms in Fig. 7 are buck converter control reference signal V_{ref}, buck converter output voltage V_{o_buck}, dc-link voltage before the unfolder V_d, input voltage V_{in} and AC voltage after the unfolder V_o, current of the unfolder switches I_{S1}~I_{S4}, respectively. The bottom two waveforms show the current of switches in the resonant cells I_{sw} and current of buck converter switches I_{QB}, I_{QB}' at the 8X-level output voltage plateau.

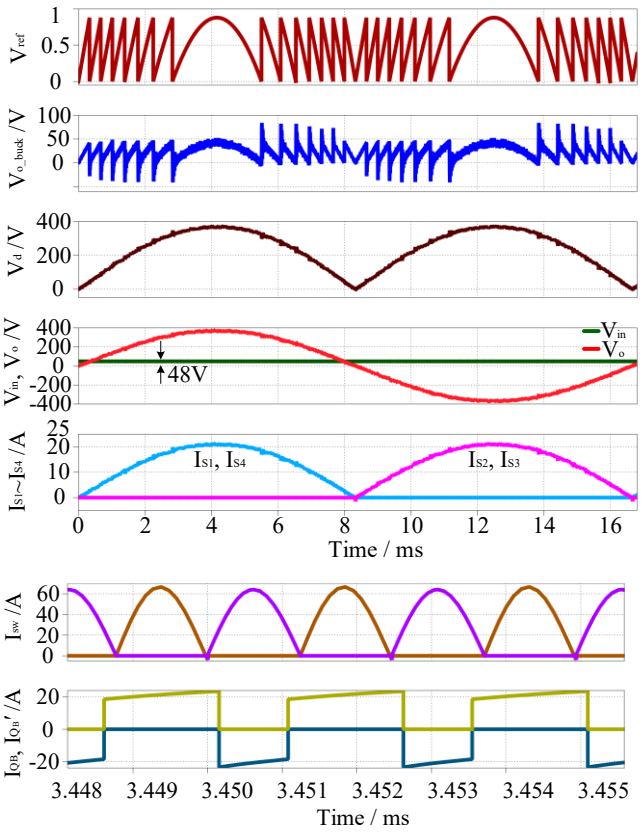


Fig. 7. Simulation results of proposed resonant 16-level modular boost inverter with a full-bridge unfolder

For the differential-mode switched capacitor inverter, the simulation results are shown in Fig. 8. The top six waveforms are buck converter control reference signals V_{ref1}, V_{ref2}, buck converter output voltages V_{o_buck1}, V_{o_buck2}, two converter output voltages V_{o_X}, V_{o_Y}, inverter input voltage V_{in}, and output voltage V_o, respectively. The bottom two waveforms are the current of switches in the resonant cells I_{sw_X} and current of buck converter switches I_{QB_X}, I_{QB_X}' at the 8X-level output voltage plateau. These current waveforms are from Converter X. The corresponding Converter Y current waveforms have the same shapes but with half the line period delay.

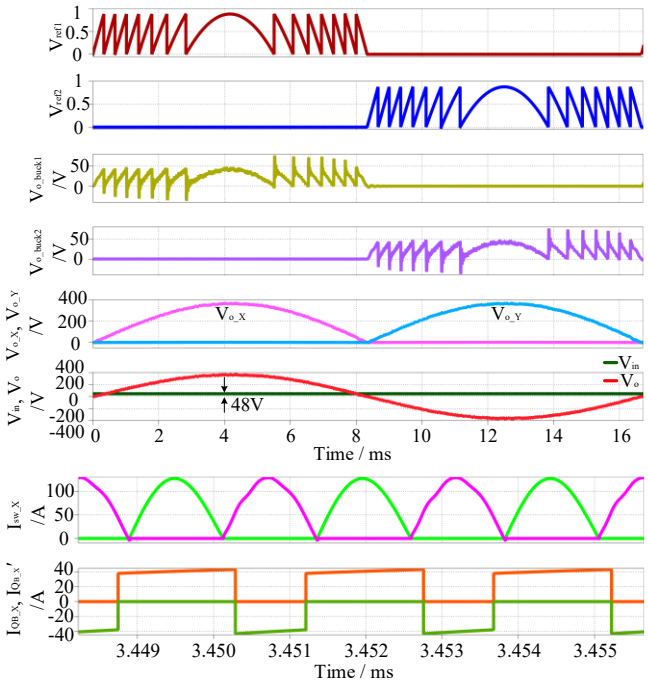


Fig. 8. Simulation results of proposed resonant 16-level modular boost inverter in differential mode

B. Stress Analysis

To analyze the switch stress, the switched capacitor multilevel modular boost inverter in [22] is used for the comparison due to the similar modular structure and switched capacitor based cells. The following comparisons are based on the simulation results of 16-level boost inverters. In the proposed two inverter topologies, all the

switches in the cells have the same voltage stress equal to input voltage. Two normalized stress parameters are used for fair comparison. The total normalized conduction power stress is defined as Eq. (7):

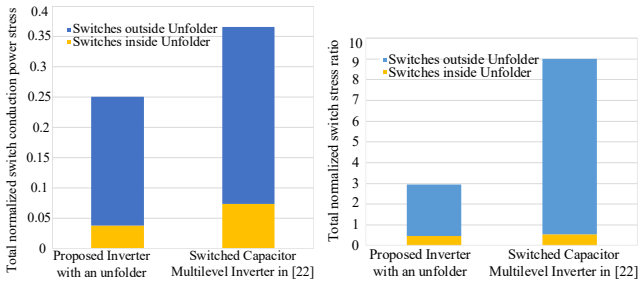
$$P_{cond}^{*} = N \cdot \left(\frac{I_{SW\_RMS}}{I_{out\_RMS}} \right)^{2} \cdot R_{DS\_ON} \tag{7}$$

where, N is the number of switches, I_{SW_RMS} is the switch RMS current, I_{out_RMS} is the nominal load RMS current, R_{DS_ON} is the switch on-resistance. According to the comparison result in Fig. 9 (a), the proposed inverter with an unfolder has less total normalized switch conduction power stress compared with the typical non-resonant switched capacitor multilevel modular boost inverter.

Another index used for comparison is the total normalized switch stress ratio, which is defined in Eq. (8):

$$N \cdot I_{SW\_RMS}^{*} \cdot V_{SW}^{*} = N \cdot \frac{I_{SW\_RMS}}{I_{out\_RMS}} \cdot \frac{V_{SW}}{V_{out\_RMS}} \tag{8}$$

where, V_{SW} is the switch voltage stress, V_{out_RMS} is the output RMS voltage. From the comparison result in Fig. 9 (b), the proposed inverter with an unfolder has smaller total normalized switch stress ratio.



(a) (b)

Fig. 9. Comparison of (a) total normalized switch conduction power stress and (b) total normalized switch stress ratio

C. Relative Total Semiconductor Chip Area Comparison

When the comparison is made among different topologies, the semiconductor design constraints need to be considered [36]. Based on the same output power rating, a comparison is conducted between the proposed inverter and the typical non-resonant multilevel modular boost inverter in [22]. Although by using the topology in [22], only 7 switches are needed in the switched capacitor cells for the 16-level boost inverter, 14 diodes with even larger die size have been applied. In this comparison, the switches in the switched capacitor cells and buck converter are EPC2022 with much smaller die size (6.05 mm * 2.3 mm), while the switches in the unfolder are GS66508B from Gan Systems with die size of 7.0 mm * 8.4 mm. From Fig. 10, it can be seen that in the proposed inverter, the total chip area is decreased by 59.87% compared with the typical non-resonant switched capacitor multilevel modular boost inverter. Thus, it utilize the semiconductor chip die sizes more efficiently.

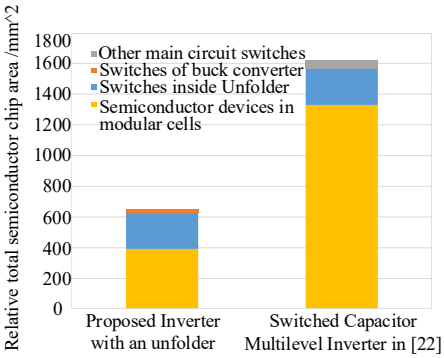


Fig. 10. Comparison of relative total semiconductor chip area

V. Actual Simulation, Prototype and Test Results

To experimentally verify the proposed resonant multilevel modular boost inverter with an unfolder, two switched capacitor modules and one full-bridge inverter are applied. Since the test including the buck converter voltage regulator is under way, this paper will only show the test results without partial power voltage regulator. Thus, the simulation of a resonant 6-level modular boost inverter with a full-bridge unfolder needs to be carried out to see whether the theoretical analysis and tested waveforms match or not. The schematic corresponding to both the simulation and the following tests is shown in Fig. 11.

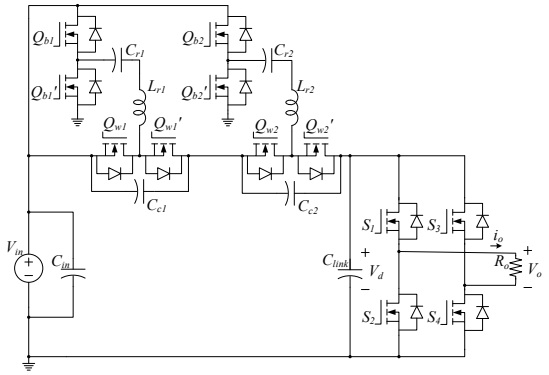
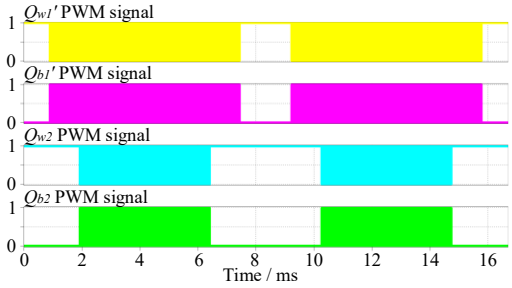
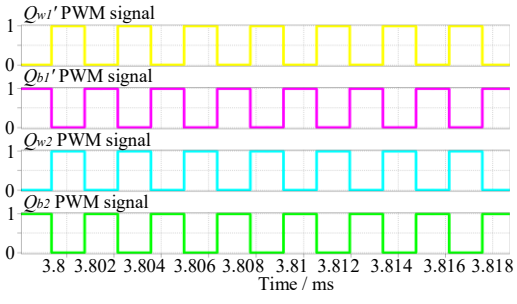


Fig. 11. Tested 6-level boost inverter prototype schematic

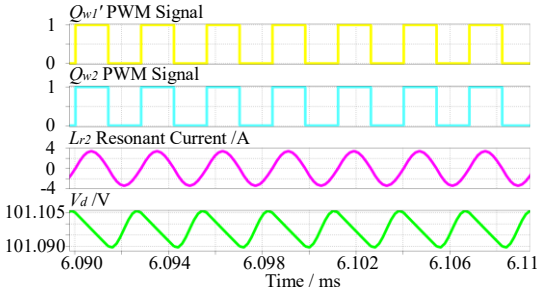
Simulation with 35V input voltage has been conducted in PLECS. The simulation results are shown in Fig. 12 (a)~(e). The top two waveforms in Fig. 12 (a) and (b) (in yellow and pink) show two complementary PWM signal waveforms of Q_{w1}' and Q_{b1}' in the switched capacitor cell close to the dc



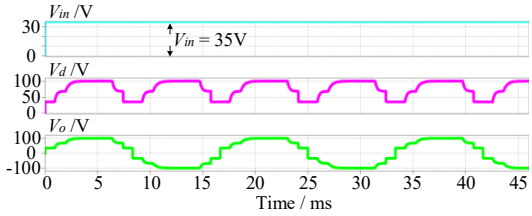
(a) PWM signals of the switches in resonant switched capacitor cells



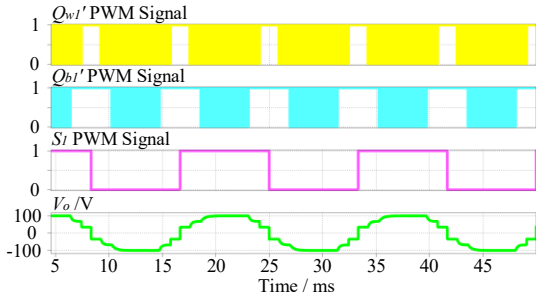
(b) Enlarged PWM signals of switches in resonant switched capacitor cells



(c) Simulated resonant current and dc-link voltage in relation to two PWM signals at 3X-level output voltage plateau (V_{in} = 35V)



(d) Simulated input voltage, dc-link voltage and output voltage (V_{in} = 35V)



(e) Simulated output voltage in relation to PWM signals of two switched capacitor cells and full-bridge unfolder (V_{in} = 35V)

Fig. 12. Simulation results of a resonant 6-level modular boost inverter with a full-bridge unfolder

power source side. The bottom two waveforms (in sky blue and green) are the corresponding waveforms of Q_{w2} and Q_{b2} in the switched capacitor cell close to the load side. Resonant current and dc-link voltage can be observed together with two PWM signals in Fig. 12 (c). These waveforms are corresponding to the 3X-level output voltage plateau. To conveniently analyze the voltage conversion ratio, input voltage, dc-link voltage and output voltage are placed in one scope as Fig. 12 (d) shows. In Fig. 12 (e), three PWM signals from two switched capacitor cells and the full-bridge unfolder are captured together with the output voltage. From the timing relationship, the control is verified and can be further used in the experiments.

The overall test platform is presented in Fig. 13, where ①, ②, ③, ④ refer to oscilloscopes, 5V power supply, main power supply, and computer, respectively. The bird's-eye view of the test platform is shown in Fig. 14, where ⑤ is DSP and FPGA control board, ⑥ are opto-receiver interface control boards, ⑦ is the designed resonant multilevel modular boost converter, ⑧ is the full-bridge unfolder, ⑨ is the bleeder resistor (35.3 kΩ/20W Micron®), ⑩ is the 94Ω resistive load. The PWM signals are generated by the control board including TI® DSP 28335 IC and Xilinx® FPGA Spartan-6 XC6SLX9 IC. Five small opto-receiver interface boards are applied to be connected with four resonant switched capacitor cells and a full-bridge unfolder to generate complementary PWM signals for each

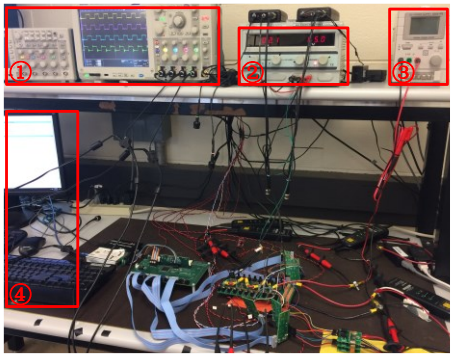


Fig. 13. Overall perspective of the test platform

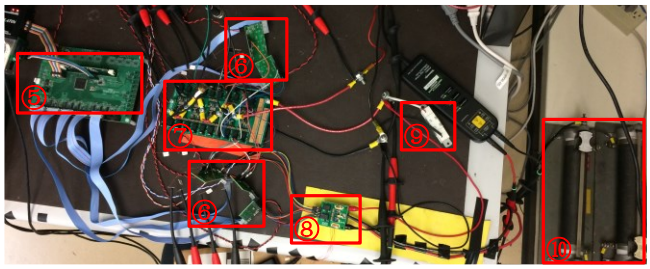
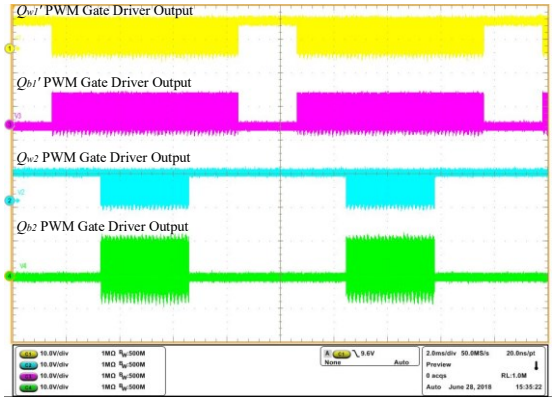


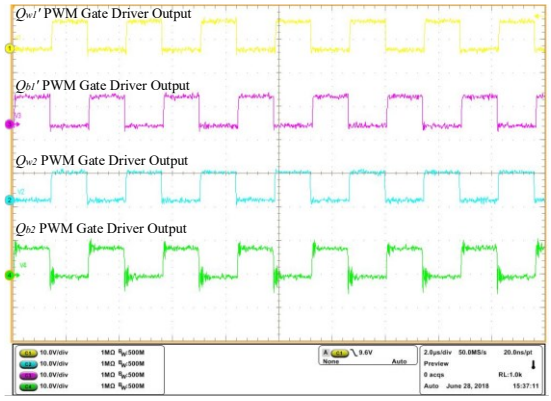
Fig. 14. Bird's-eye view of the test platform

of them. The switching frequency is set to be close to the resonant frequency. Here, 357.1 kHz switching frequency has been used. The deadtime is 60.003 ns for the five groups of PWM signals. In the main power circuit, a 35.3 kΩ/20W bleeder resistor is paralleled to the dc-link capacitor so that the stored capacitive energy is safely released when all the unfolder switches are OFF. In the measurement, all the voltages are captured by active differential probes. The resonant current is measured by PEM Rogowski current waveform transducer CWTUM/03/B with the sensitivity 100mV/A and the peak current 60A.

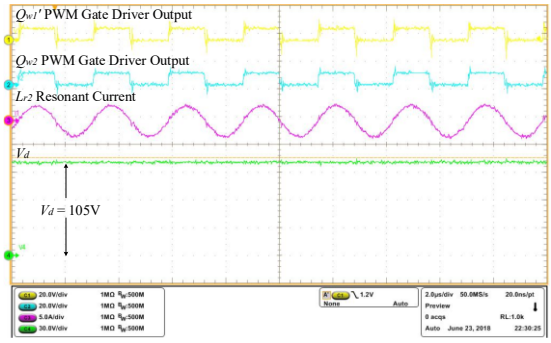
The test results are shown in Fig. 15. From the gate driver's gate resistor voltage waveforms in Fig. 15 (a) and (b), the simulated control strategies are verified. Silicon Labs SI8271GB-IS isolated gate driver IC is selected. As can be seen from the figures, the gate driver output voltage amplitude is around 9V. Fig. 15 (c) gives the resonant current waveform in the switched capacitor cell close to load side. These waveforms are captured at the 3X-level output voltage plateau, which is around 105V. The resonant current amplitude is about 6A, which matches the simulation result in Fig. 12 (c). Three tested voltage waveforms, i.e. input voltage, dc-link voltage and output ac voltage are put together in Fig. 15 (d). In Fig. 15 (e), from



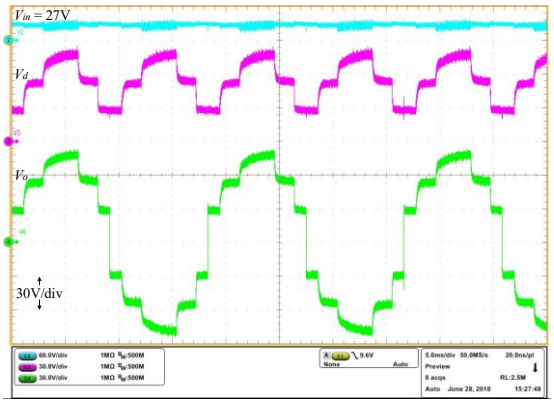
(a) Gate driver outputs of 4 switches in two different switched capacitor cells



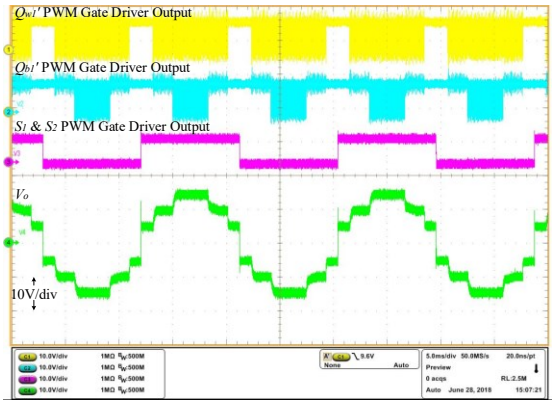
(b) Enlarged gate driver outputs of 4 switches in two switched capacitor cells



(c) Tested resonant current and dc-link voltage in relation to two PWM signals at 3X-level output voltage plateau (V_{in} = 35V)



(d) Tested input voltage, dc-link voltage and output voltage (V_{in} = 27V)



(e) Tested output voltage in relation to PWM signals of two switched capacitor cells and the full-bridge unfolder (V_{in} = 5V)

Fig. 15. Test results of a resonant 6-level modular boost inverter with a full-bridge unfolder

the timing relationship between output voltage and three gate driver PWM outputs, the tested waveforms match the simulation results in Fig. 12 (e).

VI. Conclusion and Future Work

This paper proposes two non-isolated resonant multilevel modular boost inverter topologies based on resonant switched capacitor cells and a partial power processed buck converter. The common-mode voltage and ground leakage current have been analyzed in single-phase PV inverter applications. The operation principles and control strategies of the resonant multilevel modular boost inverters operating with an unfolder and in differential mode have both been illustrated, respectively. PLECS simulation results show the validity of the boost DC/AC function in both the two topologies. They are especially suitable for the single-phase non-isolated photovoltaic applications with low input voltage, high input current, high voltage transfer ratio and small ground leakage current. From the simulation results, a significant decrease of the inductance in the buck converter voltage regulator has been verified compared with the normally used large AC-side filtering inductance. Stress analysis has shown that total normalized switch conduction power stress and total normalized switch stress ratio are smaller in the proposed topology with an unfolder than in the typical non-resonant switched capacitor multilevel modular inverter. Relative total semiconductor chip area has been decreased by 59.87% in the resonant 16-level modular boost inverter with an unfolder included. Test results show the validity of the boost inverter function when relatively simple control strategies are implemented. More test results with buck converter voltage regulator included will be shown in future publications. Besides, detailed device selection methods, PCB design, theoretical calculations, more higher-voltage higher-power test results, ZCS waveforms, corresponding power loss breakdown and efficiency evaluation will also be presented.

References

[1] S. V. Araújo, P. Zacharias, and R. Mallwitz, "Highly efficient single-phase transformerless inverters for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3118–3128, Sep. 2010.

[2] B. N. Alajmi, K. H. Ahmed, G. P. Adam, and B. W. Williams, "Single-phase single-stage transformer less grid-connected PV system," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2664–2676, Jun. 2013.

[3] D. Cao, S. Jiang, X. Yu, and F. Z. Peng, "Low-Cost Semi-Z-source Inverter for Single-Phase Photovoltaic Systems," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3514–3523, Dec. 2011.

[4] Ó. López, F. D. Freijedo, A. G. Yepes, P. Fernández-Comesaña, J. Malvar, J. Doval-Gandoy, and R. Teodorescu, "Eliminating ground current in a transformerless photovoltaic application," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 140–147, 2010.

[5] M. Calais and V. G. Agelidis, "Multilevel converters for single-phase grid connected photovoltaic systems-an overview," in *Industrial Electronics, 1998. Proceedings. ISIE '98. IEEE International Symposium on*, 1998, vol. 1, pp. 224–229 vol.1.

[6] T. Kerekes, R. Teodorescu, P. Rodriguez, G. Vazquez, and E. Aldabas, "A New High-Efficiency Single-Phase Transformerless PV Inverter Topology," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 184–191, Jan. 2011.

[7] Ó. López, R. Teodorescu, F. Freijedo, and J. Dovalgandoy, "Leakage current evaluation of a singlephase transformerless PV inverter connected to the grid," in *2007 IEEE Applied Power Electronics Conference and Exposition - APEC*, 2007, pp. 907–912.

[8] R. González, E. Gubía, J. López, and L. Marroyo, "Transformerless single-phase multilevel-based photovoltaic inverter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2694–2702, Jul. 2008.

[9] R. González, J. López, P. Sanchis, and L. Marroyo, "Transformerless inverter for single-phase photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 693–697, Mar. 2007.

[10] S. Hu, X. He, W. Li, Y. Mei, L. Lin, and F. Cao, "Highly efficient and reliable inverter concept-based transformerless photovoltaic inverters with tri-direction clamping cell for leakage current elimination," *IET Power Electron.*, vol. 9, no. 8, pp. 1675–1683, Jun. 2016.

[11] J. Rodríguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, 2002.

[12] G. J. Su, "Multilevel DC-link inverter," *IEEE Trans. Ind. Appl.*, vol. 41, no. 3, pp. 848–854, 2005.

[13] Y. Li, X. Lyu, and D. Cao, "A Zero-Current-Switching High Conversion Ratio Modular Multilevel DC-DC Converter," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 1, pp. 151–161, Mar. 2017.

[14] Y. Li, X. Lyu, and D. Cao, "A resonant modular multilevel DC-DC converter with zero current switching for MVDC application," in *2017 IEEE Applied Power Electronics Conference and Exposition - APEC*, 2017, pp. 164–169.

[15] B. Curuvija, X. Lyu, Y. Li, and D. Cao, "Single-wing ladder resonant multilevel converter," in *WiPDA 2016 - 4th IEEE Workshop on Wide Bandgap Power Devices and Applications*, 2016, pp. 328–333.

[16] Y. Li, B. Curuvija, X. Lyu, and D. Cao, "Multilevel modular switched-capacitor resonant converter with voltage regulation," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2017, pp. 88–93.

[17] Y. Li, X. Lyu, and D. Cao, "A high voltage gain modular multilevel DC-DC converter," in *2015 IEEE Energy Conversion Congress and Exposition, ECCE 2015*, 2015, pp. 3535–3541.

[18] D. Cao, X. Lyu, and Y. Li, "Multilevel modular converter with reduced device count for hybrid and electric vehicle," in *2015 IEEE Transportation Electrification Conference and Expo, ITEC 2015*, 2015, pp. 1–6.

[19] X. Lyu, "High-Power-Density Converter for Renewable Energy Application," Ph.D. Dissertation, Electrical and Computer Engineering Dept., North Dakota State University, 2017.

[20] B. Curuvija, Y. Li, X. Lyu, and D. Cao, "Single-Wing resonant multilevel converter featuring reduced number of resonant inductors," in *2017 IEEE Energy Conversion Congress and Exposition, ECCE 2017*, 2017, vol. 2017–Janua, pp. 1733–1738.

[21] D. Cao, X. Lyu, Y. Li, Z. Ni, J. Johnson, S. Jiang, and C. Nan, "An ultra efficient composite modular power delivery architecture for solar farm and data center," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2018, vol. 2018–March, pp. 73–80.

[22] Y. Ye, K. W. E. Cheng, J. Liu, and K. Ding, "A step-up switched-capacitor multilevel inverter with self-voltage balancing," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6672–6680, Dec. 2014.

[23] L. He and C. Cheng, "A Flying-Capacitor-Clamped Five-Level Inverter Based on Bridge Modular Switched-Capacitor Topology," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7814–7822, Dec. 2016.

[24] X. Lyu, Y. Li, and D. Cao, "A high power density single-phase inverter with in-series and -parallel power decoupling method," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 2549–2554.

[25] X. Lyu, N. Ren, Y. Li, and D. Cao, "A SiC-Based High Power Density Single-Phase Inverter with In-Series and In-Parallel Power Decoupling Method," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 3, pp. 893–901, Sep. 2016.

[26] X. Lyu, Y. Li, N. D. Nguyen, Z. Ni, and D. Cao, "A high-power-density single-phase inverter with pulse current injection power decoupling method," in *ECCE 2016 - IEEE Energy Conversion Congress and Exposition, Proceedings*, 2016, pp. 1–8.

[27] X. Lyu, Y. Li, Z. Ni, and D. Cao, "A minimized DC-bus capacitor with active combinational decoupling method for DC-AC application," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2017, pp. 2239–2244.

[28] X. Lyu, Y. Li, and D. Cao, "DC-Link RMS Current Reduction by Increasing Paralleled Three-Phase Inverter Module Number for Segmented Traction Drive," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 1, pp. 171–181, Mar. 2017.

[29] X. Lyu, H. Zhou, B. Curuvija, and D. Cao, "DC-link RMS current reduction by increasing paralleled 3-phase inverter module number for segmented traction drive," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2017, pp. 906–911.

[30] Z. Ni, X. Lyu, O. P. Yadav, and D. Cao, "Review of SiC MOSFET based three-phase inverter lifetime prediction," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2017, pp. 1007–1014.

[31] L. He, C. Cheng, J. Nai, and W. Chen, "A Bridge Modular Switched-Capacitor-Based Multilevel Inverter," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 632–636.

[32] G. V. Silva, R. F. Coelho, and T. B. Lazzarin, "Switched capacitor boost inverter," in *IEEE International Symposium on Industrial Electronics*, 2016, vol. 2016–Novem, pp. 528–533.

[33] L. M. Tolbert, Fang Zheng Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, 1999.

[34] Y. Tang, Y. Bai, J. Kan, and F. Xu, "Improved Dual Boost Inverter with Half Cycle Modulation," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7543–7552, 2017.

[35] Y. Fang and X. Ma, "A novel PV microinverter with coupled inductors and double-boost topology," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 3139–3147, 2010.

[36] T. Friedli, M. Hartmann, and J. W. Kolar, "The Essence of Three-Phase PFC Rectifier Systems -- Part II," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 543–560, Feb. 2014.