A GaN Switched Tank Converter with Partial Power Voltage Regulation for Electric Vehicle Applications

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***Abstract*—A new Switched Tank Converter (STC) with Partial Power Voltage Regulation (PPVR) is introduced for electric vehicle applications. It offers a flexibly adjustable conversion ratio for a wide-range battery voltage. The unregulated stage is modularized with resonant switched capacitor converters. All device voltage stresses are equal to the input voltage. The efficient unregulated stage processes the bulk of system power and the less efficient regulated stage processes a small amount of power. Thus, high overall efficiency can be achieved. A new index called Semiconductor Loss Index (SLI) is defined as a function of semiconductor die area to evaluate different power topologies. It is helpful to analyze the impact of each switch die area, different operated output power, switching frequency, and conversion ratio on the total device power loss. With the same total semiconductor die area, the proposed converter can achieve less than 1/3 device total power loss compared with boost converter. A 4-kW 1200V output converter prototype with 200V~400V input voltage range is developed, which combines a 6 times conversion ratio STC with a PPVR buck converter. The overall full-load efficiency of designed 4-kW converter can reach to 97.71%. Simulation, prototype and experiment results are presented to verify the validity of the proposed converter.**

Keywords—resonant switched capacitor converter, switched tank converter, voltage regulation, partial power, semiconductor loss index (SLI), ZCS

I. INTRODUCTION

Compact, high-efficiency boost converters to interface the battery and the inverter have been studied widely these days in the electric vehicles [1][2]. Commonly, a traditional boost [3]–[9], interleaved boost [10], buck-boost [11][12], and isolated dual active bridge [13] converters have been used to step up the voltage from the battery to DC bus for the inverter. However, the traditional boost converter suffers from low efficiency, high switch voltage and current stresses when the converter operates at high conversion ratios. To overcome these problems, sigma converter [14][15], boost composite converter [16][17], quasi-parallel voltage regulator [18] have been developed. These new topologies offer higher system efficiencies with lower switch voltage and current stresses than the traditional boost converter. They normally use multiple converter topologies combined in an overall system to form a composite structure. It is composed of an unregulated stage and a voltage regulated stage. This is important for motor drive applications because the stable DC-link voltage is critical to the motor control. The topologies mentioned above mainly consist of a full-bridge converter and a buck converter [14][15] or a boost converter [16][17], which is in series with the output but share the same input voltage. The full-bridge converter acts as the unregulated stage while the others offer the voltage regulation. The system efficiency is high because the unregulated stage processes most of the overall power while the less efficient buck or boost converter processes a small amount of power to keep the output voltage regulated.

The resonant switched capacitor converters have been well studied these years for high efficiency and high power density [19]–[27]. Based on the demonstrated Switched Tank Converter (STC) topology [23], a buck-boost converter has been added to realize the partial power voltage regulation [25]. The proposed boost converter in this paper combines a new STC unregulated stage and a buck converter based voltage regulated stage. It utilizes a modular, resonant converter to offer low switch voltage and current stress, which makes it possible to optimize the devices and increase the power density. It can also achieve soft switching, which helps improve the efficiency.

To evaluate different topologies, many performance indices have been proposed. Relative Total Semiconductor Chip Area is introduced in [28]. However, it fails to consider the relationship between die area and the device power loss. Total Switching Device Power is defined in [29]. But the product of switch voltage and current stresses cannot indicate the optimized die area requirement for different topology designs. Baliga's Figure of Merit is proposed in [30], which is irrelevant to the active die area. But when it is viewed from the perspective of device power loss, this device-level index cannot be used to evaluate different topologies by using only on-resistance and the total gate charge. This paper tries to use another performance index to compare different topologies by analyzing the relationship between the die area and the device power loss.

II. OPERATION PRINCIPLES OF PROPOSED CONVERTER

A generalized topology of the proposed new Switched Tank Converter (STC) with Partial Power Voltage Regulation (PPVR) is shown in Fig. 1. The unregulated STC is composed of N basic cells to achieve a 1:(N+1) voltage conversion ratio. In each cell, there are four switches S_i, one clamping capacitor C_{ci}, one resonant capacitor C_{ri} and one resonant inductor L_{ri}. The drain-source voltage overshoot during switching transient is alleviated by the clamping capacitors C_{ci}. The voltage regulation is realized by the partial power voltage regulator, which can be buck, boost or buck-boost converters. The switch voltage stress of both the STC and PPVR converter is equal to the input voltage.

In this paper, the proposed converter is designed for an electric vehicle application where the battery voltage ranges from 200 V to 400 V. The output voltage is 1200 V for the DC-link of a 4-kW inverter to drive the electric motors and generators. Due to the wide-range battery voltage, a conversion ratio from 3 to 6 is required. Below, the operation principles of the converter are demonstrated including the STC part and regulated PPVR buck converter part.

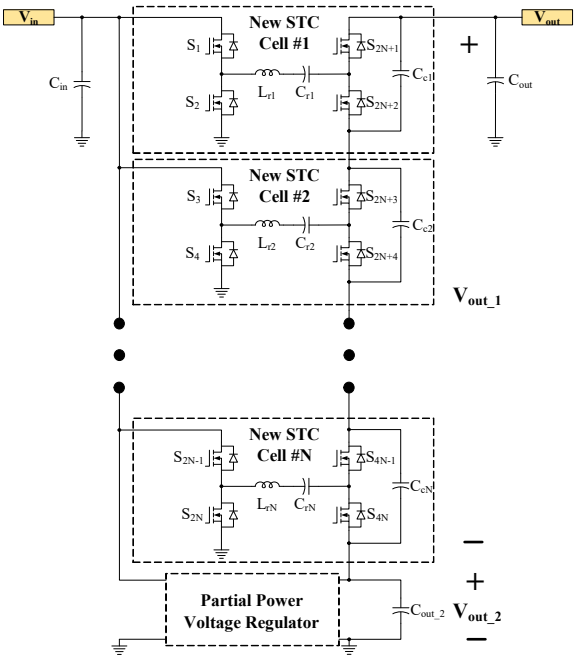


Fig. 1. Generalized new STC integrated with partial power processed voltage regulator

A. 1:6 new STC as the unregulated stage

A 1:6 new STC shown in Fig. 2 is designed considering the conversion ratio range. The two switching modes of the STC are shown in Fig. 3. All the switches marked in blue work simultaneously for half the switching cycle, while the

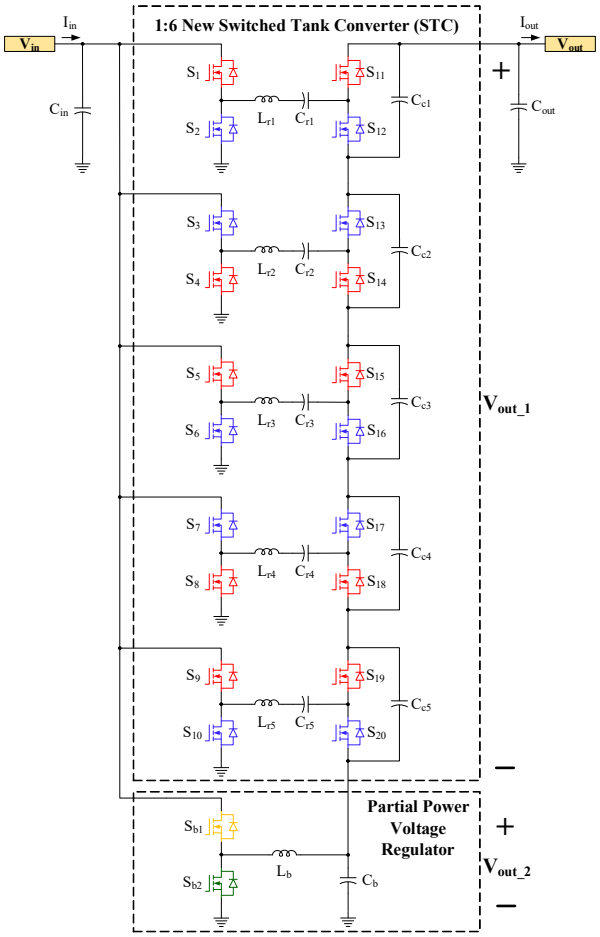
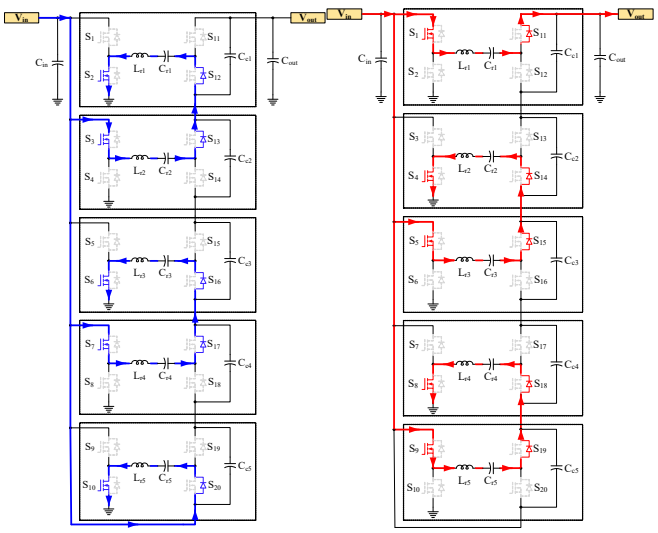


Fig. 2. Proposed 1:6 new STC integrated with a buck converter



(a) Mode 1 (b) Mode 2

Fig. 3. Two switching states of the proposed 1:6 STC

other switches marked in red operate complementarily at another half cycle. The DC voltages of C_{r5}, C_{r4}, C_{r3}, C_{r2} and C_{r1} are V_{in}, $2V_{in}$, $3V_{in}$, $4V_{in}$, $5V_{in}$, respectively when they are charged to the steady state, so that the output voltage is $6V_{in}$. By controlling the number of active STC modules, the regulated stage can achieve discrete conversion ratios of 0~6.

In switching mode 1, the odd indexed resonant capacitors are charged. C_{r5} is charged by the input voltage. C_{r3} is charged by the input voltage and C_{r4}. And C_{r1} is charged by the input voltage and C_{r2}. In the switching mode 2, the even indexed resonant capacitors are charged. C_{r4} is charged by the input voltage and C_{r5}. C_{r2} is charged by the input voltage and C_{r3}. C_{r1} and input voltage together charge the output capacitor. During each mode, the resonant current is sinusoidal and starts from zero, which realizes the ZCS (Zero Current Switching) turn-on. Besides, by designing the switching frequency a little lower than the resonant frequency, the sinusoidal current reverses the polarity before the switches are turned off. By selecting a proper deadtime between the two complementary PWM signals, the current flowing through the body diode can be controlled to decrease to zero before the next half cycle starts. Therefore, all the switches can be turned off at ZCS.

The five clamping capacitors C_{c1}, C_{c2}, C_{c3}, C_{c4} and C_{c5} are used to alleviate the drain-source voltage overshoot of S_{11} to S_{20}. The switches voltage stress of all the switches is equal to the input voltage. Hence, lower voltage ratings can be realized for all the switches, which have smaller on-resistance and lower conduction loss.

B. Buck converter as the voltage regulated stage

With the addition of the PPVR stage, this converter can operate at any conversion ratio between 0 and 6. Assuming the total number of active STC modules is N, the duty cycle of the buck converter is D, the system conversion ratio can be found in Eq. (1).

$$V_o / V_{in} = N + D \tag{1}$$

By adjusting N and D, the conversion ratio can be tuned flexibly for various battery voltage ranges. Because the voltage stress on switches of proposed converter is equal to input voltage, the converter can utilize GaN power transistors

with 650V voltage rating. With 350V battery voltage and 1200V output voltage, the overall conversion ratio is 3.4286. The unregulated converter stage has 3 active modules and has a conversion ratio of 4. The inactive module works in a bypass mode where the switches closer to the output voltage side are on and the switches closer to the input voltage side are off. The regulated stage works at 0.4286 duty cycle so that the system conversion ratio is dropped down to 3.4286 and thus 1200 V output voltage is achieved. The power processed by the new STC and the regulated buck converter are presented in Eq. (2) and (3), respectively.

$$P_{STC} = V_{out\_1} \cdot I_{out} \tag{2}$$

$$P_{reg} = V_{out\_2} \cdot I_{out} \tag{3}$$

The overall efficiency can be calculated by Eq. (4).

$$\eta_{overall} = \frac{V_{out\_1}}{V_{out}} \cdot \eta_{STC} + \frac{V_{out\_2}}{V_{out}} \cdot \eta_{reg} \tag{4}$$

III. Evaluation of the Proposed Converter

To verify the effectiveness, a comparison is made between boost converter [3]–[9] and proposed converter. For a fair comparison, the relationship between theoretical limits of GaN & SiC on-resistance $R_{ds(on)}$ times die area A_{die} and blocking voltage V_B [31]–[33] is used by curve fitting. As shown in Fig. 4, theoretical $R_{ds(on)} \cdot A_{die}$ accounts for switch current stresses, which is suitable for the comparison of switches with various die sizes working at different RMS current. In order to reflect the real $R_{ds(on)} \cdot A_{die}$ of GaN & SiC bare dies, the die information from major wide-bandgap semiconductor manufacturers such as EPC, Gan systems, Cree and Rohm is plotted into Fig. 4 as well.

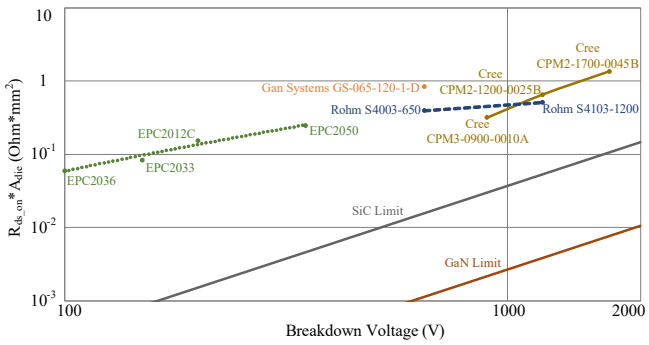


Fig. 4. Theoretical $R_{ds(on)} \cdot A_{die}$ versus. V_B including the real GaN & SiC device information from major semiconductor manufacturers

To evaluate the impact of different device technologies on converter topologies, the Semiconductor Loss Index (*SLI*) is defined in Eq. (5).

$$\begin{aligned} SLI &= \frac{1}{P_o}\left(P_{cond}(A_{die\_total}) + P_{sw}(A_{die\_total})\right) \\ &= P^*_{cond}(A_{die\_total}) + P^*_{sw}(A_{die\_total}) \\ &= P^*_{cond}(A_{die\_total}) + P^*_{Gate\_charge}(A_{die\_total}) \\ &+ P^*_{turn\_on}(A_{die\_total}) + P^*_{turn\_off}(A_{die\_total}) \end{aligned} \tag{5}$$

Where, P_{cond}, P_{sw} are total device conduction loss and switching loss, respectively. A_{die_total} is the total die area of the converter semiconductor devices. To evaluate the impact of semiconductor die area on device power loss, P_{cond}, P_{sw} are regarded as the functions of the total die area. P_{cond}^*, P_{sw}^* are the corresponding loss normalized by the output power P_o. Normalized switching loss can be further categorized into gate charge induced switching loss $P_{Gate\_charge}^*$, turn-on switching loss $P_{turn\_on}^*$ and turn-off switching loss $P_{turn\_off}^*$.

From Eq.(6.211) in [30], the device conduction loss is negatively proportional to the active die area. Hence, the device conduction loss can be expressed as Eq. (6) shows.

$$\begin{aligned} &P^*_{cond}(A_{die\_total}) \\ &= \frac{1}{P_o}\sum_{i=1}^{N}\left[I^2_{RMS\_S(i)} \cdot \left(R_{ds(on)}\right)_{(i)}\right] \\ &= \frac{1}{P_o}\sum_{i=1}^{N}\left(I^2_{RMS\_S(i)} \cdot \frac{\alpha_i(\xi_i, V_{B(i)})}{\kappa_i A_{die\_total}}\right) \end{aligned} \tag{6}$$

Where, N is the number of active switches, $I_{RMS\_S(i)}$ is the switch Root Mean Square (RMS) current, $R_{ds(on)}$ is the switch on-resistance. $\alpha_i(\xi_i, V_{B(i)})$ is the product of on-resistance and die area, determined by the device technology dependent coefficient ξ_i and the voltage rating $V_{B(i)}$. κ_i is the die cutting factor ranging from 0 to 1, reflecting different cutting strategies for the dies used by specific switches. The sum of each κ_i equals to 1.

According to Eq.(6.211) in [30], when the die area is enlarged, the input capacitance increases, which means larger gate current is needed to charge the input capacitor and thus increases the gate charge induced switching loss, which is presented in Eq. (7).

$$\begin{aligned} P^*_{Gate\_charge} &= \frac{1}{P_o}\sum_{i=1}^{N}\left[\left(Q_g\right)_{(i)} \cdot V_{gs(i)} \cdot f_{s(i)}\right] \\ &= \frac{1}{P_o}\sum_{i=1}^{N}\left(\beta_i \cdot \kappa_i A_{die\_total} \cdot V_{gs(i)} \cdot f_{s(i)}\right) \end{aligned} \tag{7}$$

Where, f_s is the switching frequency. Q_g is the total gate charge. V_{gs} is the difference of the maximum and minimum gate-source voltages. β_i is the total gate charge per die area, dependent on the device technology. Besides, turn-on and turn-off switching losses are explained in Eq. (8) and (9), respectively. The turn-on energy E_{on} and turn-off energy E_{off} are functions of turn-on and turn-off drain current.

$$P^*_{turn\_on} = \frac{1}{P_o}\sum_{i=1}^{N}\left[\left(E_{on}\right)_{(i)} \cdot f_{s(i)}\right] \tag{8}$$

$$P^*_{turn\_off} = \frac{1}{P_o}\sum_{i=1}^{N}\left[\left(E_{off}\right)_{(i)} \cdot f_{s(i)}\right] \tag{9}$$

The output capacitance C_{oss} discharge induced turn-on switching loss is part of the total turn-on switching loss. From Page 409 in [30], the gate-drain capacitance C_{gd} increases with the die area. From Eq.(6.174), (6.175), (6.178) in [30], the drain-source capacitance C_{ds} is positively proportional to the junction area. Thus, C_{oss} (equal to C_{gd} + C_{ds}) discharge induced turn-on switching loss is positively related to the die area. The C_{oss} induced turn-on switching loss is shown in Eq. (10).

$$P^*_{C_{oss}} = \frac{1}{P_o}\sum_{i=1}^{N}\left[C_{oss(i)}\cdot\left(V_{ds(i)}\right)^2\cdot f_{s(i)}\right] = \frac{1}{P_o}\sum_{i=1}^{N}\left[\gamma_i\cdot\kappa_i A_{die\_total}\cdot\left(V_{ds(i)}\right)^2\cdot f_{s(i)}\right] \quad (10)$$

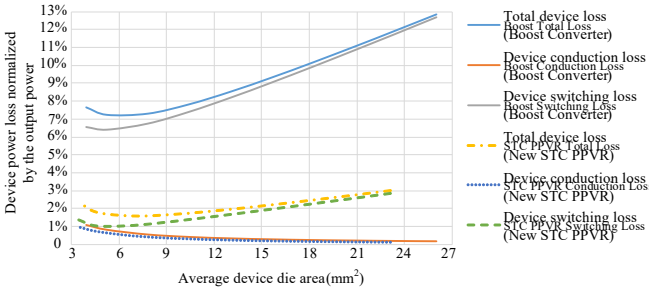
Where, V_{ds} is drain-source voltage. γ_i is the device output capacitance per die area, which is dependent on the device technologies as well. For a specific circuit topology, when the output power and switching frequency are fixed, theoretically it is possible to derive an optimum die area for each switch to achieve the minimized total device power loss. In other words, when the total device power loss is the same between two topologies under specific conditions, the one with smaller total die area can achieve more efficient die utilization. These two different evaluation perspectives based on the above *SLI* parameter can provide more comprehensive understandings between the total device power loss and semiconductor die area.

Boost or buck converter ZVS turn-on [34][35] and ZCS turn-off [36] are often realized by adding additional components and auxiliary circuits. Therefore, in this comparison, the boost converter inductance is designed in hard switching with 30% current ripple [37] considering the tradeoff between the size and the RMS current of the inductor. In order to demonstrate the advantage of the proposed converter, the 350V/1200V DC/DC step-up converter for electric vehicle application is evaluated. By designing the deadtime and making the switching frequency slightly smaller than the resonant frequency, the ZCS turn-off can be achieved. Thus, only C_{oss} induced turn-on loss is considered in the STC switching loss.

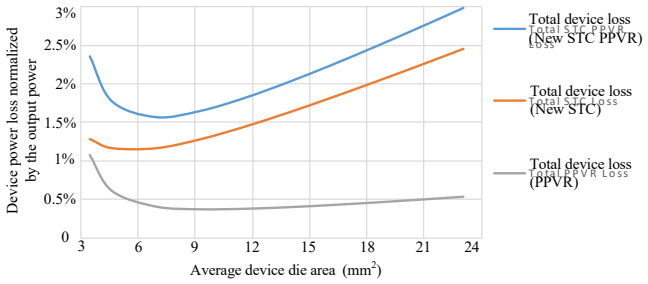
According to the 350V voltage stress of the switches, Rohm 650V SiC dies (S4003) are selected for all the switches in proposed converter. Considering the 1200V switch voltage stress in the boost converter, two in-series Wolfspeed 1200V SiC dies (CPM2-1200-0025B) are used for each of the two switches in boost converter for the comparison. Since the switching loss versus drain current is not included in the datasheet of Rohm SiC die S4003 and Wolfspeed SiC die CPM2-1200-0025B, the relationship between the turn-on, turn-off switching energy and drain current for these two dies is derived from the datasheets of Rohm's 650V SCT3120AL SiC MOSFET and Cree's 1700V C2M0045170P SiC MOSFET, respectively.

As presented in Fig. 5(a), at the same 350V input, 1200V output voltage and 4kW output power, with the same switching frequency 357kHz, the total device power loss of STC PPVR is less than 1/3 of boost converter with the same die area. It can achieve more effective die utilization at the same conduction loss. By further breaking down the total device power loss of each converter, it can be found that they share similar conduction loss. It is the switching loss that contributes largely to the total device power loss. From Fig. 5(b), the PPVR power loss becomes more insignificant as the die area increases. That's because the C_{oss} discharge induced STC device switching loss becomes more dominant as the die area is enlarged.

The *SLI* can also be applied to evaluate the impact of different output power operation, switching frequency, and conversion ratio on the total device power loss to comprehensively compare converter topologies in terms of the optimized device technology.



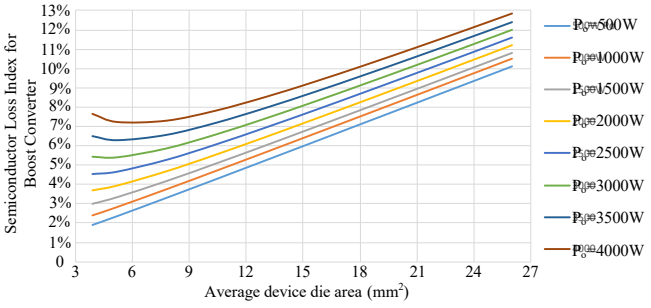
(a) Device power loss versus die area for boost converter & STC PPVR



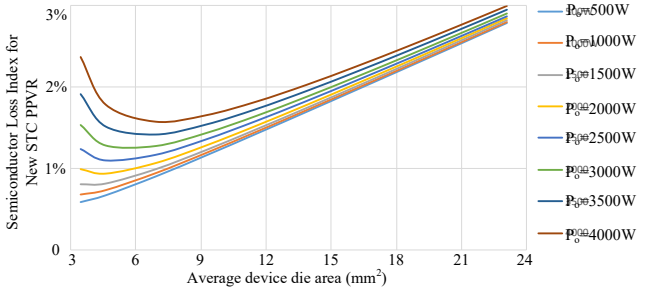
(b) Device power loss versus die area of STC PPVR

Fig. 5. Device power loss versus die area comparison based on 350V/1200V 4kW converter at 357kHz switching frequency

To further investigate the relationship of different output power operation and the die area, the *SLI* is compared between boost converter and proposed STC PPVR. This comparison is based on the 4000W designed output power rating, 350V input voltage rating, and 1200V output voltage rating. The comparison results are shown in Fig. 6 (a) and (b) for the boost converter and STC PPVR, respectively. As the output power increases, the portion of total device power loss among the output power becomes smaller in both the two converters. Compared with boost converter, the proposed one can achieve less total device power loss under both the light-load and heavy-load conditions.



(a) SLI of boost converter with different output power operation



(b) SLI of new STC PPVR with different output power operation

Fig. 6. SLI versus die area with different output power operation (designed power rating 4kW, V_{in}=350V, V_o=1200V, f_s=357kHz).

With different switching frequency, the relationship between total device power loss and semiconductor die area is shown in Fig. 7 for both the boost converter and STC PPVR. Both the two converters can achieve smaller semiconductor power loss as the switching frequency increases. The percentage of the semiconductor power loss among the output power for the boost converter can be decreased to about 2.5% when the switching frequency is reduced to 100kHz. But for the proposed STC PPVR, this percentage can be decreased to smaller than 1% at 100kHz.

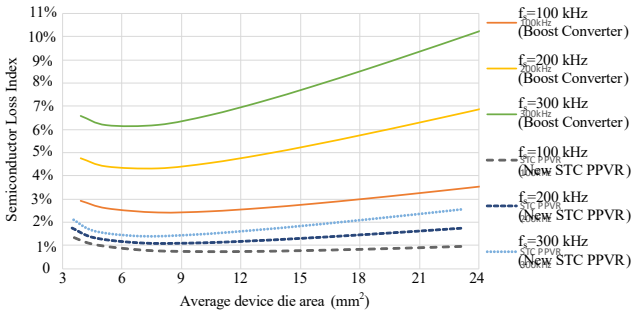


Fig. 7. SLI of boost converter and the new STC PPVR under different switching frequency (P_o=4kW, V_{in}=350V, V_o=1200V).

To evaluate the impact of conversion ratio on the total device power loss, the comparison between boost converter and STC PPVR is made with the 4kW output power, 1200V output voltage, 200V~400V input voltage range as shown in Fig. 8. It is based on the same cutting ratio of the corresponding dies. For boost converter, each switch die has 0.3 times the die area of Wolfspeed 1200V SiC dies (CPM2-1200-0025B). For STC PPVR, each switch die has 0.3 times the die area of the Rohm 650V SiC dies (S4003). As the conversion ratio rises, the device power loss of the boost converter increases linearly. For the STC PPVR, when the conversion ratio changes, the device power loss fluctuates nonlinearly. This is because the number of the working STC modules changes during different conversion ratio ranges. During conversion ratio range 3~4, 4~5 and 5~6, the number of active STC modules is 3, 4, and 5, respectively. The total device conduction loss of STC is unrelated to the conversion ratio because the STC device RMS current $i_{STC\_SW\_RMS}$ is only dependent on the output current according to Eq. (11).

$$i_{STC\_SW\_RMS} = \sqrt{\frac{1}{T_s}\int_0^{\frac{1}{2}T_s}\left(\frac{P_o}{V_o}\cdot\pi\cdot\sin\left(2\pi f_s\cdot t\right)\right)} = \frac{\pi}{2}\cdot I_o \tag{11}$$

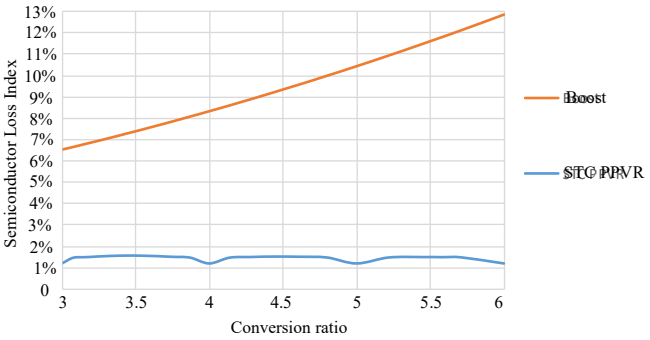


Fig. 8. Device power loss versus total die area with different conversion ratio (designed output power rating P_o=4kW, V_o=1200V).

Besides, the gate charge induced switching loss and C_{oss} related turn-on switching loss do not change with the conversion ratio when the die area is fixed. Thus, the STC switching loss is fixed. Therefore the total device power loss of the STC PPVR is affected only by the buck converter when the conversion ratio changes. Since the buck converter device current RMS changes with the similar trend during each conversion ratio range 3~4, 4~5 and 5~6, the buck converter device conduction loss follows the periodical curve when the conversion range is in each range. As a result, the STC PPVR device power loss versus conversion ratio appears as the blue curve in Fig. 8 presents.

To evaluate the power processed by buck converter under different conversion ratios from 3 to 6, calculation has been made in MATHCAD and the results are shown in Fig. 9. In this evaluation, 4kW output power, 1200V output voltage, 200V~400V input voltage range have been applied. The percentage of the power processed by buck converter reaches to the peak when the duty cycle of the buck converter is close to 0.5. This is because the turn-on and turn-off switching power losses of the buck converter are the highest around 0.5 duty cycle.

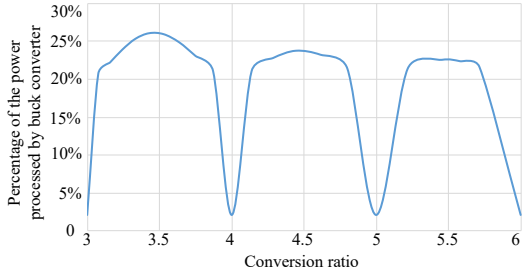


Fig. 9. Percentage of the power processed by buck converter versus conversion ratio

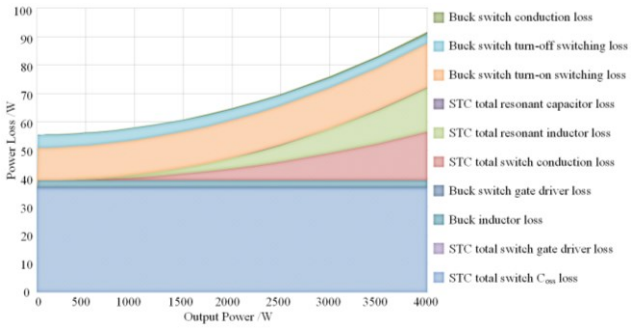
IV. Power Loss Breakdown and Efficiency Estimation

Based on the designed key components listed in Table I, the device, inductor and capacitor RMS currents are calculated. The power loss breakdown analysis and efficiency estimation are further conducted.

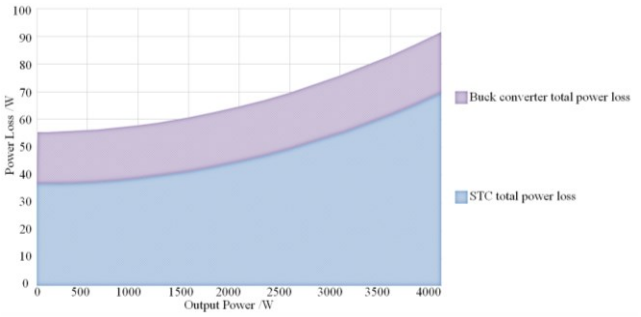
Table I. Key Components of Designed 4-kW 1200-V Output Converter Integrating 1:6 STC Stage and Buck Converter PPVR Stage

Name	Part Number / Company	Parameters
Resonant inductor	XAL1060-152MEB /Coilcraft	1.5 µH, I_{sat} = 36 A
Resonant capacitor	CGA9Q1C0G3A333J280KC /TDK	C0G / 33 nF*4
Clamping capacitor	C5750X6S2W225K250KA /TDK	X6S / 2.2 µF*6
Buck output capacitor		
Buck converter inductor	XAL6060-223MEB /Coilcraft	22 µH*2
Output capacitor	B58031U9254M062 /TDK	250 nF*38
New STC switches	GS66508B /Gan Systems	V_{dss} 650 V, I_d 30 A
Buck switches		
Gate driver of GS66508B	SI8271GB-IS /Silicon Labs	Peak output current 4 A

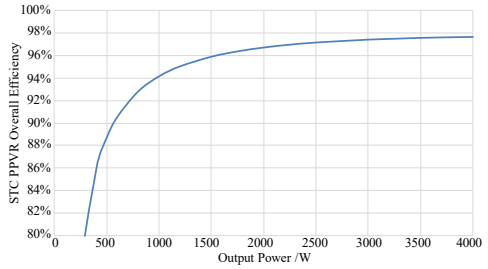
In Fig. 10(a), the STC switch conduction loss, gate driver loss and C_{oss} induced turn-on switching loss are calculated. The resonant inductor loss, ESR (Equivalent Series Resistance) losses of resonant capacitors are included. Besides, the buck converter switch conduction loss, turn-on



(a) Power loss breakdown of the STC PPVR



(b) Power loss comparison of STC and PPVR buck converter



(c) Efficiency estimation of STC PPVR

Fig. 10. Power loss breakdown and efficiency estimation

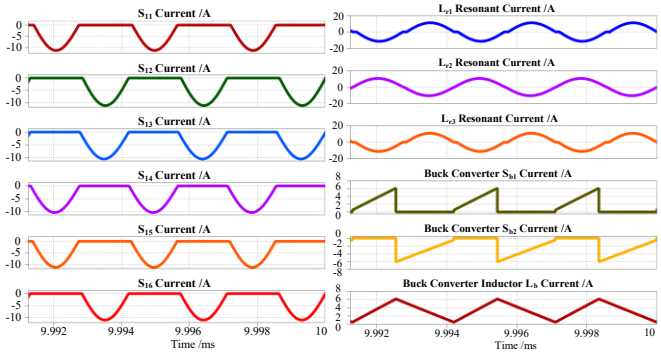
and turn-off switching loss and gate driver loss are calculated. Since the typical switching loss versus drain current is not included in the GS66508B datasheet, the relationship between turn-on, turn-off switching energy and drain current is derived from the datasheet of Rohm's 650V 21A SiC MOSFET SCT3120AL. The AC winding loss and core losses of both the STC resonant inductor and buck converter inductor are analyzed through Coilcraft core and winding loss calculation tool. From Fig. 10(a), the C_{oss} loss contributes the largest portion of the total power loss. In addition, the power loss is further classified into STC and PPVR buck converter in Fig. 10(b). The buck converter power loss is smaller than 1/3 the power loss of the STC at the full load. Based on the power loss analysis, the overall efficiency is estimated in Fig. 10(c). The peak efficiency is around 97.71% at full load.

V. Simulation Results

To verify the function of the designed 350V/1200V 4-kW STC PPVR converter, the simulation is carried out in PLECS. A boost converter with the same input, output voltage and output power is also simulated for comparison. To achieve 1200-V output voltage from 350-V input voltage, the boost converter duty cycle is set as 0.70833. In the proposed STC PPVR converter, the duty cycle of buck converter is 0.4286. Three new STC cells are considered to generate 1:4 conversion ratio in the unregulated stage. The inductor in the buck converter is 44μH to make it work in continuous conduction mode. In Fig. 2, S_{17}~S_{20} are always ON. S_7~S_{10} are always OFF. Based on the resonant inductance 1.5μH and resonant capacitance 132nF, the resonant frequency f_r can be calculated as Eq. (12) shows.

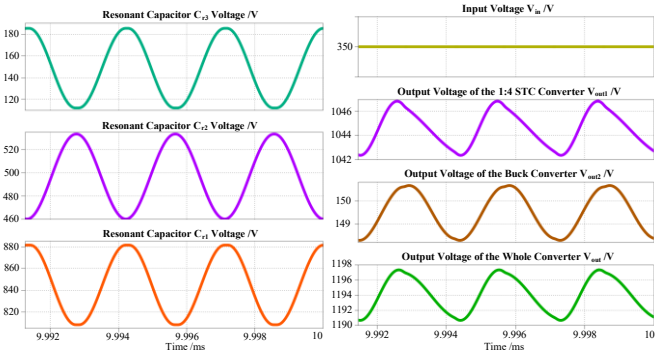
$$f_r = 1/\left(2\pi\sqrt{L_r C_r}\right) = 1/\left(2\pi\sqrt{1.5\mu H \cdot 132nF}\right) = 357.674kHz \quad (12)$$

The switching frequency is fine-tuned as 353.77kHz, which is slightly smaller than the resonant frequency. Fig. 11(a) shows the simulated current waveforms of the switches in new STC. Fig. 11(b) shows the resonant current waveforms, the buck converter switch current and inductor current waveforms. Fig. 11(c) shows the resonant capacitor output voltage waveforms. Fig. 11(d) shows the input voltage, STC output voltage, buck converter output voltage and the whole converter output voltage waveforms.



(a) New STC switch current

(b) Resonant current, buck converter switch current and inductor current



(c) Resonant capacitor voltage

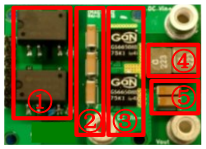
(d) Input, output voltage, buck converter output voltage waveforms

Fig. 11. Simulation results of 350V/1200V 4kW STC PPVR

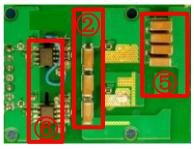
VI. Prototype Design and Experiment Results

The new STC and the PPVR buck converter are designed as two separate boards. In Fig. 12(a) and Fig. 12(b), the two sides of the buck converter are presented. The components highlighted with circled numbers are: ① Gate driver power supplies, ② Buck converter input capacitors, ③ Buck converter switches, ④ Buck converter inductor, ⑤ Buck converter output capacitors, ⑥ Gate drivers.

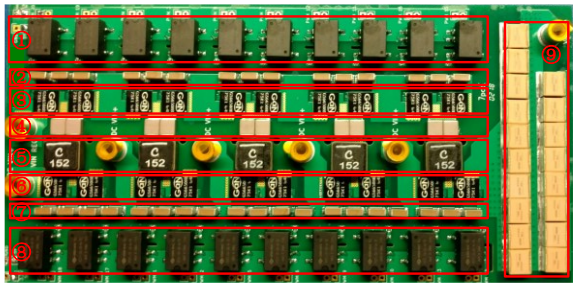
Fig. 12(c) and Fig. 12(d) show the two sides of the designed 1:6 new STC. The highlighted parts are: ① Wing-side switch gate driver power supplies, ② Clamping capacitors, ③ Wing-side switches, ④ Resonant capacitors, ⑤ Resonant inductors, ⑥ STC switches closer to , ⑦ Input capacitors, ⑧ Gate driver power supplies for STC switches



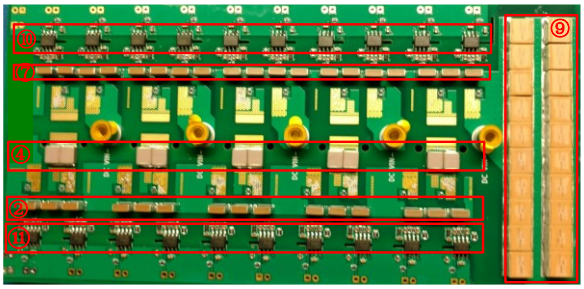
(a) Front view of buck converter



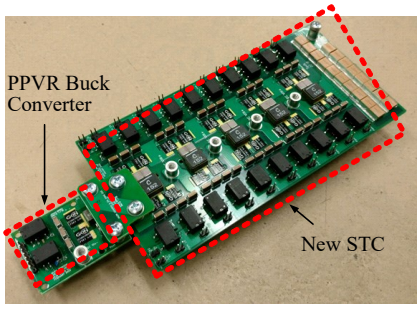
(b)Back view of buck converter



(c) Front view of 1:6 new STC



(d) Back view of 1:6 new STC



(e) New STC assembled with PPVR buck converter

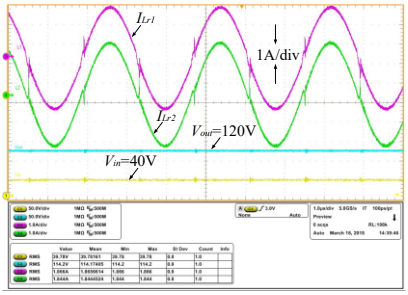
Fig. 12. Designed prototype consisting of a 1:6 conversion ratio new STC and a PPVR buck converter

closer to input voltage ⑨ Output capacitors ⑩ Gate drivers for STC switches closer to input voltage ⑪ Gate drivers for STC switches closer to output voltage. Fig. 12(e) shows the whole assembled converter integrating the new STC and PPVR buck converter.

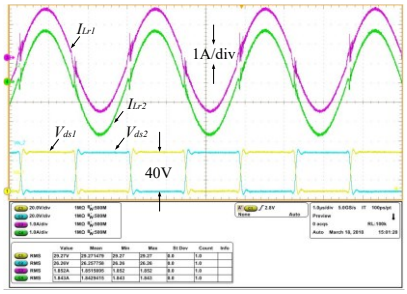
Preliminary light-load test results of two STC modules are presented in Fig. 13(a) and Fig. 13(b) to verify the validity of this topology. The input voltage is 40V. Output voltage is 120V. The 183Ω load resistance is applied, which means the output power is 78.7W. From input and output voltage waveforms in Fig. 13(a), voltage conversion ratio is verified. The resonant current in the two modules I_{Lr1} and I_{Lr2} are shown to match the corresponding simulation results. The device drain-source voltage clamping has been verified from the V_{ds1}, V_{ds2} waveforms in Fig. 13(b).

VII. Conclusion

In summary, this paper proposes a new STC with PPVR for the step-up DC/DC converters with continuously adjustable conversion ratio. A new index, i.e. Semiconductor Loss Index (*SLI*) which reflects the relationship between



(a) Tested input & output voltage, resonant current of 1:3 new STC



(b) Tested V_{ds} and resonant current of 1:3 new STC

Fig. 13. Light-load 1:3 conversion ratio new STC test results

device power loss and total die area is introduced. It can comprehensively reflect the impact of each switch die area, different operated output power, switching frequency, and conversion ratio on the total device power loss, which helps evaluate different power topologies in terms of device technologies. The proposed converter achieves better die size utilization compared with boost converter under the same device power loss. In other words, the proposed converter realizes smaller device power loss compared with boost converter when the semiconductor die area is the same. The modularized design and soft-switching operation make it possible to achieve high power density and high efficiency. Analysis has shown the overall full-load efficiency of designed 4-kW converter is 97.71%. A 4-kW prototype integrating a 1:6 STC and a PPVR buck converter stage has been built to verify the theoretical analysis. Simulation and preliminary test results have verified the validity of the proposed topology. Further experiment results of full-load 4-kW converter, including the power loss and efficiency measurement will be presented in the future publications.

Acknowledgment

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