A 100kW Switched-Tank Converter for Electric Vehicle Application

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***Abstract*—This paper presents a 100kW one-cell switched-tank converter (STC) for electric vehicle (EV) application. A new evaluation method that evaluates different converter topologies has been proposed in this paper to show the advantages of the STC over the boost converter and 3-level flying capacitor multilevel (FCML) converter. Both non-interleaved (1-phase) and interleaved (2-phase and 3-phase) operation of the STC have been analyzed. The analytical study shows that it is difficult to achieve the optimum design of the passive components such as input and output capacitors in 1-phase converter because of the high RMS current flowing through them. This means the passive components need to be over-designed in order to meet the current stress requirement. For instance, the designed capacitance of input capacitor is several times of the required value, which leads to bulky capacitor size. Therefore, this paper evaluates the potentials of using 2-phase and 3-phase interleaved operation to address this issue. Two operation modes, zero-voltage switching (ZVS) mode and zero-current switching (ZCS) mode, are evaluated to show the ZCS operation mode is more suitable for the presented converter with interleaved operation. By using the interleaving concept, the predicted 100kW 3-phase interleaved converter can achieve 60% size reduction based on the 1-phase converter design. And the predicted power density of the 3-phase interleaved STC can achieve 115kW/L power density. Simulation results are provided to validate the theoretical analysis. Both 1-phase and 3-phase 100kW prototypes under developing are shown in this paper.**

Keywords— resonant, switched-tank, DC-DC, electric vehicle, ZCS, ZVS, SiC

I. INTRODUCTION

As the growth of environmental awareness among the world, direct vehicle emissions of conventional vehicles are recognized to be harmful to human health and the major source of greenhouse gases. Battery electric vehicles start drawing more and more attention because they have zero direct vehicle emissions. And they could be the key solution to help improve the environment of the world. With the development of SiC technology, SiC devices are widely used in power electronics area, such as inverters[1]–[3], Also, how the leveraging the advantages of SiC devices in electric vehicle powertrain applications become hot topics in recent years[4]–[6].

As shown in Fig. 1, the electric vehicle powertrain includes on-board charger, battery system, bi-directional dc-dc converter and motor drive system. The nominal battery voltage is usually around 300V, and the DC bus of the inverter is around 600~800V [7]. Thus, the bi-directional DC-DC converter will need to boost the battery voltage up to two times higher and feed to the motor drive system. In [8], a boost converter is optimized to achieve high power density and high efficiency. The volume of the converter is 9.15 liter and it achieves 6kW/L power density. In [9] and [10], a composite boost converter has been presented, it achieves lower loss than conventional boost converter. The predicted volume of the 39kW converter is 1.8 liter. In [11], a three-phase interleaved boost converter shows that interleaved topology can greatly reduce the volume of the converter. In [12], a 100kW boost converter with coupled inductor are presented. The converter achieves 27.9kW/L power density and 98% efficiency.

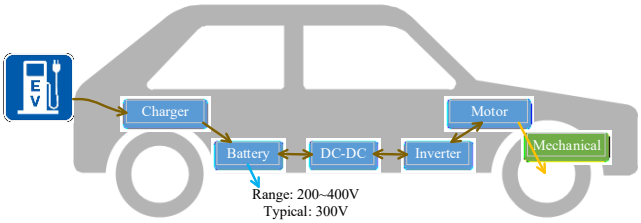


Fig. 1 Powertrain of an electric vehicle

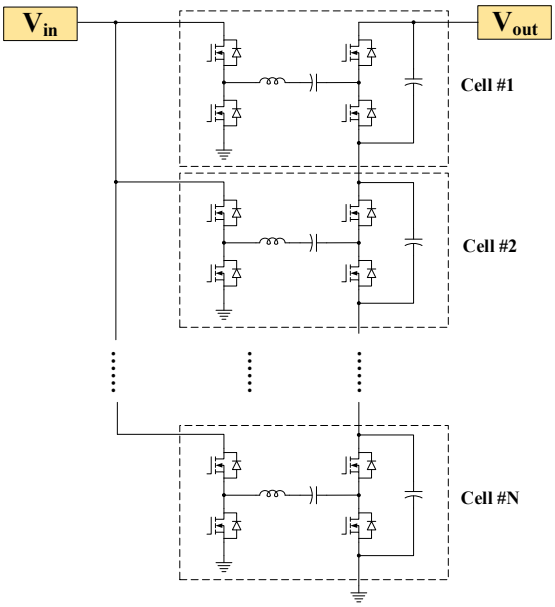
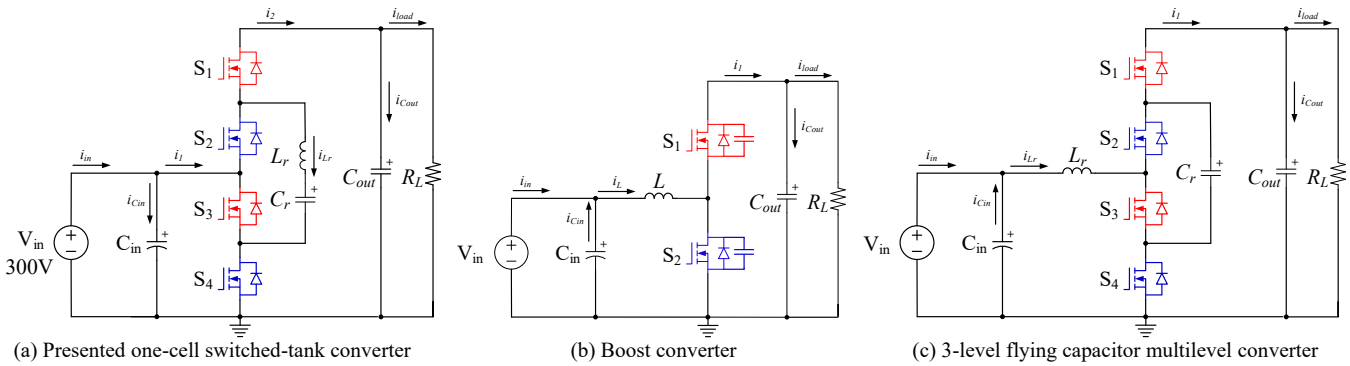


Fig. 2 Generalized circuit structure of the new STC

This paper proposed a new evaluation method that evaluates different converter topologies show the advantages of the



(a) Presented one-cell switched-tank converter (b) Boost converter (c) 3-level flying capacitor multilevel converter

Fig. 3 Circuit configuration of the compared dc-dc converters

presented one-cell STC over the boost converter and 3-level flying capacitor multilevel (FCML) converter. This paper also evaluates the potential converter size reduction by using interleaving concept. Compared with the state-of-art solution that still uses conventional boost converter in the circuit (22kW/L) [10], this paper presents a 1-phase STC that can achieve higher density (45kW/L) with an estimated total volume of 2.2 liters in the second section. However, although the 1-phase converter achieves very high density, the size of passive components (e.g. input and output capacitors) is not optimized because of the high RMS current flowing through them. As a result, interleaved topology has been evaluated to reduce the size of passive components. Both ZVS operation mode and ZCS operation mode are studied in this paper, which shows the ZCS operation mode is more suitable for the interleaved operation. With 3-phase interleaved operation, the estimated converter size reduction can be as high as 60%. Simulation results are provided to show that the RMS current of the passive components has been significantly reduced with 3-phase interleaved operation. At last, a 100kW 1-phase prototype and a 3-phase prototype are demonstrated for size comparison purpose.

II. CIRCUIT CONFIGURATION AND ANALYSIS

A. Circuit Configuration and Topology Evaluation

Fig. 2 shows the generalized circuit configuration of the new switched-tank converter. This structure is highly modular and scalable. Fig. 3(a) shows the circuit configuration of the presented one-cell STC. This converter has two operation modes, which are ZCS mode and ZVS mode. Under ZCS operation mode, the conversion ratio of the converter is fixed, which is 2 to 1. Under ZVS operation mode, the output of the converter can be regulated. However, because the converter achieves the highest efficiency when its conversion ratio is 2 to 1 and the DC bus voltage of the inverter does not need to be regulated to a specific value in the existing electric vehicles [13], voltage regulation is not within the scope of this paper.

First, three different converter topologies are compared, which are the one-cell switched-tank converter, 3-level FCML converter and boost converter, as shown in Fig. 3. In this comparison, we assume the boost converter is operating at continues conduction mode (CCM) and the inductor current ripple is 30% of its average current value. So, semiconductor switching loss of the boost converter cannot be ignored in this topology evaluation part. Also, we assume the 3-level FCML converter and STC operating at ZCS mode. Thus, the semiconductor loss of this two converters is the same.

In order to ensure the fairness of the comparison, semiconductor loss index (SLI) is introduced to evaluate the utilization level of semiconductor devices in all the circuits, which is represented by $P_{loss\_norm}(A_{die})$. The semiconductor loss index $P_{loss\_norm}(A_{die})$ can be calculated by using (1). Note that the $P_{cond}(A_{die})$, $P_{gate}(A_{die})$ and $P_{switching}(A_{die})$ means the total semiconductor conduction loss, total gate drive loss and total switching loss of the converter when the total semiconductor die area usage is A_{die} in a converter. They can be calculated by using equation (2), (3) and (4). In the ZCS case, the total switching loss can be simplified as MOSFET output capacitor loss, as shown in (5). The $P_{converter}$ is the power rating to the converter. According to (1), we can tell that if the total semiconductor die area usage of two converters are the same, then the converter that has lower semiconductor loss index value is more efficient than the other one. In summary, the converter with lower semiconductor loss index can better utilize the switching devices.

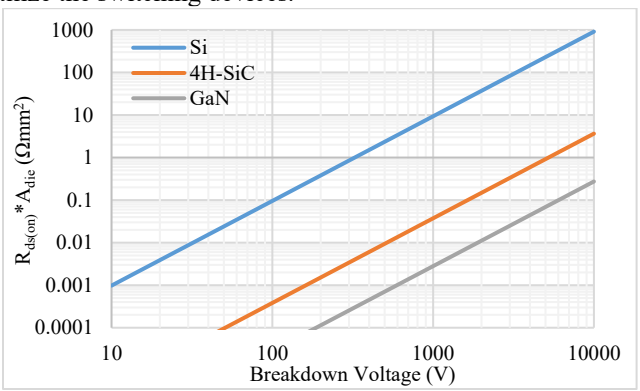


Fig. 4 Theoretical on-resistance and blocking voltage relationship for silicon, silicon-carbide, and gallium nitride devices [20]–[23]

Table I Die Information Used In the Comparison

Part#	Company	Voltage Rating	Current Rating
S4003	Rohm	650 V	118 A
S4103	Rohm	1200 V	95 A
CPM3-0900-0010A	Wolfspeed	900 V	196 A
CPM2-1200-0025B	Wolfspeed	1200 V	98 A

$$P_{loss\_norm}(A_{die}) = \frac{P_{cond}(A_{die})+P_{gate}(A_{die})+P_{switching}(A_{die})}{P_{converter}} \quad (1)$$

$$P_{cond}(A_{die}) = \sum_i I_{rms_i}^2 \frac{\alpha_i(\xi_i V_{B_i})}{k_i A_{die}} \quad (\alpha_i(\xi_i, V_{B_i}) = R_{ds(on)} A_{die}(V_{B_i})) \quad (2)$$

$$P_{gate}(A_{die}) = \sum_i V_{gs_i} f_{s_i} \beta_i k_i A_{die} \quad (\beta_i = \frac{Q_{g_i}}{A_{die}}) \quad (3)$$

$$P_{switching}(A_{die}) = \sum_i [E_{on_i}(A_{die}) + E_{off_i}(A_{die})] f_{s_i} \quad (4)$$

$$P_{switching\_zcs}(A_{die}) = \sum_i V_{ds_i}^2 f_{s_i} \gamma_i k_i A_{die} \quad (\gamma = \frac{C_{oss_i}}{A_{die}}) \quad (5)$$

According to Fig. 4, with the same semiconductor technology, the value of $R_{ds(on)}$*A_{die} is a fixed number when the breakdown voltage V_B is fixed. This means for a certain semiconductor technology, the $\alpha_i(\xi_i, V_{B_i})$ is a fixed value when V_{B_i} is determined. The ξ_i in (2) represents the coefficient of the semiconductor technology of the i^{th} device. In addition, we also assume the parameters β_i and γ_i shown in (3) and (5) are constant values. This means when we increase the total die area A_{die} by N times, the Q_g and C_{oss} will also be N times larger and the $R_{ds(on)}$ will reduce by N times, which is the same as connecting N dies in parallel. The parameter k_i means the ratio of the i^{th} die's area over the total die area A_{die} since there are multiple switches been used in a converter, and $\sum_i k_i = 1$. By tuning the parameter k_i, the switch conduction loss of a converter can be optimized. It's worth mentioning that the semiconductor loss index values are the same for 3-level FCML converter and STC.

For converter with 300V input and 600V output, 1200V dies from both Rohm and Wolfspeed are used in the boost converter evaluation. And we assume the die area of the upper switch and the lower switch in the boost converter are the same, which means k_i=0.5. On the other hand, 900V die from Wolfspeed and 650V die from Rohm are used in the STC and 3-level FCML converter. Table I shows the SiC die information used for the evaluation. Fig. 5 shows that the power loss of switching devices in STC and 3-level FCML converter is less than 50% the total semiconductor loss of the boost converter under full load. This is because the switching loss is a major contributor to the total semiconductor power loss in boost converter. Note that although the 3-level FCML converter and STC have the same semiconductor loss index, the mechanical layout of 3-level FCML converter is more challenging since its inductor, input and output capacitors are on the dc side.

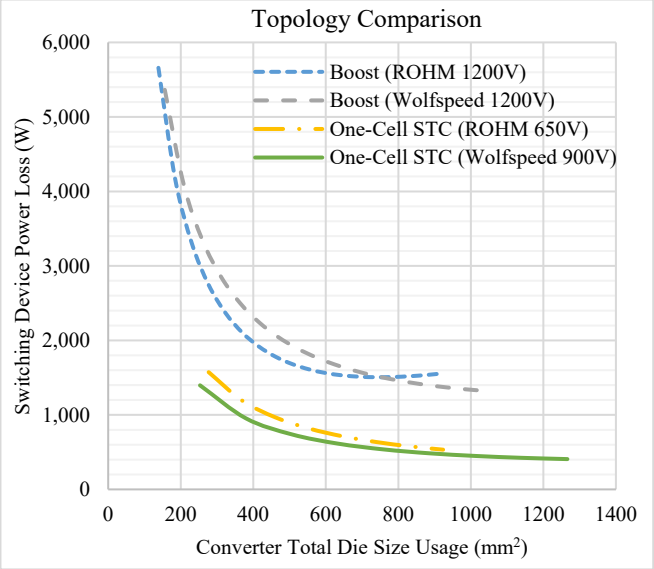


Fig. 5 Topology comparison (300V input and 600V output, 100kW)

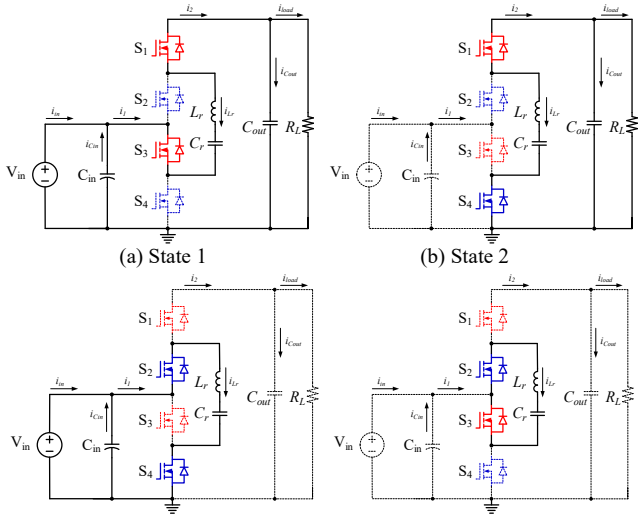


Fig. 6 Four switching states of the presented converter

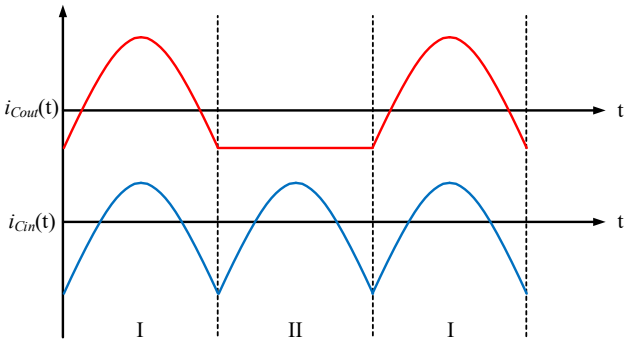


Fig. 7 Current waveforms of ZCS operation

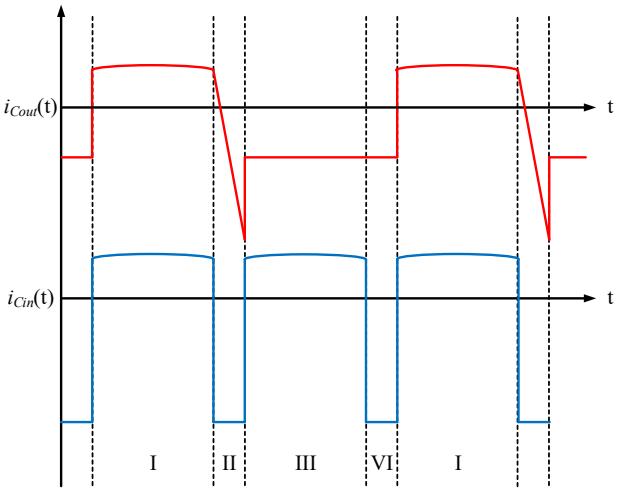


Fig. 8 Current waveforms of ZVS operation

B. *Design of Passive Components in 1-Phase Converter*

Since the topology evaluation shows that the STC is a better choice than the other two converters, the next step is to figure out the potential improvement that can be done to reduce the passive component size of the one-cell STC, especially the input and output capacitors. Therefore, the current flowing through input and output capacitors should be analyzed. In order to analyze the current waveforms of passive components in the circuit, some assumptions have been made to simplify the analysis procedure. First, the voltage ripple across the input capacitor, output capacitor and resonant capacitor is small enough. Second, all the switching devices are ideal. It is worth mentioning that the mechanisms to achieve ZCS and ZVS operation of the presented converter will not be included in this paper since they have been analyzed in previous works [14]–[18]. This paper only focuses on obtaining the current waveforms of different passive component under different operation modes. In Fig. 6, state 1 and 3 shows the operation states of ZCS mode, while state 1 to 4 shows 4 operation states of ZVS mode. The waveforms of current flow through the passive components in both modes can be found in Fig. 7 and Fig. 8, respectively.

In order to study the actual size reduction that can be achieved by using interleaved topology. A 1-phase 100kW converter is developed at first. Table II shows the specifications of the designed 1-phase converter. The operating frequency of the designed converter is 100kHz. Table III shows the input and output capacitors that are used in the prototype. The capacitance of each input and output capacitor are 12uF and 5uF, respectively. According to Table IV, when we assume the voltage ripple of both input and output of the converter is less than 5%, then the minimum capacitance values of the input and output capacitor banks are 30uF and 40uF. On the other hand, the root mean square (RMS) values of the current flowing through input and output capacitors are 165A and 205.5A. As a result, in order to make sure the capacitor banks have enough current capability, the actual designed capacitance values of the input and output capacitors in the circuit are 120uF and 70uF, respectively. This means the capacitance in the circuit is over-designed. Therefore, the size of input and output capacitors are not optimized. A component volume breakdown shows that the input capacitor and output capacitor take more than 30% of the total component size, as shown in Fig. 9.

Table II Parameters of the Analyzed 1-Phase 100kW Converter

	Symbols	Values
Power Rating	P_{out}	100 kW
Input Voltage	V_{in}	300 V
Output Voltage	V_{out}	600 V
Resonant Capacitance	C_r	7.2 uF
Resonant Inductance	L_r	350 nH
Switching Frequency	f_s	100 kHz
Input Capacitor	C_{in}	120 uF
Output Capacitor	C_{out}	70 uF

Table III Capacitors Used In The 1-Phase Prototype

	Part#	Capacitance
Input Capacitor	B32674D3126	12uF
Output Capacitor	B32674D6505	5uF

Table IV Capacitance and Current Capability Requirements of Input and Output Capacitors (Assume Voltage Ripple <5%)

	Current Capability Requirement	Capacitance Requirement
Input Capacitor	165 A	30 uF
Output Capacitor	205.5 A	40 uF

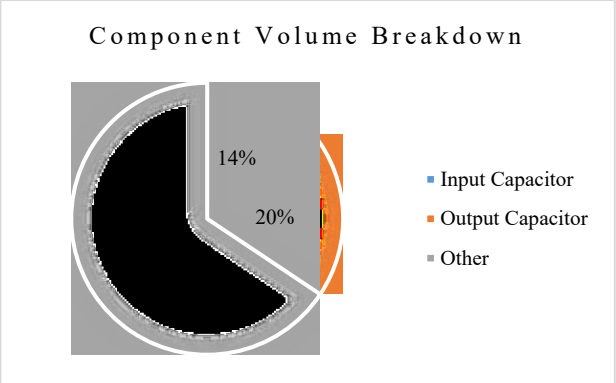


Fig. 9 Capacitors take 34% of the total component volume

III. Interleaved Topology and Comparison

Interleaved concept provides a good solution to make use of the passive components in a more rational manner. In order to have a reasonable comparison between 1-phase converter, 2-phase interleaved converter and 3-phase interleaved converter, the values of resonant inductance and resonant capacitance frequency are always kept the same. This means switching frequency is always the same in the following analysis.

A. *Current Stress of Passive Components*

In the interleaved operation, the control signals of the converter in different phases shift 180-degree and 120-degree from each other in 2-phase interleaved connection and 3-phase interleaved connection, respectively. Fig. 10 shows the 3-Phase interleaved circuit connection of the presented circuit. Fig. 11 shows the normalized capacitor RMS current when the converter operates at ZCS mode. Similarly, Fig. 12 shows the

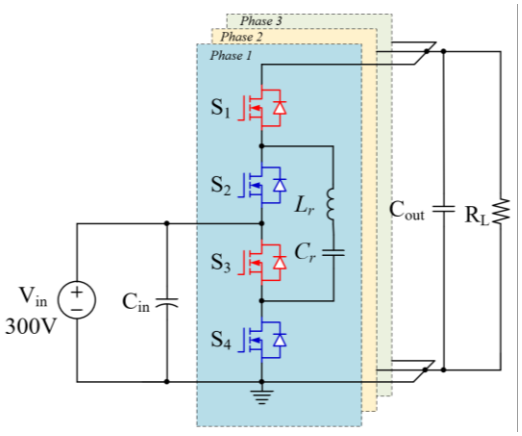
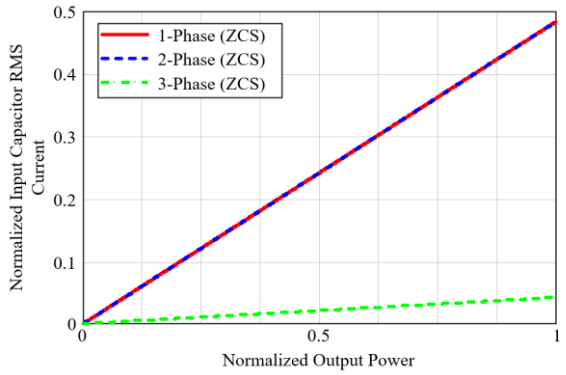
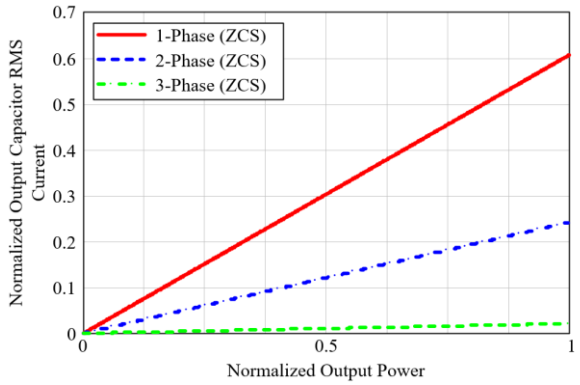


Fig. 10 3-Phase interleaved connection of the presented converter

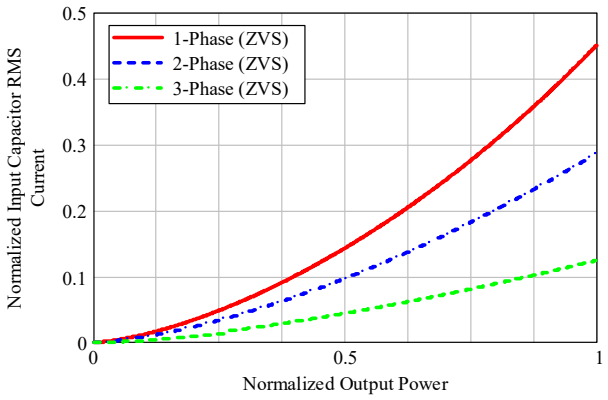


(a) Input capacitor RMS current

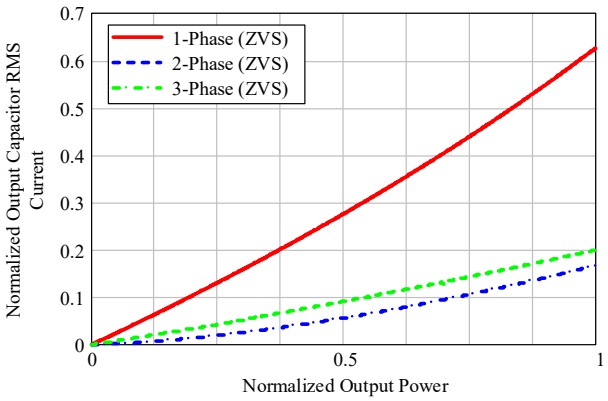


(b) Output capacitor RMS current

Fig. 11 Normalized current stress of capacitors (ZCS operation)



(a) Input capacitor RMS current



(b) Output capacitor RMS current

Fig. 12 Normalized current stress of capacitors (ZVS operation)

normalized current stress of the input and output capacitors when the converter operates at ZVS operation mode. According to these two figures, we can tell that the RMS values of the currents flowing through input capacitor bank and output capacitor bank are significantly reduced with the interleaved operation. Especially when the converter operates at ZCS mode, the current stress of the input and output capacitors can be reduced by more than ten times. This means the size of the input capacitor and the output capacitor can be significantly reduced with interleaved operation.

B. Estimated Component Size and Inductor Size Reduction

The inductance of the resonant inductor can be calculated using (6). And the relationship between the saturation current and the saturation flux density can be found in (8). Based on (8), the saturation current of a inductor can be represented by the mean length of the magnetic path l_m, length of the air gap l_g, inductor turn number N, permeability μ_0, relative permeability μ and the saturation flux density, as shown in (8). Thus, (9) has been derived from (6) and (8). According to (9), resonant inductance value and saturation current value of an inductor are proportional to the core's cross-section area and magnetic path length. In our case, the peak current of the inductors will become 1/N times in an interleaved N-phase converter, this means that the size of magnetic component size can also be significantly reduced in interleaved structure (e.g. ~9 times in a 3-phase converter). It's worth mentioning that a similar inductor volume reduction analysis is also proposed in [19]. At last, an estimated component size reduction of 64.5% can be achieved by using 3-phase interleaved operation, as shown in Fig. 13.

$$L = \frac{N^2 A_c}{\frac{l_g}{\mu_0} + \frac{l_m}{\mu * \mu_0}} \tag{6}$$

$$H = N * I_{sat} = (\frac{l_g}{\mu_0} + \frac{l_m}{\mu * \mu_0}) B_{sat} \tag{7}$$

$$I_{sat} = \frac{(\frac{l_g}{\mu_0} + \frac{l_m}{\mu * \mu_0}) B_{sat}}{N} \tag{8}$$

$$L I_{sat}^2 = B_{sat}^2 A_c (\frac{l_g}{\mu_0} + \frac{l_m}{\mu * \mu_0}) \tag{9}$$

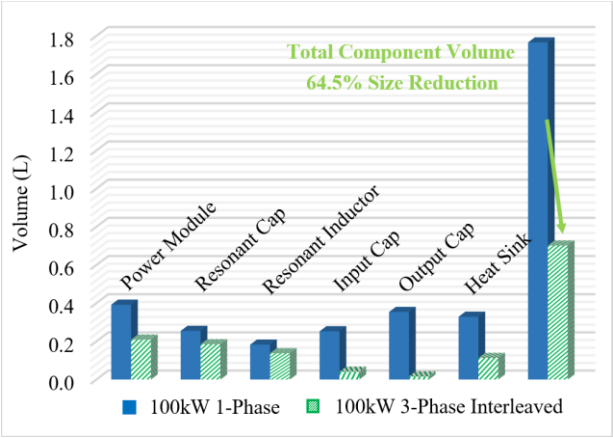
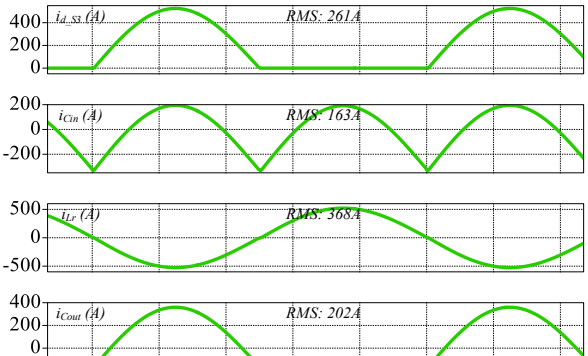


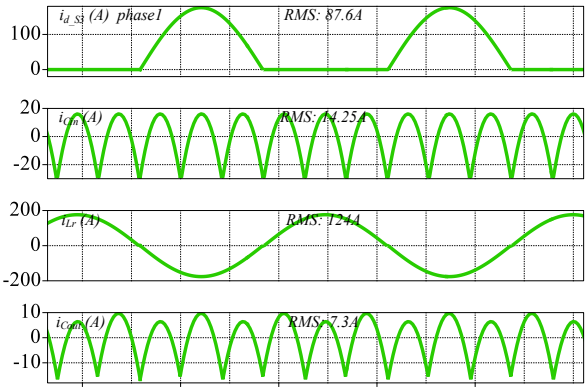
Fig. 13 64.5% component size reduction can be achieved by using 3-phase interleaved topology

IV. SIMULATION RESULTS AND PROTOTYPE

Simulation has been performed to validate the theoretical analysis on the current stress of passive components in the circuit. In ZCS mode, the 3-phase interleaved operation allows the current stress of input capacitor drop from 163A to 14.25A, which is 11.5 times lower. And the current stress of output capacitor is reduced by 28 times, from 202A to 7.3A, as shown in Fig. 14. On the other hand, according to Fig. 15, the current stress of input capacitor is 4.7 times lower in the 3-phase interleaved converter when it operates at ZVS mode, which is 25.4A. In comparison, the current stress of input capacitor in 1-phase converter is 120.6A. In addition, the current stress values of output capacitors in 1-phase converter and 3-phase interleaved converter are 191.5A and 38.4A, respectively. We can tell that the current stress of output capacitors is reduced by five times with the interleaved operation. The simulated current stress values of input and output capacitors match the theoretical analysis. And according to the simulation, one can tell that the interleaved operation can better mitigate the high current stress issue on input and output capacitors when ZCS operation mode is enabled, which also suggest that the ZCS operation is more suitable for interleaved operation. A 1-phase 100kW converter prototype based on Rohm SiC power module BSM600D12P3G001 is designed to verify the theoretical analysis of the capacitor current, as shown in Fig. 16. The 1-phase converter achieves 45kW/L density. Furthermore, a 3-phase high power density converter based on Infineon CoolSiC FF11MR12W1M1_B11 is proposed. Both single side cooling and double side cooling method are considered. With the double side cooling layout, the 3-phase converter achieves 115kW/L power density. Compared with the 1-phase converter, the converter volume reduction is 60%. The magnetic material used to build the inductor is Hitachi ML29D, which is very suitable for the applications range from 50kHz~250kHz.

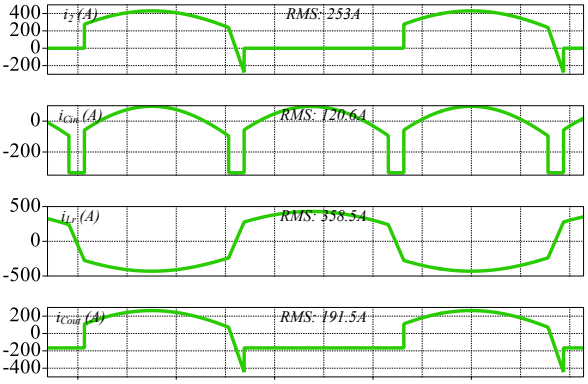


(a) Current waveforms of 1-Phase converter

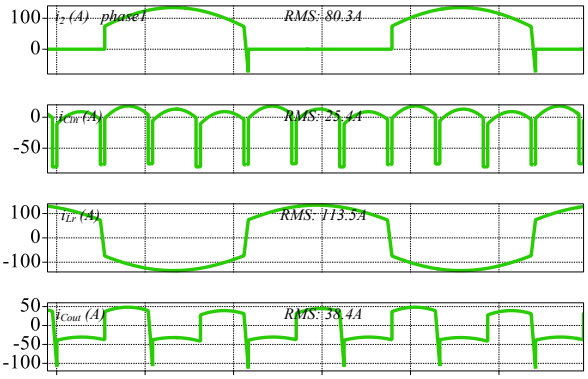


(b) Current waveforms of 3-Phase converter

Fig. 14 Simulation for 100kW with 300V input/600V output (ZCS operation)



(a) Current waveforms of 1-Phase converter



(b) Current waveforms of 3-Phase converter

Fig. 15 Simulation for 100kW with 300V input/600V output (ZVS operation)

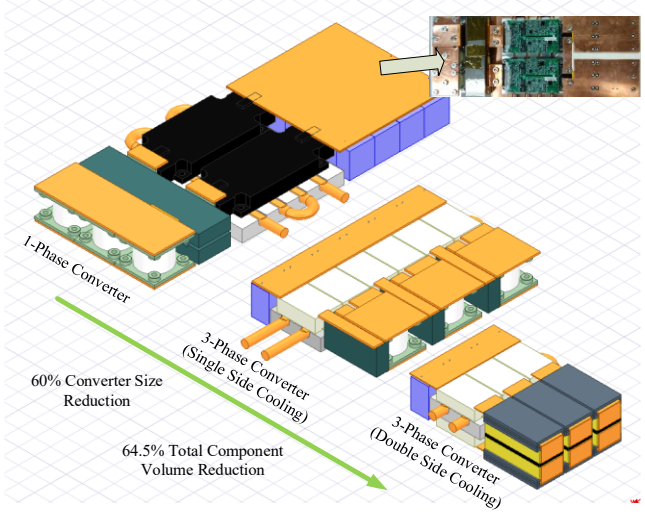


Fig. 16 100kW 1-phase converter and 3-phase converter under developing

V. CONCLUSION AND FUTURE WORK

This paper proposed a new topology evaluation method to evaluate different converter topologies. The study shows that

the presented one-cell switched tank converter has the advantage of lower semiconductor index value and lower mechanical layout difficulty over the conventional boost converter and the 3-level FCML converter. Furthermore, this work evaluates the potential of utilizing interleaving concept to optimize the volume of passive components, thus to achieve size reduction of the 100kW one-cell STC that can be used in electric vehicles. With the interleaved operation, the capacitor over-design issue led by high current stress can be alleviated. The volume of the input capacitor, output capacitor can be reduced by 6 times and 17 times, respectively. An estimated 60% size reduction based on 1-phase converter and a density of 115kW/L can be achieved on a 3-phase one-cell STC with interleaved operation.

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