

# Silicon Photonic Circuit Design Using Rapid Prototyping Foundry Process Design Kits

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(Invited Paper)

**Abstract**—A successful design, fabrication and test of silicon photonic circuits requires design tools, process design kits (PDKs), foundries for fabrication, and test facilities. This paper describes the complete design flow of photonic circuits using rapid-prototyping multi-project wafer (MPW) foundry processes available in the SiEPIC program. The focus of this paper is on rapid prototyping based on electron beam lithography as an alternative and complementary to what is available via deep-UV lithography-based foundries. We describe in detail the PDK and the use of open-source and commercial tools for the design of optical filters, sensors, neuromorphic photonic processors, and optical switches, and discuss test and packaging approaches for these designs. We demonstrate that a “germanium-less” process can be used to build small systems featuring photoconductive detectors, electronics, and phase shifters.

**Index Terms**—silicon photonics, foundries.

## I. INTRODUCTION

Silicon photonics is a technology which allows for the dramatic miniaturization of optical and photonics components

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Manuscript received December 15, 2018; revised January 2019.

ments on an integrated platform, and is based on CMOS electronics manufacturing [1]. Silicon photonics is an enabling technology for application areas including optical data communications (long distance telecommunications and data-centre optical interconnects), biomedical sensing and diagnostics, spectroscopy, structural monitoring, quantum information processing and quantum computing, neuromorphic photonic processing, microwave photonics, and LIDAR (optical radar for automotive applications) [2]–[11]. During the last decade, there has been an explosion of research interest in this technology and there are now numerous companies that have commercialized silicon photonics products, and many others engaged in development.

Silicon photonics is an attractive technology for manufacturing photonic integrated circuits, and several reasons are typically stated. First, silicon photonics offers the possibility of low-cost fabrication. The manufacture of silicon photonic chips is performed by several state-of-the-art foundries – facilities which typically cost billions of dollars. Fabricating photonic integrated circuits (PICs) is correspondingly expensive (\$100k to \$1M per run), thus multi-project wafer (MPW) runs are coordinated where a group of users share the cost of a fabrication run. The costs are reduced significantly for medium to high volume manufacturing, e.g., for 10,000 chips (25 mm<sup>2</sup>), the cost reduces to approximately \$1 per mm<sup>2</sup> [12]. Second, the manufacturing is done using CMOS compatible processes, therefore monolithic integration of electronics and photonics is possible.

The list of foundries that offer low-volume or high-volume manufacturing is growing every year. A non-exhaustive list includes imec, CEA-Leti, AMF (formerly known as IME A\*STAR), VTT, IHP, CompoundTek, AIM Photonics, Sandia Labs, TowerJazz, GlobalFoundries, and STMicroelectronics. MPW aggregation services are provided by such entities as ePIXfab, CMC Microsystems, MOSIS, and CMP. A detailed description of foundries and processes that are openly available is provided in a recent review article [12]. Foundries offer an impressive list of fabrication modules including capabilities for optical input/output (surface gratings or edge couplers), passive components and circuits for filtering and splitting light, various high-speed modulators and low-speed phase

shifters, and high-speed detectors. These fabrication processes are stable and repeatable, meaning the designers can count on the same fabrication process being available in the future. Such fabrication also requires numerous mask layers, typically twenty or more, to implement the above list of functionality.

The challenge for researchers and companies interested in developing new products is that the turnaround times from the international foundries are typically very long, access to leading-edge processes is not readily available (e.g., sub-100 nm feature sizes), the fabrication processes are fixed, and customization is very expensive especially if it precludes shared MPW runs. Although state of the art facilities can operate at  $< 2$  days per mask layer (i.e., 2 months for a typical 20 mask layer process), this is typically achieved for high volume, mature, processes. Research activities, supported via multi-project wafer (MPW) fabrication, run at a lower priority (where resources are limited), and often include less mature fabrication processes, therefore the turnaround times can range from 3 to 12 months.

In response to these needs, the SiEPIC program (a Canadian NSERC-funded research training program in Canada, “Silicon Electronic Photonic Integrated Circuits”) started offering scheduled multi-project wafer (MPW) rapid prototyping fabrication using electron beam lithography (EBL), with fabrication provided by Washington Nanofabrication Facility (WNF) at the University of Washington in the United States, starting in 2014 (the fabrication process has been publicly available since 2011 [13]), and with Applied Nanotools (ANT) in Canada [14], starting in 2015. In both cases chips are fabricated and delivered typically within 2 weeks. Lithography is performed using a direct-write, low-throughput, serial process, using an electron beam, where the write time is proportional to the area to be written, e.g.,  $1 \times 1 \text{ cm}^2$  chip takes 1 to 10 hours to expose, which is acceptable for small quantities but becomes a bottleneck for multi-wafer fabrication. A comparison of EBL-based rapid prototyping versus CMOS DUV pilot line processes is provided in Table I. We have witnessed a significant growth in the need for rapid prototyping during our scheduled bi-monthly EBL fabrication runs. In addition to the WNF and ANT facilities, there are now additional facilities aimed at offering rapid-prototyping and/or customization of silicon photonics, including SiPhotonIC in Denmark [15], Cornerstone in the UK [16], and AMO in Germany [17].

These rapid fabrication runs have enabled practical training with a complete design-fabricate test cycle to take place within a short time. The edX “Silicon Photonics Design, Fabrication and Data Analysis” online short course (7 weeks long) teaches students and industry professionals how to design integrated optical devices and circuits, using a hands-on approach [18]. We fabricate participants’ designs using state-of-the-art silicon photonic rapid-prototyping 100 keV electron-beam lithography facilities. We measure all participants’ designs using an automated optical probe station and provide participants with the measurement data which they then analyze. While we also do such training with foundries, the longer fabrication time results in a design cycle that typically takes one year, whereas rapid prototyping makes it possible to include a silicon photonics design cycle within an undergraduate or graduate university

single-semester course, making it very appealing for a first-time experience.

From a designer perspective, the design cycle is the same whether the fabrication is performed by a rapid prototyping facility or a major foundry. A previous publication provided an overview of the design tools and methods for circuit design [19]. This paper describes the details of all the steps involved in completing a design-fabricate-test cycle within a publicly accessible open-source Process Design Kit (PDK), SiEPIC-EBeam-PDK [20], developed as part of the SiEPIC program.

A PDK, at the very least, provides a description for the fabrication process (cross-section diagrams), a list of layers, and some rules to follow such as minimum feature sizes [19]. These basics are described in Section II, illustrated using example fabrication processes. Beyond these basics, the PDK should also contain additional functionality, including the capability to perform functional verification, design for test verification, and circuit simulations. It is also important to simulate the effects of lithography, particularly for structures such as Bragg gratings. Finally, a PDK is implemented in one or more design tool environments. The implementation of the PDK within the KLayout [21] environment with an add-on set of photonic-specific functionality provided in the SiEPIC-Tools package [22] is described in Section IV. Examples from a library of components and methods to create circuits are described in Section III, and examples of some circuits fabricated and tested are presented in Section VI. Section V describes layout verification in terms of manufacturability, functionality and testing, including packaging. Optical and electrical tests are described in Section VI.

We show that even in the absence of a germanium process, a “germanium-less” process can still be used to make photonic systems that require electronic feedback. We can implement O-E-O conversion using photoconductive heaters [23], a device that offers both detection and an electrically-controlled phase shift.

The design tool discussions in this paper apply equally to working with deep-UV lithography foundries. Discussed in Section II-G, we have developed a pathway to transition from EBL-based rapid-prototyping to deep-UV based foundry fabrication. The key challenge is that EBL and deep-UV lithography can have very different realizations in regards to what is drawn in the layout versus the geometry that is fabricated: for a 90 degree corner, EBL results in near-perfect corners, whereas deep-UV results in significant smoothing; we can predict and include these differences during the design cycle. Utilizing the speed advantage of EBL fabrication, it is thus possible to rapidly prototype challenging designs with a lower cost, then proceed with higher cost, higher volume, deep-UV fabrication, once the designs have been verified to work.

## II. FABRICATION PROCESSES

Since rapid prototyping facilities typically perform services on a low-volume basis, each job can be readily customized allowing users to mix and match process steps; thus these facilities are flexible in the fabrication processes that they offer. Several processes are described next with options for:

TABLE I  
COMPARISON BETWEEN DUV-BASED FABRICATION IN A CMOS PILOT LINE VERSUS FABRICATION THROUGH AN ELECTRON-BEAM LITHOGRAPHY RAPID PROTOTYPING SERVICE.

	DUV CMOS pilot line	EBL Rapid-Prototyping
Process maturity	Mature fabrication processes; many fabrication steps; high yield; allows for complex systems to be reliability built.	Experimental fabrication processes; new capabilities, e.g., high resolution fabrication, novel materials.
Mask layers	Many mask and process layers (e.g. 20); allows for comprehensive photonic functionality.	Low number of mask layers; reduced photonics functionality (e.g., passive plus heaters).
Lithography	Deep UV lithography (193 or 248 nm); significant feature smoothing; requires masks; steppers; high throughput.	Direct-write (maskless) using a small electron beam (10-20 nm); accurate feature reproduction; low throughput.
Turn-around time	3 to 12 months for active photonic processes; well defined fabrication schedules.	Less than one week (using direct-write EBL) to one month, depending on process complexity.
Quantity of chips	Fabrication is performed on one or more wafers; client receives many chip copies.	Fabrication is performed in small batches of one wafer or less; low volume; user can purchase a single die.
Cost	Minimum orders for MPW runs are typically in the tens of thousands of dollars.	Single chip typically starts around one thousand dollars.

- Passives, described in Section II-A: a single etch process, with a full etch in a 220 nm SOI layer, oxide cladding, with a design area of 8.8 x 8.8 mm.
- Passives with heaters, described in Section II-B: adds resistive metal heaters above the waveguides, to be used as phase shifters, with an option for thermal isolation, described in Section II-C.
- Module for edge coupling, described in Section II-D: adds a deep etch to provide a smooth edge of the chip for edge coupling.
- Actives, described in Section II-E: adds doping, metal vias, and metal interconnects and bond pads. Herein, we discuss N and N++ doping, although P and P++ are also possible. Doping with a single species, such as N and N++ doping, enables 1) doped waveguide heaters [24], 2) defect-mediated detectors [25], 3) in-resonator photoconductive heaters (simultaneous phase shifter and photodetector) [23], and 4) permanent trimming by thermally-induced dopant diffusion [26].

Both WNF and ANT facilities offer custom fabrication services. Optional services are available on request, including dicing into sub-chips, alternative cladding materials, and multi-tier etching (for partial-etch grating couplers and rib waveguides).

This Section builds on past work on passive silicon photonics fabrication, and emphasizes the active process that includes doping to demonstrate photoconductive heater-detectors.

#### A. Passive silicon photonics fabrication process

The simplest silicon photonics fabrication process available at both WNF and ANT consists of a single etch in a thin silicon layer [13]. The process uses a silicon-on-insulator (SOI) substrate with an active silicon (Si) layer thickness of 220 nm and a buried oxide (BOX) thickness of either 3000 nm (WNF) or 2000 nm (ANT), diced into 25 mm squares (WNF, ANT) or processed on 100 mm or larger wafers (ANT). Designs are first processed using the BEAMER software from GenISys, with multiple options available including the advanced single-line smoothing (SLS) method [27] described in Appendix A. Patterning is performed using hydrogen silsesquioxane (HSQ) resist exposed in a JEOL JBX-6300FS (WNF) or JBX-8100FS (ANT, at The University of British Columbia) electron beam

lithography system using 100 keV beam energy, 8 nA beam current, base dose of 1800  $\mu$ C/cm<sup>2</sup>, dose-modulation proximity effect correction, and a field-shift of 2, in which the pattern is written twice with a shift of one-half of the field size of 500  $\mu$ m (WNF) or 1000  $\mu$ m (ANT) between the two written passes. The fundamental placement grid is 1 nm (WNF) or 0.5 nm (ANT); this is the minimum increment to which a shape can be positioned. However, to achieve reasonable throughput for large patterns, a pixel spacing of 6 nm is used; this is also known as the shot-pitch, or beam step size, and is the spacing between pixels filling each shape. Resist development is in 25% tetramethyl-ammonium hydroxide (TMAH) for 4 minutes, followed by rinsing first in deionized (DI) water, then isopropyl alcohol (IPA), and finally drying with nitrogen (N<sub>2</sub>). The pattern is then transferred into the silicon device layer using a chlorine (Cl<sub>2</sub>) Inductively-Coupled Plasma (ICP) etch. The remaining resist is then stripped in buffered hydrofluoric acid (HF), and a passivation layer of 2000 nm of SiO<sub>2</sub> is deposited using PECVD.

#### B. Heaters process module

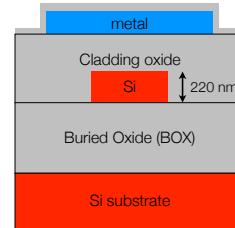


Fig. 1. Cross-sectional diagram of the full-etch silicon photonic process, with a metal heater above the waveguide.

This section describes an option to implement thermo-optic phase shifters based on resistive metal heaters placed above the waveguide layer, as shown in Fig. 1. The addition of heaters to a passive process allows designers to build circuits, such as cascaded microring add-drop filter devices described in Section VI-A and Fig. 23, and neuromorphic photonic systems described in Section IV-C and Fig. 19.

The description is based on the NanoSOI rapid prototyping service offered by ANT [14]. The thermo-optic phase-shifter process uses titanium-tungsten (TiW) micro-heaters

and aluminum routing traces. The heaters are capped with a thin passivation oxide to protect them from oxidation damage and extend operational lifetime and maximum heat output. Bonding pads are opened through the oxide capping layer to provide direct electrical contact to the aluminum for probing or wire bonding. Fig. 2 shows a TiW heater element (width 4  $\mu\text{m}$  and thickness 200 nm) in operation at high power output, where light emission from the heater is visible on the CCD camera.

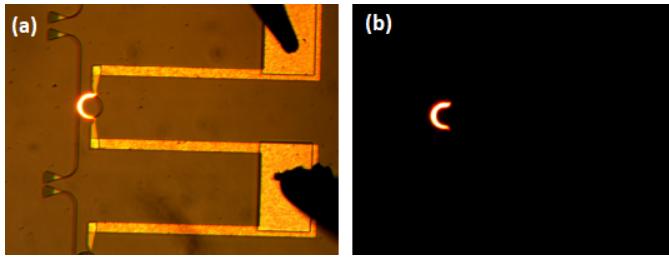


Fig. 2. Operation of a semi-circular heater element for thermo-optic phase shifting of a microring resonator, with an estimated heat power output of 150 mW. Images are captured with a CCD camera with an illumination lamp (a) on and (b) off.

### C. Thermal isolation process module

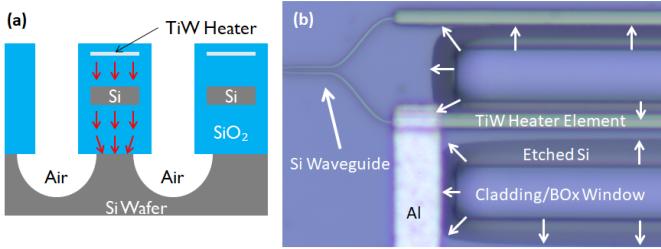


Fig. 3. Reduction of thermal cross-talk in an MZI switch. (a) Schematic of an MZI device showing an oxide window and lateral silicon etching (red arrows denote direction of heat flow), and (b) microscope image of a fabricated MZI device. Darker regions are laterally-etched silicon that is visible through the transparent cladding oxide and BOX layers.

Leakage of heat into waveguides not targeted for phase shifting (thermal cross-talk) is a challenge in dense photonic circuits. Trenches can be created through the cladding and buried oxide layers to create a thermal barrier between devices. A similar process has been used to make efficient thermal tuning in ring resonators [28], and with the addition of an undercut, has been used to demonstrate ultra-efficient thermo-optic phase shifters in interferometers [29]. An example device fabricated with the ANT process is shown in Fig. 3 where two arms of a Mach-Zehnder interferometer (MZI) switch are thermally isolated using a combination of a cladding/BOX window etch and lateral etch of the handle silicon underneath the BOX. The lateral silicon etch can be tailored to remove the handle silicon and fully suspend the cladding and waveguide (provided there is enough structural stability to avoid collapse) or leave a silicon pillar for added mechanical support, as in Fig. 3a. The ANT process uses an AZP4620 photoresist mask, an anisotropic high-bias ICP-RIE process for the oxide

window etch and an isotropic low-bias ICP-RIE process for the lateral silicon etch. Placement accuracy of the oxide windows is limited to  $\pm 2 \mu\text{m}$ .

### D. Edge coupling process module

ANT also offers a process option to implement edge couplers which allow for single fibers, fiber arrays and die-based adapters to couple directly to waveguides. High-efficiency edge couplers fabricated with this process are described later in Section III-B. They are based on a deep trench etch to create an optical quality facet for nanotaper or sub-wavelength grating edge couplers, using a switched high-rate ICP-RIE etch process. The entire depth of the handle silicon is removed, which enables die-based adapters to easily couple directly to the devices.

### E. Active Silicon Photonics Fabrication process

Building on the passive process, the following describes a “germanium-less” active silicon photonics process, which includes both phase shifters and detectors using defect-mediated detection.

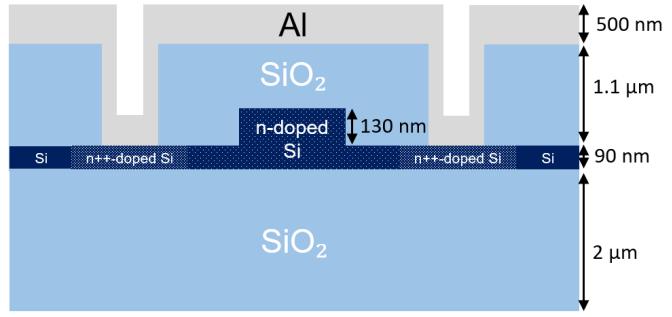


Fig. 4. Cross-sectional diagram of the silicon photonic process that includes rib waveguides with electrical contacts and doping. These are used to make in-resonator photoconductive heater devices described in Section VI-C (not to scale).

The passive waveguides, masking layers for doping and metal contacts for the in-resonator photoconductive heater (IRPH) devices were fabricated by ANT. Ion implantation of phosphorous dopants and rapid thermal annealing was performed at McMaster University. The mean silicon device layer thickness of the starting 100 mm SOI wafer was measured to be 221.1 nm. After cleaning the wafer using a 3:1 piranha solution, a negative-tone electron beam resist (hydrogen silsesquioxane, HSQ) was spin-coated onto the wafer and baked. The design file (GDS) was fractured and proximity corrected using GenISys’ BEAMER software, and described in Appendix A. The resist was patterned using a JEOL JBX-8100FS high-throughput EBL system (capable of fabricating 200 mm wafers) at 100 keV electron energy and 4 nm shot pitch size with a 5 nA beam current (the machine grid is 0.5 nm). The HSQ mask was developed with immersion in a 25% tetramethylammonium hydroxide (TMAH) solution. The unprotected regions of the silicon device layer were partially etched down to an average thickness of 84.5 nm using an ICP reactive ion etch process. After removal of the HSQ

mask using 10:1 buffer oxide etchant (BOE), the devices were imaged using a scanning electron microscope at 15 keV energy to confirm the fabrication quality of the waveguides, e.g., Fig. 5.

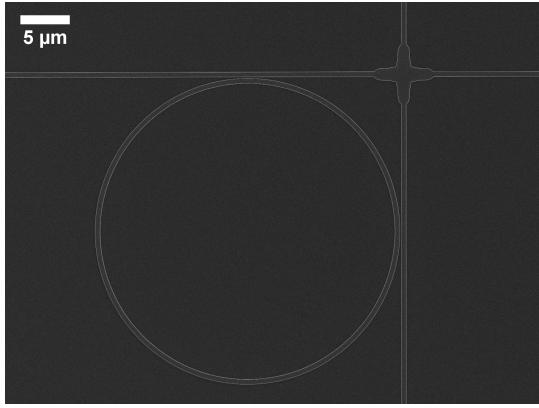


Fig. 5. Top-down scanning electron microscope image of a passive microring resonator, before ion implantation and deposition of oxide cladding. This ring is used in the 2x2 switch described in Section VI-C.

To estimate the losses of the partially etched rib waveguides (500 nm core width and a slab thickness of 90 nm), 4 spirals with a length of 0, 5.733, 9.429 and 20.612 mm were fabricated, and the cut-back method was used to estimate the optical power propagation loss. Fig. 6 shows the extracted loss in (dB/cm) across wavelength, for both chips fabricated with and without the SLS technique (see Appendix A). The SLS technique improved the losses by  $\sim 0.3$  dB across the C-band. Further investigations of this technique are required to optimize the waveguide propagation loss.

Selective phosphorous doping was accomplished by masking the silicon using a 1.2  $\mu\text{m}$ -thick HPR504 mask patterned with photolithography on an ABM manual mask aligner. The overlay accuracy of the patterning process to the silicon features is  $\pm 1 \mu\text{m}$ . Two successive masking and implantation cycles were performed to implement lightly-doped (N) and heavily-doped (N++) silicon regions. Two dopants were used: N was used as a light dopant with a nominal, average concentration of  $1.0 \times 10^{17} \text{ cm}^{-3}$  to result in a conductive semiconductor, with a doping concentration that did not in-

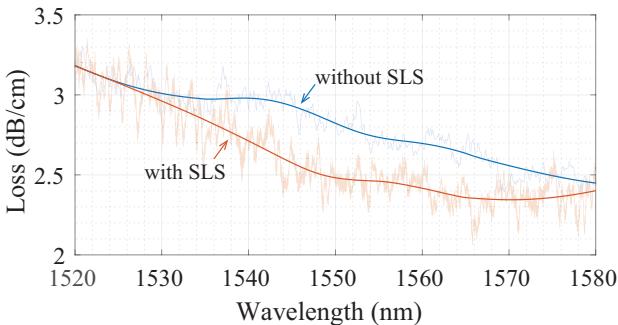


Fig. 6. Optical losses of the partially etched curved rib waveguides (500 nm core width and a slab thickness of 90 nm) measured using the cut-back method using spiral waveguides, for chips fabricated with and without the SLS technique. The smoothed measured data is plotted with thick solid lines.

duce significant waveguide propagation loss; N++ with a concentration of  $1.0 \times 10^{20} \text{ cm}^{-3}$  was used to make electrical contacts.

Doping was performed via ion implantation using the McMaster University Universal Ion Implanter within the Centre for Emerging Device Technologies (CEDT). To create the n-doped channel (N) regions, phosphorus was implanted at two energies, 25 keV and 60 keV, both to a dose of  $2.5 \times 10^{12} \text{ cm}^{-2}$ . For the n-doped contact regions (N++), an implantation of phosphorus at 20 keV to a dose of  $1.0 \times 10^{15} \text{ cm}^{-2}$  was performed. The implants were performed at  $7^\circ$  off-axis to avoid channeling effects. Activation of the phosphorus doping was achieved via annealing of the samples at  $970^\circ\text{C}$  for 1 minute in flowing nitrogen using a JipElec Rapid Thermal Processor.

To create the contact pads for wire bonding, a 1.1  $\mu\text{m}$ -thick  $\text{SiO}_2$  layer was first deposited using plasma-enhanced chemical vapor deposition (PECVD) at  $300^\circ\text{C}$ . This layer serves as an optical cladding medium for the waveguides, and also physically isolates the metal contact pads from the evanescent field of the waveguide. Openings in the  $\text{SiO}_2$  layer were created over the heavily-doped N++ regions (mask "VC") using HPR504 positive-tone photoresist and the exposed  $\text{SiO}_2$  was etched using an RIE system. The etch was only ran to a depth of 950 nm since the high-bias RIE process can damage the thin silicon layer underneath. The remaining 150 nm of oxide was removed with immersion in a 10:1 BOE solution for 4 minutes. A 35% overetch was done to ensure that all of the  $\text{SiO}_2$  in the openings was removed in preparation for the aluminum metal deposition. The HPR504 photoresist mask was removed with acetone and a 500 nm-thick aluminum film was deposited using a planar magnetron sputtering process. The sputtering system has an angled gun and a rotating stage for directing metal into the via openings and sidewalls for good electrical connection between the doped silicon layer and top aluminum film. Contact pads, vias and traces were patterned into the aluminum film using a HPR504 photoresist mask (mask "Metal") and immersion in an aluminum wet etchant solution. To reduce the electrical resistance between the silicon and aluminum vias, it is then recommended to perform an anneal at approximately  $400^\circ\text{C}$  in an  $\text{N}_2$  environment, or apply a moderate bias voltage to the devices to stress the contacts. During device testing, a "burn-in" of up to 40 V was initially applied to the devices to reduce the contact resistance. This was applied using a constant current source of 0.1 mA with a voltage compliance of 40 V.

#### F. Design Rule Check (DRC) verification

Design Rule Check (DRC) verification is traditionally focused on manufacturing rules provided by the foundry. These rules are in place to ensure that the design will function as expected without damaging the fabrication equipment or contaminating other designs. Verification is performed using tools such as Mentor Calibre, or using KLayout's DRC engine.

The rules in place for the Active process described in Section II-E are listed in Tables II, III, and IV.

The doping and metal masks are performed using contact optical lithography, and are independently aligned to the Si

TABLE II  
MINIMUM FEATURE SIZES

Layer	Minimum size
Si: Silicon partial etch	60 nm
Si N: Silicon N	5 $\mu$ m
Si N++: Silicon N++	5 $\mu$ m
VC: Oxide contact vias	5 $\mu$ m
Metal: Aluminum	5 $\mu$ m

TABLE III  
MINIMUM SPACE BETWEEN LAYERS (EXCLUSION)

Layer	Si	Si N	Si N++	VC	Metal
Si	60 nm	-	2 $\mu$ m*	3 $\mu$ m*	-
Si N	-	5 $\mu$ m	-	-	-
Si N++	2 $\mu$ m*	-	5 $\mu$ m	-	-
VC	3 $\mu$ m*	-	-	5 $\mu$ m	-
Metal	-	-	-	-	10 $\mu$ m

layer. We assume that the overlay accuracy for each mask is 1  $\mu$ m. This means that doping and metal masks may be offset from each other by twice of this amount. This has implications on the Inclusion and Minimum space rules. In order to ensure electrical contact between the layers, the following Inclusion rules are defined (also see Table IV). Rules that are marked with a “\*” are recommendations to ensure a functional circuit; they are not strict “manufacturing” rules.

- Si N overlapping Si N++\*: doped regions must overlap each other so that a good electrical contact is made between the two doped silicon regions.
- Via inside Si N++\*: this is required so that a good electrical contact is made between the metal and the silicon.
- Via inside Metal: this is required so that a good electrical contact is made between the metal and the metal via.

#### G. Lithography simulation

To account for the difference in the lithography processes between EBL and deep-UV lithography, we have developed a lithography model which simulates the fabrication outcome of a deep-UV process. The high resolution of EBL fabrication can then be used to fabricate this simulated design allowing for experimental measurements and adjustments before investing into a deep-UV fabrication run. The lithography model can also be used to more accurately predict the response of a device, such as the Bragg gratings described in Section III-C, where previous work showed that the smoothing has a significant impact on Bragg grating, typically reducing the bandwidth by a factor of 2 or more [30].

TABLE IV  
INCLUSION OR OVERLAP (A MUST BE INSIDE B)

A	B				
	Si	Si N	Si N++	VC	Metal
Si	-	-	-	-	-
Si N	-	-	-	-	-
Si N++	-	3 $\mu$ m*	-	-	-
VC	-	-	3 $\mu$ m*	-	5 $\mu$ m
Metal	-	-	-	-	-

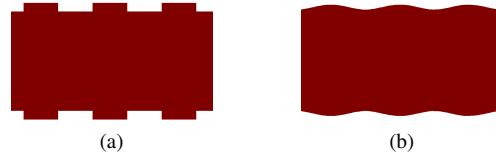


Fig. 7. Layout of a TE 1550 nm Bragg grating device. a) as-designed geometry, b) geometry after performing 193 nm deep-UV lithography simulations.

The lithography model is built on test structures previously fabricated using 193 nm deep-UV lithography by IME A\*STAR, Singapore. The model was validated using straight Bragg grating waveguides as well as the more complex contra-directional grating-assisted couplers [31]. An example of the lithography simulation can be seen in Fig. 7. To access the lithography simulations, there are several options: 1) the PDK provides a client-server system, where the client (KLayout SiEPIC-Tools) sends the ideal design file to the server (Linux workstation with Mentor Calibre installed) which performs the lithography simulation and returns the result on a separate layer in the output file, 2) the lithography simulation is available as part of the upload submission process for the SiEPIC-EBeam-PDK layout submission process [32], or 3) local execution of the lithography simulation software, Mentor Calibre Computational Lithography [33].

### III. COMPONENT LIBRARY

This section describes some of the components that have been fabricated, tested, and added to the open-source library, SiEPIC-EBeam-PDK, as either fixed cells, or as parameterized cells [20].

The library contains devices to couple light in and out of the chip (grating couplers, edge couplers), splitters (y-branch, directional coupler, adiabatic coupler), filters (Bragg gratings, contra-directional grating-assisted couplers, and ring resonators). Using these building blocks, circuits such as interferometers or multi-ring systems can be assembled, simulated, and fabricated.

#### A. Grating couplers

We use different types of grating couplers (GCs) in our rapid prototyping fabrication depending on the choice of etch depth: partial etch versus full etch. We often prefer to use process with a single etch in order to have a rapid turn-around time, reduce fabrication complexity, and to save cost.

For most of our fabrication runs (Sections II-A and II-B) we use a fabrication process that results in strip waveguides; thus we use a GC that was designed specifically for a full etch. To achieve the correct grating strength and reduce back-reflections, sub-wavelength structures (or meta-materials) are used to replace the partial etch region. This cell is available as a fixed cell “ebeam\_gc\_te1550” [34], and as a parameterized cell “Focusing Sub-wavelength grating coupler (fswgc)” [20], and achieves a best-case insertion loss of 4.1 dB with a 1-dB bandwidth of 30.6 nm.

For the active process described in Section II-E, we need to make electrical contacts to the device. Thus we use a rib

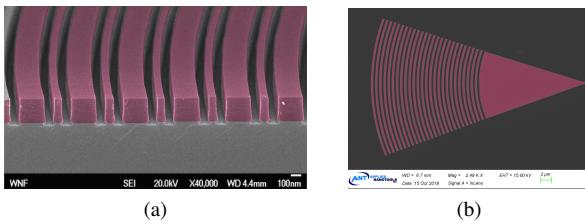


Fig. 8. SEM images (false colour) of optical fibre grating couplers, a) full-etch grating coupler, using sub-wavelength gratings, b) partial-etch grating coupler.

waveguide, and a partial etch GC designed using a parameterized universal GC [35], where the user-specified design-intent parameters are: wavelength = 1550 nm, silicon thickness = 220 nm, etch depth = 130 nm (resulting in a 90 nm silicon slab, as in Fig. 4), polarization = TE, duty cycle = 0.5, and insertion angle = 29 degrees. This cell is available as a parameterized cell “Universal Grating Coupler” and as a fixed cell “ebeam\_gc\_te1550\_90nmSlab” in the SiEPIC-EBeam-PDK [20].

### B. Edge coupler

End coupling an optical fiber to an on-chip edge coupler at the chip facet is a straightforward way to inject light to and from on-chip circuits and components for rapid prototyping. To match the larger fiber mode (9  $\mu\text{m}$ ), the silicon waveguide effective index is decreased from 2.45 to around 1.46 near the facet, thus increasing the mode size (to 3  $\mu\text{m}$ ) and its mode overlap with the fiber. This reduction can be done by narrowing the strip waveguide width to create an inverse taper [36], as shown in inset (1) of Fig. 9a or by using a sub-wavelength grating (SWG) waveguide [37] as in Fig. 9b, with the fabrication approach described in Section II-D. The latter is enabled by the small feature size achievable by EBL, as sub-100 nm features are necessary for operation in the sub-wavelength regime. The SWG coupler offers an additional degree of freedom compared to the strip coupler. By reducing the fraction of silicon, a good overlap can be achieved while keeping a square cross-section. This explains the lower polarization dependent loss achieved with the SWG coupler. The larger bandwidth is due to the lower dispersion of the SWG when operating in the sub-wavelength regime.

The efficiency of strip and SWG edge couplers coupled to an SMF-28 cleaved fibres are shown in Fig. 9a and b, respectively. The strong ripples in the couplers’ responses are caused by the absence of anti-reflection coatings or an matching-index gel at the air-chip interface, resulting in a non-negligible Fresnel reflection and a weak Fabry-Perot effect. The main limitation to achieving higher efficiency comes from the finite extent of the waveguide bottom (2  $\mu\text{m}$  BOX) and top (2  $\mu\text{m}$  SiO<sub>2</sub>) cladding which prevents the design of a large mode that matches the 9  $\mu\text{m}$  fibre mode, and results in a poor mode overlap and therefore high insertion loss. By replacing the cleaved SMF-28 fibre with a small spot size (2.5  $\mu\text{m}$ ) lensed fibre, the average efficiency (for TE and TM polarizations) is increased by  $\sim 5$  dB for both couplers reaching  $\sim 1$  dB per

fiber-to-chip coupling, as shown in inset (2) of Fig. 9. In this case, the couplers are designed to match the smaller mode size. The combination of SWG couplers and lensed fibers provides a coupling solution for components requiring very low insertion loss. The remaining coupling losses arise mainly from Fresnel reflections and leakage losses in the low confinement, tapered region. The SWG edge coupler is available in the SiEPIC-EBeam-PDK as cell “ebeam\_swg\_edgcoupler” [20].

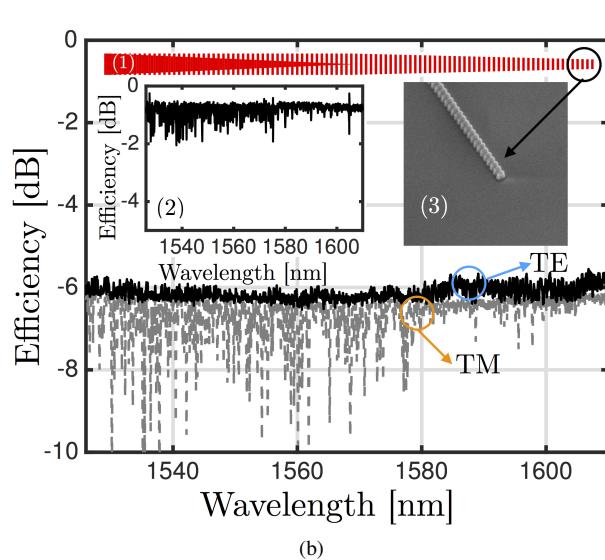
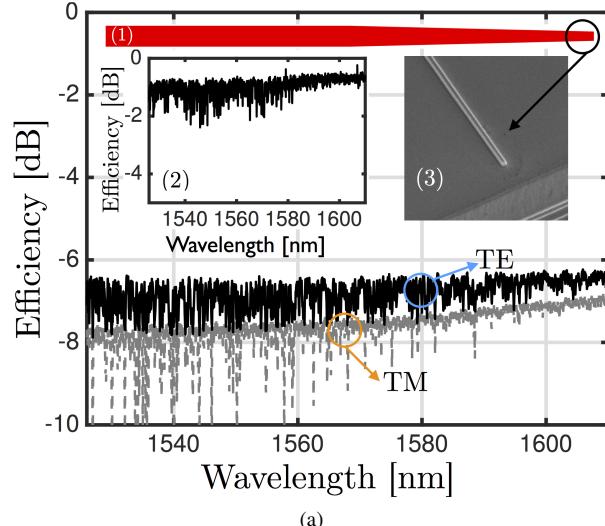


Fig. 9. Coupling efficiency over the C+L band using an SMF-28 cleaved fiber for (a) a sub-wavelength grating coupler and (b) a strip nanotaper edge coupler. Inset (1) schematically shows the coupler taper, (2) shows the averaged efficiency (TE-TM) when using a 2.5  $\mu\text{m}$  spot size tapered fiber and (3) shows an SEM picture of each coupler.

### C. Bragg filter

Realizing 2-port Bragg grating filters on the SOI platform can be implemented by corrugating the sidewalls of the waveguides, as shown in Fig. 10a. Such filters can be parameterized by controlling the corrugations width, corrugations period, corrugations profile, and the average waveguide width. These parameters can control the filter characteristics such as the

filter's shape, bandwidth, and central wavelength. Detailed discussion on their design is available in the literature [38].

The Bragg grating is available in the SiEPIC-EBeam-PDK as a parameterized cell “ebeam\_bragg\_te1550” [20]. This component allows the designer to change the period, number of grating periods, the corrugation width, the grating misalignment [39], and to choose a geometry type (rectangular or sinusoidal). The gratings have been fabricated, measured, and compact models have been built, as described in Section III-G. Such Bragg filters have negligible insertion loss [40]. Additionally, the cell can be parameterized to create filters with a wide range of bandwidths, from as narrow as 0.4 nm and as high as 20 nm [39].

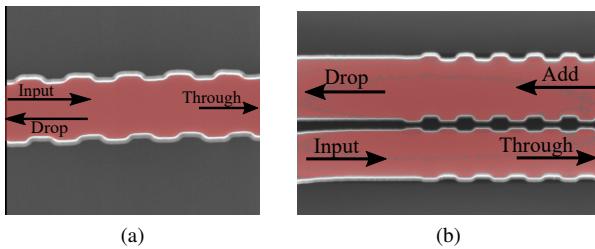


Fig. 10. SEM images (false colour) of Bragg grating-based devices on stip waveguides: (a) 2-port Bragg grating filter, (b) 4-Port contra-directional coupler.

#### D. Contra-directional coupling-based filters

Contra-directional couplers (contra-DCs, CDCs) are 4-port devices which consist of a set of two parallel Bragg grating waveguides. Using such devices offers an advantage over conventional single waveguide Bragg grating-based filters since the filtered (dropped) wavelengths in CDCs are coupled backwards (contra) from the input waveguide, into the parallel add/drop waveguide (see Fig. 10b). Thus, the need of on-chip or external circulators to extract the dropped wavelengths are eliminated. Similar to conventional Bragg gratings, the CDC can be parameterized to control the filter's shape, bandwidth, and central wavelength, while maintaining negligible insertion losses. Detailed discussion on their design is available in the literature [41]. CDCs are an attractive approach to realize on-chip CWDM (de) multiplexers, since multiple CDCs with different design parameters can be cascaded to realize a multi-channel optical add-drop multiplexer (OADM) filters over a communication band [42]. CDC-based CWDM OADMs have several advantages over arrayed waveguide gratings (AWG) based OADMs as they can be designed to have low insertion losses, wide-bandwidths, flat-top responses and low inter-channel crosstalk levels with a small on-chip footprint [43].

The CDC is available in the SiEPIC-EBeam-PDK as a parameterized cell “contra-directional coupler” [20]. This component allows the designer to change the period, number of grating periods, the corrugation width, corrugation profile (uniform, chirped, apodized), the grating misalignment [44], and the geometrical shape (rectangular or sinusoidal).

To assist the system designers with choosing the proper design parameters of the CDC, a modeling and simulation flow

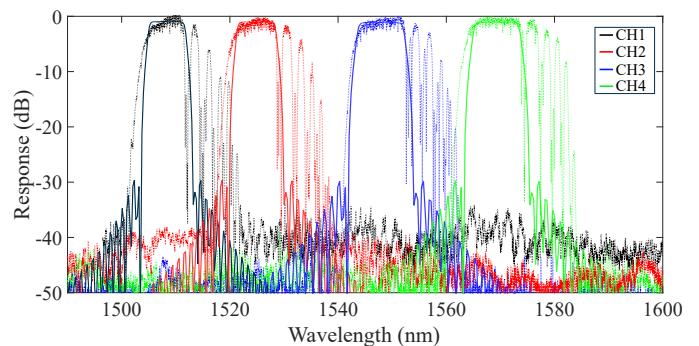


Fig. 11. A 4 channel CWDM demultiplexer implemented using 4 cascaded contra-directional couplers with different corrugation periods (period = [0.312, 0.320, 0.328, 0.336]  $\mu\text{m}$ ). All other parameters are held constant (number of grating periods = 1000, gap = 0.1  $\mu\text{m}$ , waveguide 1 corrugation width = 0.024  $\mu\text{m}$ , waveguide 2 corrugation width = 0.048  $\mu\text{m}$ , waveguide 1 width = 0.44  $\mu\text{m}$ , waveguide 2 width = 0.56  $\mu\text{m}$ , Gaussian index for apodization = 2.7). The experimental results (dotted) are compared with the simulated results (solid) obtained from the SiEPIC-EBeam-PDK simulation flow.

was implemented for the CDCs in the SiEPIC-EBeam-PDK. The PCell is first drawn with the designer's parameters and implemented in the layout, and then an eigenmode simulation is performed on the two-waveguide system to extract the effective indices and group indices of the two waveguides. An FDTD bandstructure calculation using Bloch boundary conditions is then performed to extract the coupling coefficient of the grating [39]. Whereas a Bragg grating band structure calculation needs only to be done at the  $k_x = 0.5$  point in the band structure, for the CDC it is not known a-priori where the operating point will be. Thus, a recursive search for the operating point ( $k_x$  and frequency) needs to be performed. Next, the PCell parameters, effective and group indices fits, and coupling coefficients are used in an analytic coupled-mode theory, transfer matrix model [41] to simulate the overall response of the CDC. Finally, the generated transfer function can be parsed into a scattering-parameters file to create a compact model of the device, compatible with circuit simulation design tools. Fig. 11 shows a 4-channel demultiplexer implemented using 4 cascaded CDCs. Note that the large sideband lobes can be suppressed by reducing the grating corrugation widths, and potentially using apodization parameters suitable for the length and grating strength of the device.

#### E. Mode-evolution adiabatic splitter

Mode-evolution-based optical power splitters, also known as adiabatic 3 dB couplers, are 2x2, 4-port devices that are used for coupling/splitting light evenly over a broad wavelength range. In an adiabatic 3 dB coupler, two asymmetric waveguides are typically used as Ports 1 and 2 to excite only one supermode (either the lowest-order even or lowest-order odd supermode) of the two waveguide system when light is injected into either Port 1 or Port 2, respectively (Fig. 12a). The excited supermode, either the even or odd mode, will evolve into the same order supermode of the two symmetric waveguides at Ports 3 and 4 for broadband 3 dB power splitting (Fig. 12b). The adiabatic 3 dB coupler also

works in reverse when light is injected into Ports 3 and 4. When light is injected into either Ports 3 or 4, the lowest-order even and lowest-order odd supermodes are excited equally and evolve into the same order supermodes of the asymmetric waveguides at Port 1 and Port 2, respectively, for broadband, even power splitting. No mode conversion occurs between the supermodes and, therefore, there is no mode interference between the supermodes.

For rapid prototyping, we first developed an SOI adiabatic 3 dB coupler based on shallow-etched rib waveguides having 220 nm high core and 90 nm high slab [45]. This device has a 100  $\mu\text{m}$  long mode evolution region and was fabricated using EBL tools. For this device, we obtained 50/50 power splitting over a wavelength range from 1500 nm to 1600 nm for the TE mode with an imbalances of  $<0.5$  dB. After demonstrating our device using EBL tools, we fabricated the rib-waveguide-based adiabatic 3 dB coupler using both the 248 nm and the 193 nm deep-UV lithography processes that are provided by IME at Singapore. Fabricated using deep-UV lithography, this device has been widely used for building integrated photonic circuits including micro-ring-based optical gyroscopes [46], MZI modulators [47], Michelson interferometric modulators [48], [49], and optical switches [29]. This device has been included as a fixed cell in both the SiEPIC-EBeam-PDK for EBL tools and the SiEPIC-AMF-Library (custom library for the AMF deep-UV optical lithography process).

We then designed the devices using SWG-based waveguides (see Fig. 12a and b) that enable compact design and require only a single-etch process for fabrication. We demonstrated adiabatic 3 dB couplers using SWG waveguides that had a total coupler length of 50  $\mu\text{m}$  and achieved 50/50 power splitting over a wavelength range of 1490 nm to 1620 nm with an imbalance of  $<0.3$  dB [50]. The SWG adiabatic 3 dB coupler is available in the SiEPIC-EBeam-PDK as cell “ebeam\_splitter\_adiabatic\_swg\_te1550” [20].

To further improve the device performance, we designed compact, ultra-broadband adiabatic 3 dB couplers utilizing SWG-assisted strip waveguides for TE mode operation [51]. The SWG-assisted adiabatic 3 dB coupler, having a mode evolution region of only 15  $\mu\text{m}$  and a total length of 35  $\mu\text{m}$ , has a theoretically-predicted operating bandwidth from 1200 nm to 1700 nm and experimentally achieved TE mode power splitting with an imbalance of  $<0.3$  dB and average excess losses of  $<0.11$  dB over the measured 185 nm wavelength range (from 1455 nm to 1640 nm). The SWG-assisted adiabatic 3 dB coupler is available in the SiEPIC-EBeam-PDK as cell “ebeam\_splitter\_adiabatic\_swg\_assist\_te1550” [20].

#### F. Ring resonator sensors

Silicon photonic devices have emerged as excellent transducers for continuous and quantitative label-free biosensing in the past decades [52]. By changing the external refractive index, the evanescent field around the waveguide is disturbed, which further affects the behavior of the propagation mode in the waveguide, thereby realizing the real-time detection. Among all configurations, ring resonators have been investigated extensively as an emerging sensing technology

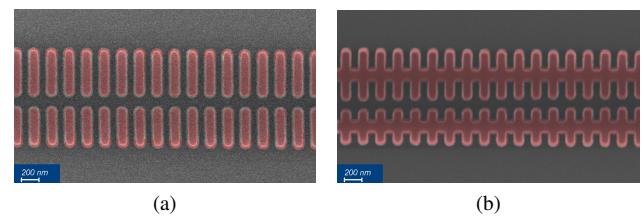


Fig. 12. SEM images of SWG-based waveguides for adiabatic 3 dB couplers: (a) Two SWG waveguides with different widths, (b) two SWG-assisted strip waveguides with different SWG widths.

due to their small footprint for highly-compact multiplexed assays [53]–[55]. To characterize sensor performance, the most widely used figures of merit are the sensitivity ( $S$ ) and detection limit (DL), which represent the strength of light-matter interactions and the minimum refractive index change for a detectable output signal, respectively. Two specific types of sensitivities are defined in biosensing applications to distinguish the status of target molecules: the bulk sensitivity ( $S_{\text{bulk}}$ ) and the surface sensitivity ( $S_{\text{surf}}$ ) which monitors the refractive index change in the entire cladding and within the first few tens to hundreds of nanometers above the surface, respectively [7]. Compared to the surface sensitivity, the bulk sensitivity aims to characterize the refractive index sensing capability in bulk solution, which can offer a rough comparison among different sensor geometries.

For a conventional ring resonator-based sensor at 1550 nm wavelengths in the TE mode, the bulk sensitivity is around 38 nanometer per refractive index units (nm/RIU) [6], which is far below the performance of Surface Plasmon Resonance (SPR) sensors, as well as commercialized evanescent field-based refractive index sensing approaches (e.g., Biacore Life Sciences). To satisfy the requirement of modern clinical diagnostic tests, modal/structural improvements have been investigated by leveraging EBL fabrication, such as using the TM mode and SWG-based waveguides. As shown in Fig. 13, compared to the TE mode, a larger portion of evanescent field is present outside of the waveguide in the TM mode, which offers a higher light-matter interaction, thus a higher sensitivity (238 nm/RIU) [56]. Due to their simple configuration, these TM mode-based resonators can be realized by CMOS foundries based on deep-UV lithography for low-cost mass production. The regular waveguide-based ring resonator is assembled using two parameterized cells, “ebeam\_dc\_halfring\_arc”, in the SiEPIC-EBeam-PDK. The published TM-mode ring sensor uses a radius of 40  $\mu\text{m}$ , a coupling length of 3  $\mu\text{m}$ , and a coupling gap of 200 nm, which is compatible with both EBeam and deep-UV lithography processes [57].

Another method to enlarge the modal area is reducing the optical confinement of the waveguide by applying low effective index structures, such as an SWG waveguide where parts of the silicon core are periodically replaced with  $\text{SiO}_2$  or  $\text{H}_2\text{O}$ , with a high spatial frequency (Fig. 14b) [58]. These SWG-based ring resonators offer an improved bulk sensitivity of 490 nm/RIU, roughly 2-fold higher compared to TM rings [8]. Recently, we developed an SWG-based configuration which represents a sub-wavelength periodicity in both the

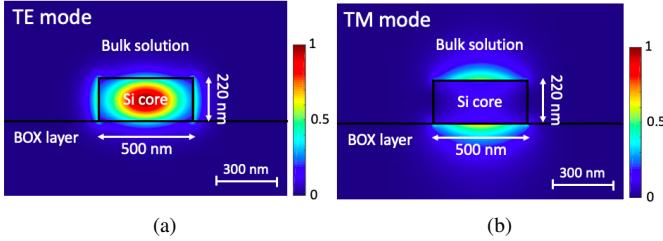


Fig. 13. Illustration of electric field intensity distributions of the (a) TE and (b) TM modes in a  $200 \times 500$  nm conventional waveguide with water cladding at 1550 nm wavelengths. Figure adapted with permission from Reference [52].

transverse and propagation directions, as presented in Fig. 14c [9]. This multi-box SWG geometry not only reduces the effective refractive index of the optical mode but also enables more surface contact area around each silicon segment for the analyte to attach, achieving a bulk sensitivity of 580 nm/RIU. A set of isopropyl alcohol (IPA) dilutions were selected as the refractive index standards for the bulk sensitivity comparison among TM, SWG and multi-box waveguide-based ring resonator sensors. The measurement results are presented in Fig. 15. The SWG waveguide-based and multi-box waveguide-based ring resonators are available in the SiEPIC-EBeam-PDK as parameterized cells, “SWG\_Ring”, “MultiBox\_Ring”, respectively [20]. Parameters we published are as follows: a radius of 30  $\mu\text{m}$ , a period of 250 nm and a duty cycle of 60% for the SWG waveguide-based ring resonator sensor [8]; and a radius of 30  $\mu\text{m}$ , a period of 240 nm, a duty cycle of 75%, a waveguide width of 180 nm, and 5 rows with a row gap of 60 nm for the multi-box waveguide-based ring resonator sensor [9]. The coupling gap is also adjustable to ensure the critical coupling in each ring configuration.

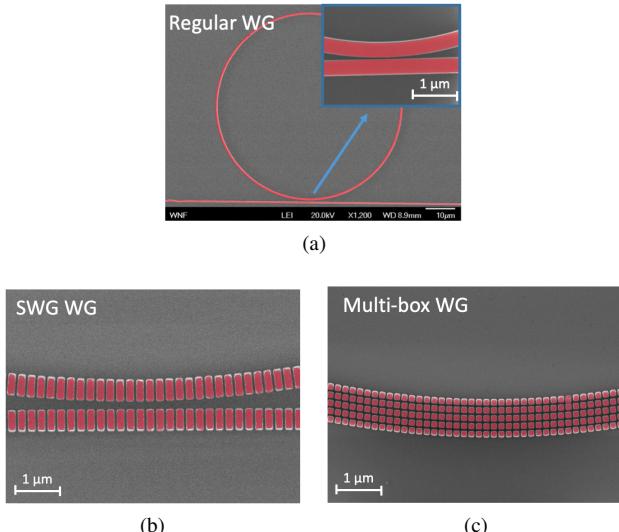


Fig. 14. Top-view scanning electron microscope (SEM) images (false colour) of (a) the regular waveguide-based ring resonator, (b) the SWG waveguide-based ring resonator magnified in the coupling region, (c) the multi-box waveguide-based ring resonator.

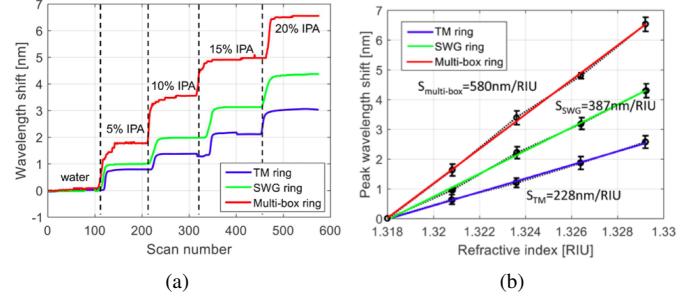


Fig. 15. (a) Measured resonant peak wavelength shifts of the TM mode, SWG, and multi-box waveguide-based ring resonators, in the presence of an IPA solution. (b) Calculated bulk sensitivity results of three proposed resonators. Figure adapted with permission from Reference [9].

#### G. Compact Model Library and Circuit Simulations

Photonic compact models are in the early years of rapid development. There are already a number of foundries providing photonic PDKs with compact model libraries (CMLs) calibrated to their specific manufacturing processes [20], [59]. Inside the PDK, each device has a compact model that matches the layout, so users have the ability to perform schematic-driven layout or layout-driven simulation, via a netlist to exchange the circuit design data. Statistical modeling is a key topic today as it is indispensable for predicting the yield of the circuit [60], [61].

Given the emphasis on rapid prototyping, we need a means of rapidly creating compact models for components to enable circuit simulations.

1) *Automated S-Parameter models:* This subsection describes how to create S-parameter models for a passive photonic device, based on a component layout. An automated compact model generation flow module was implemented in the SiEPIC-Tools [22] PDK framework. This simulation flow, shown in Fig. 16, enables the user to create a complete compact model from an arbitrarily drawn structure by utilizing 3D FDTD simulation tools to generate the S-parameters of the structure and to create a compact model suitable for circuit simulations. The user will first draw a bounding box over the structure, which defines the structure’s simulation region, and then defines the optical input and output ports of the device. The simulation module can then be launched, where the FDTD simulation parameters are set (defaults are loaded from “FDTD.xml”), including mesh accuracy, optical modes and polarization, wavelength range, and finally, an option to run corner analysis simulations based on physical parameters input for variability analysis.

The SiEPIC-Tools simulation module first extracts the polygons of the structure from the layout which are imported to the FDTD simulator. The simulation settings are then set based on the settings set above. A quick convergence test is performed to ensure the simulation span is thick enough and the results are accurate. An S-parameter sweep is then performed, where light is injected from every port of the device and measured on all the ports, for all the selected modes, and for all the possible process corners (if selected). The generated S-parameters data are then saved.

The simulation module will then launch a circuit simulation tool (Lumerical INTERCONNECT) and creates a scripted element which reads the S-parameters data files; the element is then saved in a compact model library. This compact model can then be used in circuit simulations, and is compatible with layout-aware Monte Carlo simulations [60], as the S-parameters are interpolated from the simulated corner S-parameters.

The component illustrated in the example in Fig. 16 is a  $1 \times 2$  adiabatic tapered splitter based on the design in Ref. [62]. The nanotapers have a minimum feature size of 60 nm at their tips, have gaps of 100 nm, and have a length of 25  $\mu\text{m}$ . The measured insertion loss values are  $0.03 \text{ dB} \pm 0.04$  for TE, and  $0.02 \text{ dB} \pm 0.08$  for TM. The component is available in the SiEPIC-EBeam-PDK as a fixed cell, “ebeam\_splitter\_adiabatic\_1x2” [20].

2) *Circuit Simulations*: In the design flow used in electronics, the designers start from the abstract schematic of the system, carry out simulations, then create the physical layout. In integrated photonics, particularly in a rapid prototyping context, designers often prefer to start at the physical level, namely the components and their layout. To perform simulations of a physical circuit (post-layout simulation), the approach is to generate a circuit schematic representation from the layout. Utilizing the PDK’s compact models, such a design flow, shown in Fig. 17, is made possible in the SiEPIC-Tools PDK framework [22], where a netlist is extracted and imported into a circuit simulation software [63].

In the circuit simulation software, the elements in the circuit are mapped to the compact models. This will generate a nominal simulation output of the circuit under test. Additionally, Monte Carlo circuit simulations can be performed to study the effects of wafer-to-wafer and chip-to-chip variability. The user can specify the Monte Carlo simulation parameters such as the number of simulations, within-wafer physical variations, and wafer-to-wafer variations. These simulations verify that the circuit behaves as expected, prior to sending it to the foundry for manufacturing.

#### IV. LAYOUT

As discussed in [19], there are several tools available for creating design layouts. This section focuses on the PDK implementation in KLayout [21]. KLayout supports several design flows that can be mixed depending on the project, based on user experience level, and to enable a team to collaborate on a project. The most common approach, particularly for a first-time designer, is to use the graphical user interface (GUI) to design using a library of fixed and parameterized cells (PCells). PCells are written using a programming language (typically Python). The more advanced method is a script-based approach where the script instantiates fixed cells and PCells. This can be implemented within KLayout’s IDE, or can be implemented using a procedural design method using an external Python environment.

##### A. SiEPIC-EBeam-PDK in KLayout with SiEPIC-Tools

The Process Design Kit (PDK) for the fabrication processes described above are available online. The package

SiEPIC\_EBeam\_PDK [20] provides the technology configuration and several fixed and parameterized cells. The package SiEPIC-Tools [22] provides functionality for waveguide routing, DRC, functional verification, design for test verification, netlist extraction, and circuit simulations including layout-aware Monte Carlo variability analysis.

The installation of the PDK is simple within KLayout and is done by using the built-in menu: Tools - Manage Packages. PDKs can be hosted on public servers, or on authentication-protected repositories. PDK updates are easily available via the package manager.

##### B. GUI-driven layout

For relatively simple circuits and test structures, such as data communication transceivers, where we have fewer than 100 components, creating a layout manually is often the fastest method. This involves graphically instantiating library components, snapping/aligning components, connecting them with waveguides and electrical interconnects, verifying the circuit, and performing simulations. This layout-driven approach is described in the edX online course [18] and in publications [63], [64]. Using PCells and other functionality such as snapping and verification, we created a layout of a  $2 \times 2$  optical switch. The layout is shown in Fig. 18, and test results in Section VI-C.

##### C. Script-driven procedural layout

For more complex designs, it is preferable to create the design via a program, or script. Script-driven layout is a particular implementation of a strategy known as parametric design. Parametric design means that the geometry of the layout is determined by an algorithm, or code – designers write and fine-tune the code, not the geometry. This code can take into account user-defined parameters, design rules, and technology constraints, and procedurally generates a conforming layout.

This method adds an abstraction layer between geometry and functionality – design execution and design intent, respectively. Concretely, it allows users’ layout to be compatible with multiple technologies or PDKs, and the layout can be regenerated after changes and updates occur in the technologies, PDKs, and library cells. It also allows for cooperation between different users who can code subcircuits, which will eventually be merged into a single layout and automatically placed and routed.

We can understand the principles of script-based layout with the help of a real example. Fig. 19 shows the silicon photonic neural network demonstrated in Ref. [67], fabricated on the ANT rapid prototyping platform. Neuromorphic photonics is an effort to develop radically new classes of information processors by combining the physical properties of light, the algorithmic strengths of neural networks, and the scalability of silicon photonics [10]. Photonic neural networks are large-scale and complex systems containing thousands of interconnected, configurable devices – very different from a large array of one device copied repeatedly, perhaps with variants of 2 or 3 parameters (such as the optical switch in Fig. 18). To lay

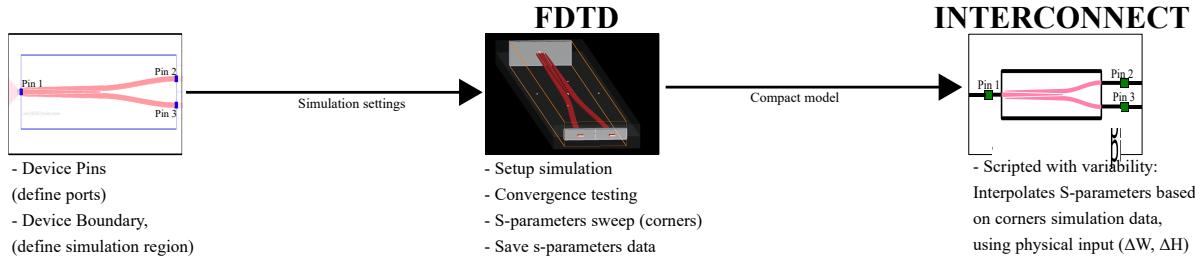


Fig. 16. The simulation flow for the SiEPIC-Tools automated compact model generation using S-parameters.

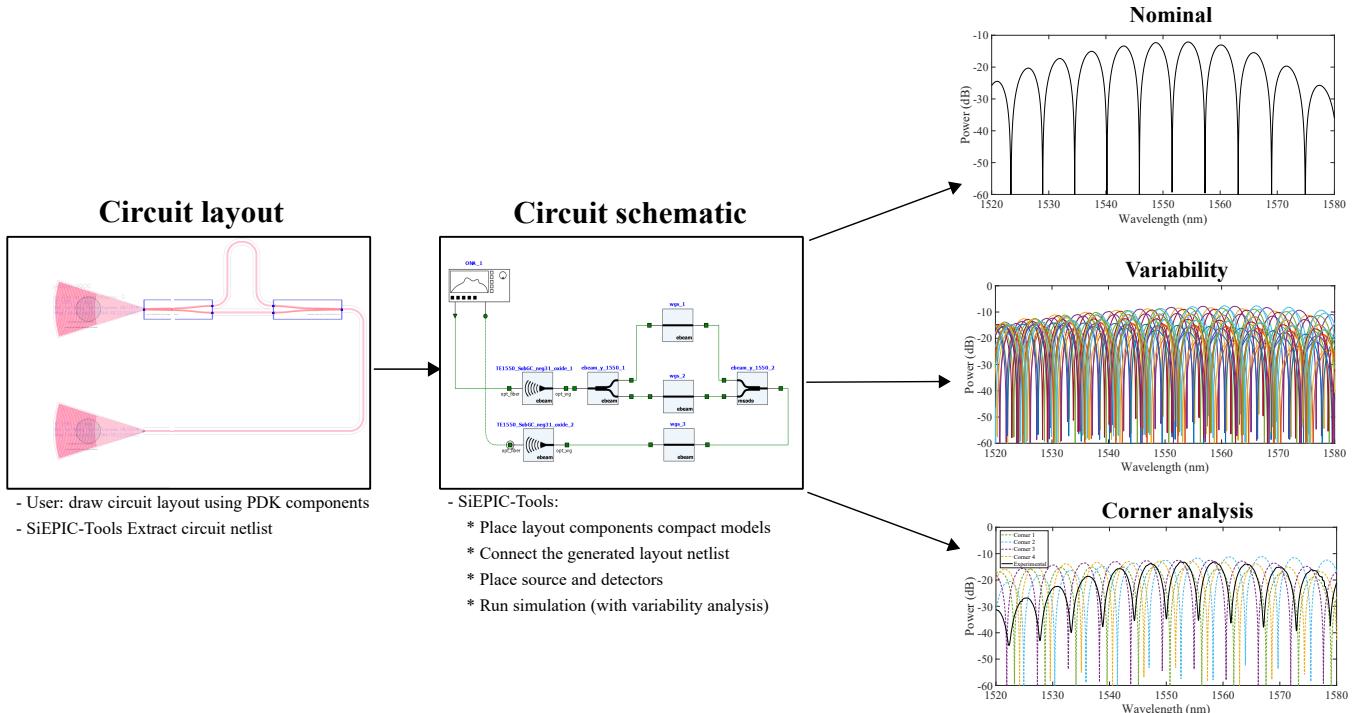


Fig. 17. Layout-to-circuit simulation flow in the SiEPIC-Tools PDK framework.

out a complex photonic neural network, script-driven design is necessary.

Scripting enables a complex and completely configurable hierarchy, which in this case, comprises of five levels. Every microring resonator (MRR) is slightly different, as is each subnetwork. Ascending the hierarchy involves abstraction of parameter concepts. The following example enumerates the parameters necessary to organize the circuit described in Fig. 19. Note that the parameters present in the lower-level PCells (e.g.  $w_{wg}$  in MRR) are carried over to the higher-level PCells (e.g. to WB), such that a parametric change in the top-level cascades down to the lowest level.

- 1) MRR: radius ( $R$ ), gaps ( $g_1, g_2$ ), waveguide width ( $w_{wg}$ );
- 2) Weight Bank (WB): initial radius ( $R_i$ ), radius increment ( $\Delta R$ ), number of MRRs (3), carry-over parameters from MRR (...);
- 3) Network: Interconnect topology (Broadcast or Star), number of weight banks (6), carry-over parameters from WB;
- 4) Test Array Structure: Contacts option: shared or inde-

pendent, carry-over parameters from Network;

- 5) Probe experiment setup: L-shaped electrical probe array with  $45^\circ$  rotation, stacked fiber GC array, with equal pitch matching the available probe dimensions, carry-over parameters from Test Array.

Abstraction is more easily represented in written codes than in gestural manipulations. Since the structure is entirely defined by code, high-level changes (e.g., number of neurons or pitch of the pads) involve simply changing one or two script variables and recompiling. Scripting accommodates changes, which also means that code modules can be pulled out and reused in changing situations. This includes different devices on the same chip, subsequent iterations of the rapid prototyping platform, or even completely different platforms.

The top hierarchical level illustrates breakout from the device ports to I/O pads and GCs. The semi-automated wire routing procedure here consists of three commands: a  $90^\circ$  group turn, a group fan-out, and then  $45^\circ$  and  $-45^\circ$  group

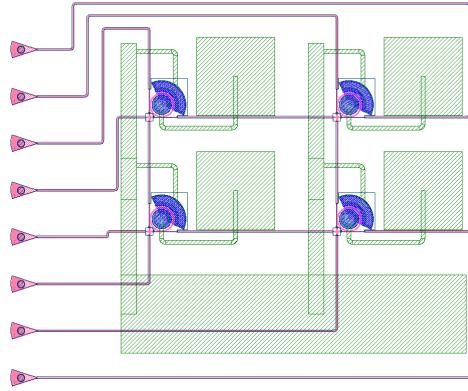


Fig. 18. Layout of a 2x2 optical switch, using four in-resonator photoconductive heaters for tuning and stabilizing each ring, where each heater-detector ring has a single contact, and they all share a common ground. The layout was created manually in the KLayout GUI. The same layout can be created procedurally using a script.

turns to connect at the pads<sup>1</sup>. The generalized autorouting problem is avoided through use of port constraints, discussed below. In the case of wire routing, in particular, high-level changes are frequently necessary during the design cycle. In the top right of Fig. 19c, it can be seen that a similar routing approach, produced by the same routing functions, is being used for a different type of circuit (out of frame).

These same semi-auto routing functions (turn, fan-out, connect, etc.) have been applied, with minor modifications, to platforms with multi-layer routing and with wirebonds instead of probe arrays. It is important to note that these functions are possible because the port locations are computed by the layout engine and are available as an attribute of the PCell object. This will be shown in the following example.

Fig. 20 shows the procedural routing approach using an open-access example available online [68]. Once a device cell (in this case, *MZI*) is created and its optical and electrical ports are defined, one can call general purpose procedures to change the location of these ports or to route optical and electrical netlists. These PCells were generated as follows:

```

1 from .cells import MZI
2
3 # fan to the right
4 MZI_FanRight = makeOpticFanRightCell(MZI)
5 # route to pads/GC
6 MZI_Experiment = makeExperimentCellA(MZI_FanRight)
7
8 # TOP is the top cell reference
9 # origin is the origin coordinate
10 # The following line draws the MZI_Experiment pcell
11 # with default parameters in TOP at position origin
12 MZI_Experiment('Cell_Name').place_cell(TOP, origin)

```

Listing 1. Source code of Fig. 20, available in Ref. [68].

The advantage in designing the final layout with Listing 1 is that these functions/classes are modular, reusable, and can be developed in parallel by different designers.

<sup>1</sup>Probe pad arrays are arranged at 45° to the V-groove fiber array so that two probe arrays, each taking 90° of azimuthal angle, can fit together.

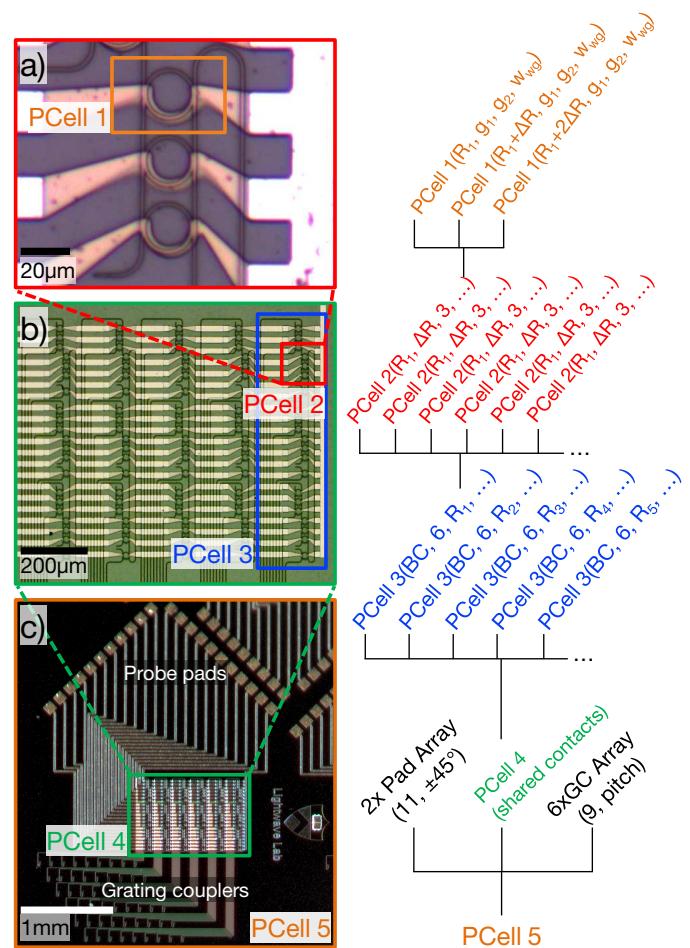


Fig. 19. A neuromorphic photonic system designed with procedural layout. It contains five hierarchical levels of embedded PCells (1-5). (a) Tunable microring weight (1) and weight bank (2) [65]. (b) Broadcast-and-weight network (3) and higher-order network (4) [66]. (c) Semi-automated routing to electrical I/O and optical I/O, forming the top level PCell (5).

As of version 0.26, KLayout is also available as a Python module that can be used within a stand-alone Python environment (e.g., Jupyter, Anaconda, Spyder), via the command “import klayout” (see [21, GitHub page]). It joins other Python-based open-source layout engines [69], [70], with the advantage that code and PCells can be reused for script-assisted GUI-driven layout (Section IV-B).

Script-driven layout for complex systems presents major advantages over hand-based and script-assisted layout, but it also carries major challenges. The conversion of code to a finished layout happens at the push of a button, which means the intermediate building progress is opaque during procedural generation, and the relationship between code changes and produced geometry is not obvious. Furthermore, script-driven layout inevitably has a steeper learning curve than hand-driven layout. It requires knowledge not only of photonics and geometry but of programming and software engineering; however, there is a strong movement in the open-source community to make these techniques and software available and to provide educational resources to beginners. Here, we mention two open-source packages recently released that attempt to address these issues.

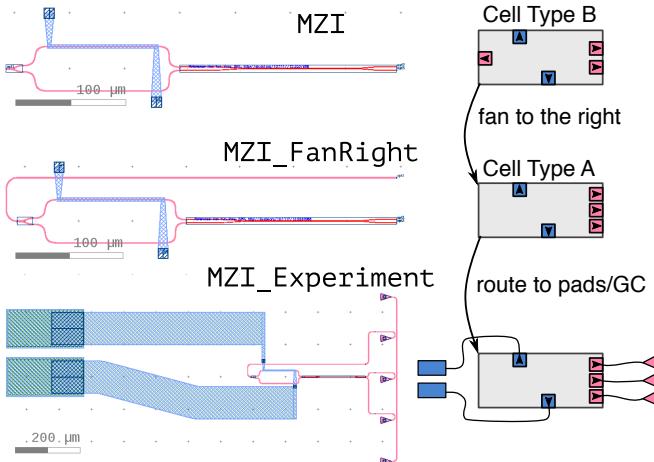


Fig. 20. Script-based cell transformation and routing. *MZI*, *MZI\_FanRight*, and *MZI\_Experiment* are all PCells defined in KLayout. *MZI\_FanRight* and *MZI\_Experiment* were generated automatically by general purpose routing functions.

*a) Debugging layout:* Shedding light on the internal build process involves debugging – stopping a build during runtime and examining the live state of variables. In normal code, we might be interested in an integer value changing in a loop. Layout code is different in that variables of interest are geometries; special tools are needed to visualize them while they are partially constructed. The KLayout application comes with an integrated development environment (IDE) for debugging layout scripts. The user can halt the code, then send a live “Cell” object to the main GUI window. An advantage of this method is that developed PCells remain compatible with hand-based layout in KLayout GUI. A user of this PCell would not necessarily need to do any programming. The SiEPIC-EBeam-PDK project includes a library of PCells that can be used either in a scripting or a manual GUI context.

For developing more complex code, one would often like to use a professional IDE such as Spyder and a full-featured debugger such as the Python Debugger (PDB), but then these are not connected to the KLayout application. This problem can be solved by creating an Inter-Process Communication (IPC) link between the KLayout GUI process and an outside layout generation process, which is done by the package “lyipc” [71]. Separating the processes means that the external language does not have to be based on KLayout’s Python API or even based on Python. Furthermore, processes do not necessarily have to be on the same computer. One can debug their code running on a remote, high-performance computer while visualizing its live geometry on their laptop.

*b) Testing layout correctness:* One cannot know what geometry will be produced by a particular layout script without running it. Complex layouts can consist of thousands of lines, and a change in one might have unintended side effects – a problem particularly threatening to collaborative design projects. Manual review is extremely cumbersome and only as good as the knowledge and eyes of the reviewer, plus there are usually hundreds of changes between reviews. In typical code projects, this issue is addressed by automated testing, in

which a set of tests is run every time a change is made. The test outputs are checked to ensure they produce the “correct” outputs, raising a flag if one does not. In layout code, the outputs are geometric, which raises the questions of how to specify the correct answer and how to perform the check. Layout geometries can be deemed equivalent when there are no shapes present in one but not the other – an XOR function. The correct answer can be a static layout file that has been examined by eye in the past.

The “lytest” [72] package combines the ideas of automated testing and XOR equivalency checking. It uses the KLayout XOR engine and the pytest unit testing framework, which can be integrated with git to run the tests on a cloud server upon every commit. lytest also works with lyipc, mentioned above, to provide visual feedback on any incorrect geometry elements. As a result, the following things can be known about a bug: its geometrical characteristics, the exact time it was introduced (and by who), and the lines of code that changed to produce it. In addition to debugging information, lytest can provide a constant guarantee of script-to-geometry correspondence, even as the test scripts and their supporting libraries change continuously. This type of guarantee is important in peer-to-peer collaborations and in foundry-to-user PDK exchanges. A PDK user can be assured that a tested PCell will not change, even if the PDK updates fluidly and the PCell function perhaps gains new features. The SiEPIC-EBeam PDK has recently incorporated lytest and has begun testing its building blocks.

#### D. Functional verification of circuits

While most foundries and design tools provide verification functionality in regards to manufacturability, in practice numerous errors associated with user designs are not related to manufacturing, but rather are related to functionality. Human-powered design review is generally needed to identify such errors, however, the following describes progress made towards automating the verification to include functional checks.

In this implementation, KLayout SiEPIC-Tools provides functional verification using Python functions, rather than a DRC script in the DRC-specific language. This allows for more complex rule creation, including loading parameters from XML files. A description of the implementation of netlist extraction and verification is provided in a previous publication [63]. The rules include:

##### a) Waveguide checks:

- The waveguide radius needs to be large enough, as specified in the PDK, to avoid excess insertion loss.
- Waveguide bends should have a sufficient number of points per circle. This is defined as ensuring that the deviation of the polygon with respect to a perfect curve is not larger than the database resolution (typically 1 nm).
- Manhattan check: The PDK is configured such that all connections to components are Manhattan (vertical or horizontal). Specifically, the first and last waveguide segment need to be Manhattan so that they can connect to device pins.

*b) Component checks:* Verify that the components are not overlapping. Each component includes a device extent polygon geometry (on the DevRec layer), and the script checks to ensure that no DevRec polygons are overlapping (touching is acceptable).

*c) Connectivity checking:*

- Disconnected pin: all component pins should be connected to other components or waveguides. Connectivity must be perfect, with the pins facing each other with the same angle (180 degrees), and with the same position (accurate to the user database unit).
- Mismatched pin widths: the waveguides need to be the same dimension (width) and type (e.g., strip waveguide).

#### E. Design for Test (DFT) verification

KLayout SiEPIC-Tools provides Design For Test rule verification. Similar to the Functional Verification, it is implemented using Python functions and allows for more complex rule creation. The existing code can be adjusted for different parameters, or modified and extended to deal with different DFT constraints (e.g., Design for Packaging constraints for bond-pad locations and pitch).

The EBeam PDK is configured for automated testing using fiber arrays aligned to vertical grating coupler 1D arrays. In principle, the rules could be modified for individual fibers, or edge couplers, and could be extended to include electrical test. Automated test is performed using automated probe stations, which are commercially available, e.g., from Maple Leaf Photonics.

The standard adopted for specifying test locations is to label each circuit under test with an “opt\_in” label. The label is formatted as opt\_in\_pol\_wav\_type\_deviceID\_parameters, where the polarization (pol) and the wavelength (wav), e.g., TE and 1550; type is for the automated probe station to know what type of device is being measured, e.g., “device”, deviceID is a user-specific device name, and parameters are optional fields for the user. The PDK configuration file, DFT.xml, lists what light source wavelength and polarizations are available, as well as the orientation of spacing of the fibre arrays.

Note that the “opt\_in” labels together with the design for test rules specified in DFT.xml are used to configure the circuit simulations; see Section III-G2.

- opt\_in label required: Labels must be on the layer “Text”.
- opt\_in label uniqueness: Automated test opt\_in labels should be unique. This makes the data analysis more straight forward if each device is uniquely labeled.
- opt\_in label location: Automated test opt\_in labels must be placed consistently in the layout, at the (0,0) point of the GC cell. One standard is to place them at the tip of the GC (the connection to the waveguide); another definition could be to place them at the fiber target location.
- opt\_in wavelength: verify that the wavelength source is available, as defined in the DFT.xml file.
- opt\_in polarization: verify that the polarization is available, as defined in the DFT.xml file.
- GC pitch: GCs must be placed on a specific pitch. The spacing, and the array direction (e.g., vertically arranged),

are specific to the test configuration. These are configured in the EBeam PDK to be 127  $\mu$ m for the edX course featuring EBeam fabrication.

- GC orientation: The GC needs to be oriented (rotated) the correct way for automated testing, and consistent with the alignment GCs used on the chip. In the edX course with EBeam fabrication, we use 0 degree rotation (tip pointing to the right) for the TE-polarized GC, “ebeam\_gc\_te1550”, and 180 degrees (tip pointing to the left) for the TM-polarized GC, “ebeam\_gc\_tm1550”.
- Fiber array configuration: The circuit must be connected such that there is at most X GCs above the opt\_in label (laser injection port) and at most Y GCs below the opt\_in label. For the tests performed for the edX course with EBeam fabrication, we use a four-channel fiber array, with the second fiber used for the laser injection, thus X=1 and Y=2.

## V. PACKAGING CHIPS FOR TESTING

Testing passive photonic chips can be done using an automated probe station. Simple active circuits with few electrical signals can be manually tested on a probe station. However, as the complexity increases, it becomes desirable to package the chip, namely make the optical and/or electrical connections to the chip to be permanent and robust. There are several packaging approaches reported in the literature, where each method has its merits and shortcomings. Due to the lack thereof standard packaging design rules [73] the choice of the best packaging approach is application- and cost-dependent [73], [74]. For instance, to fully leverage the CMOS compatibility advantages, automated packaging at high-volume using low-cost and robust techniques should be developed. This necessitates tackling some of the packaging challenges which can be divided into power-, speed-, and integration-based challenges [73].

Power challenges arise due to the coupling efficiency between the optical fibers carrying the data and the on-chip optical I/Os. On-chip optical I/Os are implemented either using an edge coupler or a surface grating coupler. A detailed description with the trade-offs brought by each from a packaging perspective can be found in Refs. [74]–[76]. Temperature control and management is another issue that adds to the overall power budget. Since optical packaging requires aligning the on-chip optical I/Os to the optical fibers, alignment at the micro level is required for optimum coupling efficiency, which can be time consuming (depending on the chosen approach) posing a speed challenge to the optical packaging and increasing the overall cost. Active alignment usually requires the use of shunt waveguides, a laser, and a photodetector [74]. This process can take up to tens of minutes per device; however, it has the merit of being more accurate compared to passive alignment, which does not require the use of a laser source for alignment, but uses a vision-based process instead. Passive alignment is a faster and more robust method, which usually takes < 3 times it takes for active alignment [77]. This comes at the expense of a less accurate alignment which would yield higher power losses

causing an increase in the overall power budget. Last but not least, integrating the laser, control electronics (drivers, amplifiers, and high-speed electronics), micro-lenses and isolators is also a challenge. Integration challenges can limit high-speed electrical signals or demand alternative ways to better manage the temperature control of both chips, depending on the chosen method, whether 3D integration using flip-chip bonding or 2.5D integration via an electrical interposer.

Choosing the best packaging approach can vary from application to another, however, regardless of the application, a detailed analysis shall be made to maintain a compromise between the trade-offs faced by the power, speed and integration challenges, which dictates the overall cost of the packaging approach selected. In an attempt to tackle the aforementioned challenges, Luxtera and Tyndall developed a micro-optic hybrid integration, where the laser is packaged using an edge-emitting laser and a micro-ball lens that focuses light onto a surface grating coupler [78]. Active alignment was then used to align the components together for efficient coupling. Once aligned, thermally conductive epoxy [79] was applied to hold the components in place and ensure proper heat dissipation from the laser diode to a thermo-electric cooler placed underneath the silicon photonic chip.

Here, we describe the packaging approach used for rapid prototyping of the active chips fabricated using the process described in Section II-E. We follow a similar approach (to Luxtera and Tyndall's) except that an external laser was used, thus we do not tackle the laser integration challenge. We demonstrate the packaging of the  $2 \times 2$  optical switch described in Section VI-C. However, optical filters, neuromorphic photonic processors, and larger optical switches could be packaged in a similar fashion.

#### A. Chip on carrier, and PCB

The fabricated chips were assembled and wirebonded to an 84-pin Kyocera ceramic quad flat non-leaded chip carrier (PB-C86131) as shown in Fig. 21a. These chip carriers have a high thermal conductivity to allow for heat generated on chip to be dissipated when a heat sink is attached from underneath. The chip carrier was placed in an 84-pin socket (AE11110-ND) and soldered to an FR-4 PCB (Fig. 21b). The PCB was placed on a 6-axis controlled stage, and connected to a source-measure circuit via jumper wires for electrical I/O (Fig. 21c).

The PCB, with carrier and chip, was placed on the automated probe station, to align to the fiber array. Laser light was launched into the devices on chip through single mode polarization maintaining (PM) fibers mounted in a  $127 \mu\text{m}$  pitch fiber array (See Fig. 21c). Two source-measure circuits consisting of 2 channel Keithley 2602 source-measure unit (SMU) were used, and controlled remotely by interfacing them with Python on a personal computer. Two devices were tested: a  $200 \mu\text{m}$  straight photoconductive heater, and a  $2 \times 2$  optical switch. We used a Keysight N7714A laser as the input light source for tuning, and an Agilent 81682A swept tunable laser and an Agilent 81635A photodetector to obtain the optical transmission spectra after tuning the  $2 \times 2$  switch.

#### B. Wirebonding

Ultrasonic wirebonding was performed using a wedge-wedge wirebonder. 1 mil ( $25.4 \mu\text{m}$ ) diameter aluminum bonding wire was used which necessitated a pad size of at least  $75 \mu\text{m}$  on the chip ( $100 \mu\text{m}$  pad sizes were used to avoid possible short circuits resulting from aluminum splashing). The wirebonding was performed at room temperature, using ultrasonic powers of 0.75 W and 0.525 W for the chip and chip carrier pads, respectively. The welding time was set to 10 ms and 15 ms, for the chip and chip carrier pads, respectively. The chosen powers and welding time were optimized until the wirebonds did not show any sign of nonstick, foot-lift or heel-break. Although a pull-strength test was not carried out, however, it is recommended to ensure optimum and reliable wirebonds [80].

#### C. Optical fibre packaging

Post characterization, the fiber array was glued using an ultraviolet (UV) glue and a UV gun. The glue was cured 5 times for 30 seconds per minute. The fiber array was stable and the PCB was packaged into a plastic box with fiber channel (FC) connectors. Fig. 22 shows the packaged PCB in steps. The electrical I/O to the chip can be supplied using a multichannel SMU source. This packaging approach was used to test multi-ring circuits and large channel count optical switches, as described in Ref. [81].

#### D. Packaging silicon-photonic biosensors

For biosensing, researchers have focused primarily on the design of sensing devices and their performance, while system-level integration of silicon photonic biochips has received less attention [82]. Hitherto, multiple functions including on-chip fluidic handling, electrical and optical analysis, and readout processing have been investigated for the chip-scale integration [83]. However, microfluidic and electrical/optical integration requires a relatively large silicon photonic die size (10-100 mm<sup>2</sup>), where most of the area only serves as mechanical support for the fluidic and liquid isolation of the optoelectrical I/Os [84].

The cost of silicon photonic chips scales with the size, thus to reduce costs, we have developed a system-level architecture with silicon die as small as 1 mm<sup>2</sup>, allowing complex microfluidic, electrical and optical integration [84]. Use used a lab-scale Fan-Out Wafer Level Packaging (FOWLP) process, where individual photonic and electronic dies can be encapsulated into 2-inch epoxy reconstituted wafers, and patterned with both electrical interconnects and microfluidic channels by standard photolithography. The experimental demonstration of FOWLP-packaged silicon photonic biochips indicates the potential for the commercial development of a system-level integrated sensing system for low-cost multiplexed diagnostics.

## VI. PHOTONIC CIRCUITS WITH ELECTRICAL CONTROL

#### A. Cascaded microring filters

Fig. 23 presents images of a cascaded microring add-drop filter made with rings of  $5 \mu\text{m}$  radius, and fabricated using

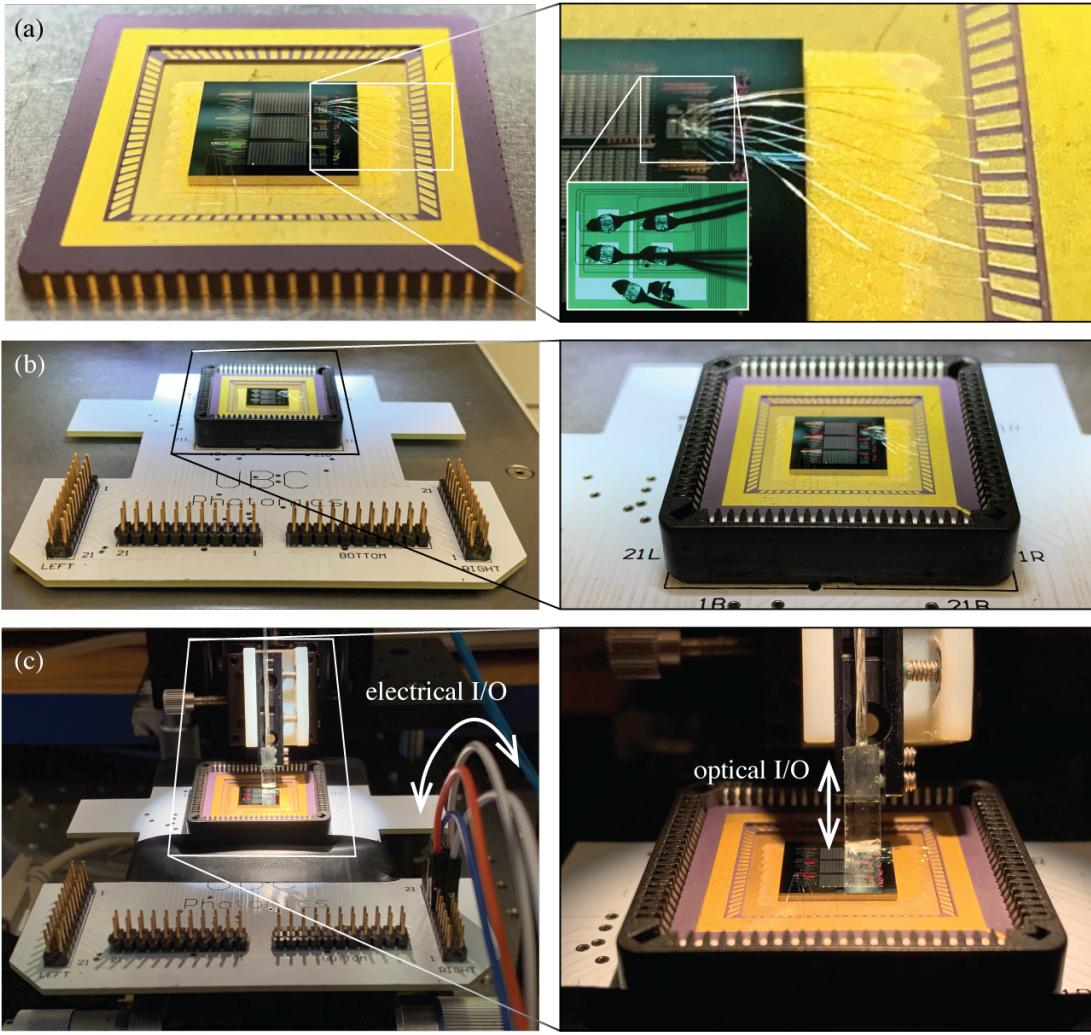


Fig. 21. Chip packaging for electro-optical testing. (a) The fabricated chips were assembled and wirebonded to an 84-pin Kyocera ceramic quad flat non-leaded chip carriers (PB-C86131). The inset shows a zoomed-in view of the Al bondwires connecting the switch pads on the chip to the chip carrier. A further inset shows a top view of the bondwires bonded to the 5 pads of the  $2 \times 2$  optical switch. (b) The chip carrier placed in an 84-pin socket (AE11110-ND) and soldered to an FR-4 PCB. The inset shows a close-up view of the chip carrier placed in the socket. (c) The PCB placed on a 6-axis controlled stage, and connected to a source-measure circuit via jumper wires for electro-optic testing. The inset shows a close-up view of the 8-port 127  $\mu$ m-pitch PM fiber array for optical I/O.

the process described in Section II-B. These devices are very sensitive to non-uniformities in the fabrication process as well as to thermal variations in the environment. To compensate for those effects, a resonance tuning mechanism for each microring is mandatory. Integrated metal micro-heaters with small feature size were used to tune the phase of each resonator. The transmission spectrum presented in Fig. 23c shows the response of a similar cascaded microring filter with 2.5  $\mu$ m radius, as-fabricated, as well as after tuning. With such small rings, the free spectral range is measured to be 37.15 nm, which is large enough for wavelength division multiplexing (WDM) applications in the C-band. The misalignment of each individual microring caused by manufacturing process variations is a limitation but proper tuning is made possible by the integrated micro-heaters. After tuning, all rings can be aligned to the same central wavelength as shown which reduces the 3 dB bandwidth to 35 GHz.

### B. Photoconductive detectors

Doping silicon waveguides allows for the direct detection of light (through surface and defect states, and the photoconductive effect) and manipulation of the optical phase of light (through heating the silicon waveguides) [23], [81], [85]. This allows a system to compensate for fabrication errors and enables large and dense systems integration that rely on the accurate control of light in the chip [81], including neuromorphic circuits [11]. We demonstrate the photoconductive effects of 200  $\mu$ m long silicon photoconductive detectors (shown in Fig. 24a) fabricated using the active process described in Section II-E, and show their integration into a  $2 \times 2$  ring-based optical switch to yield the desired tuning state.

Fig. 24b shows the dark current of the 200  $\mu$ m photoconductive heater across the voltage applied. The current saturates at higher voltages due to the drift-velocity saturation at high electric fields. Fig. 24c shows the (differential) photocurrent detected at various bias applied across the 200  $\mu$ m-long straight

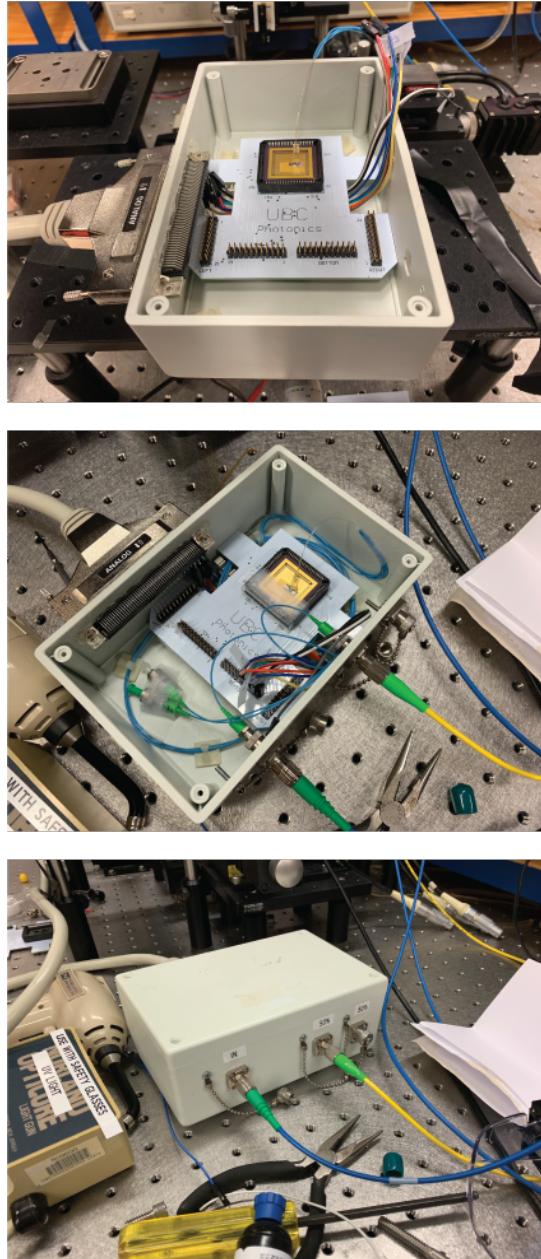


Fig. 22. Packaged silicon photonic chip. The optical I/O is provided through the glued fiber array.

photoconductive heater, when the input optical power to the device was set to 4.5 mW. The (differential) photocurrent is calculated as the difference of the current of the photoconductive heater when the laser is turned on less the dark current. While the photocurrent increases at larger bias voltages due to a larger gain resulting from shorter electron transit time between the two terminals, this comes at the expense of a larger dark current and higher noise [86] as shown in Fig. 24b. In order to more accurately measure the photocurrent and responsivity, the photoconductive heater was biased to 2.8 V, and the photocurrent was measured across various input optical powers. The photocurrent and calculated responsivity are shown in Fig. 24d. The  $\pm 3\sigma$  value for each optical input power was calculated from 100 photocurrent measurements

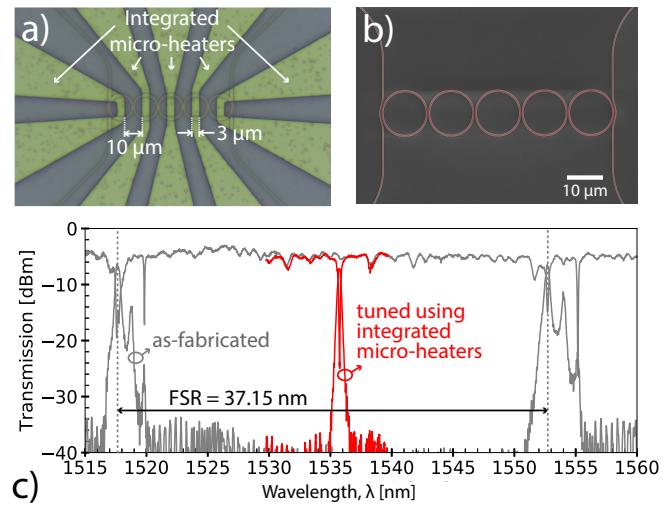


Fig. 23. Fifth-order cascaded microring resonator add-drop filter (MRF). (a) Image of the integrated micro-heaters for a MRF with microrings of radius 5  $\mu\text{m}$  showing features of small size on the metal layer. (b) SEM image of MRF of radius 5  $\mu\text{m}$ . (c) Spectral response of a 2.5  $\mu\text{m}$  MRF as-fabricated (misaligned) and after tuning using integrated micro-heaters.

at each input optical power to the device. Thus we show the photocurrent and calculated responsivity for measurements above the measurement noise floor (at optical input powers  $> -20\text{dBm}$ ). We operated the detector over a range of -5 dBm to +5 dBm during our control stabilization experiments, hence the dynamic range is at least 10 dB.

### C. Ring-based optical switch

Microrings are attractive key elements in photonic circuits. They can be found in a plethora of applications, from biosensing, quantum information, neuromorphic processing, machine learning and communications. They can also be useful for data centers, where they can be arranged to form a switch matrix to route light across different ports. Here we show an application of a ring-based system, and test the applicability of the photoconductive heaters to precisely monitor and route light between the ports of a  $2 \times 2$  ring-based optical switch, as shown in Fig. 18 and 25. Fig. 26a shows an optical microscope image of a switch cell. The microring had a radius of 15  $\mu\text{m}$  and a core width of 500 nm. Fig. 26b shows the optical transmission (at the cross port) and the (differential) photocurrent as a function of the photoconductive heater electrical power. Since the photocurrent and optical intensity maxima are aligned at the same heater power, the photocurrent can provide a means to tune the microring and route the light between the different switch ports through setting the switch cell to on-resonance (bar state) and off-resonance (cross state), when the photocurrent is maximized or minimized, respectively [81], [87]. Fig. 27 shows the optical spectrum of the as-fabricated response of the optical switch, as well as the optical spectrum of the tuned switch in the staircase. The tuning algorithm that was implemented is similar to the one described in [81], where only rings 1, 2 and 4 were tuned on-resonance at the set laser wavelength of 1551 nm.

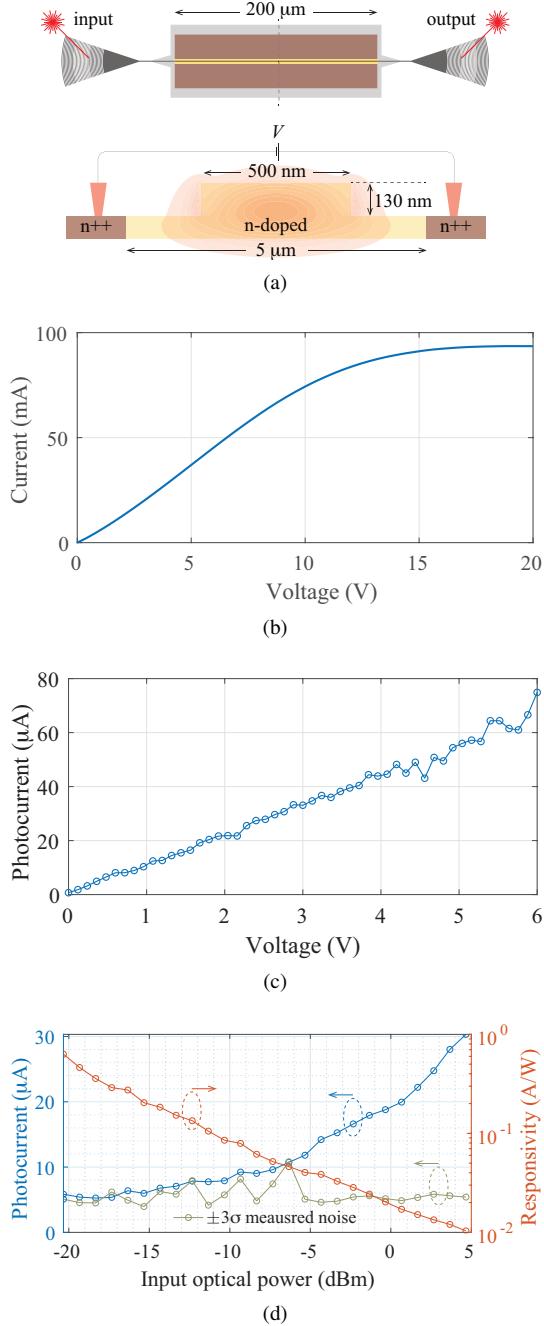


Fig. 24. Photoconductive measurements. (a) Layout (top and cross-section views) and (b) dark current of the 200  $\mu\text{m}$  photoconductive heater across the voltage applied. The current saturates at higher voltages due to the drift-velocity saturation at high electric fields. (c) Photocurrent across the heater's bias voltages at an input optical power of 4.5 mW at 1550nm. (d) The photocurrent and calculated responsivity of the photoconductive heater across various optical powers. The  $\pm 3\sigma$  measured noise is also shown.

## VII. ANALYSIS AND FUTURE WORK

### A. Overlay accuracy of doped regions

Selective masking of dopants for the in-resonator photoconductive heaters was performed with photolithography using a manual mask aligner. The overlay accuracy of the mask openings is therefore limited by the ability of the operator and tool to manually align marks on the photomask to the silicon layer. Typically this overlay accuracy is on the scale

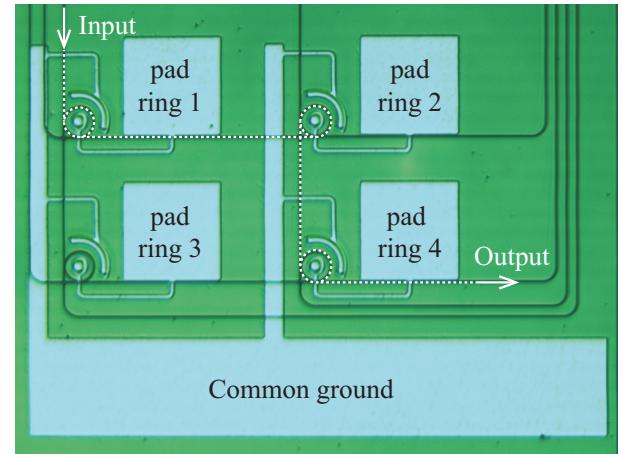


Fig. 25. Optical microscope image of a  $2 \times 2$  ring-based optical switch showing the staircase path along which light is routed. This is achieved by tuning rings 1, 2 and 4 on-resonance through maximizing their photocurrents.

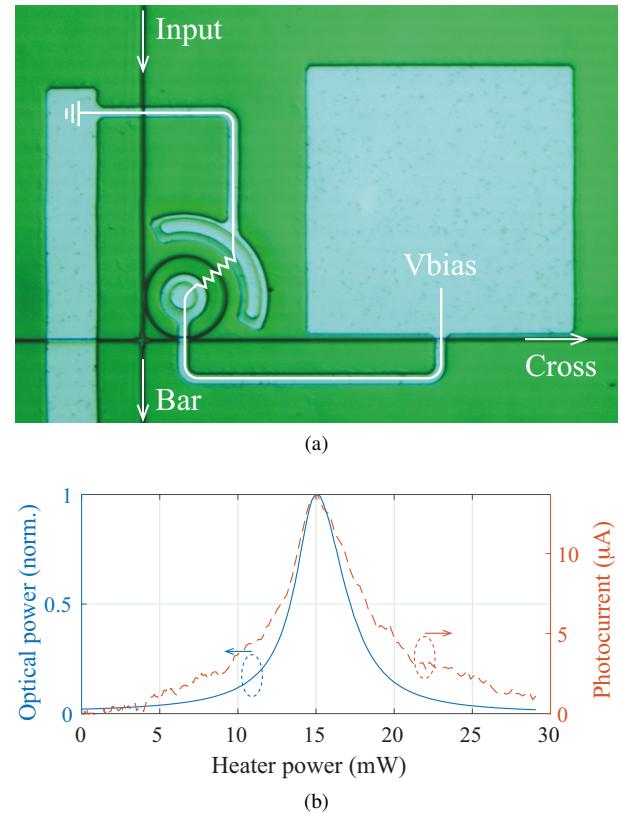


Fig. 26. (a) A single unit cell of the  $2 \times 2$  ring-based switch shown in Fig. 25, indicating the 2 switch states, bar: when the ring is off-resonance, and cross: when the ring is on-resonance. (b) Optical transmission in the cross state, and photocurrent measured when biasing the photoconductive heater at various voltages. The photocurrent is maximized when the ring is on-resonance with the laser frequency.

of 1 to 2  $\mu\text{m}$ . Improvement in the overlay accuracy of these doped regions allows for more compact placement of the doped regions which can increase the photoconductive gain, thus improving the photoconductor's responsivity and overall quantum efficiency. For instance, similar measurements were performed on devices that were fabricated with a 60 nm overlay accuracy (2  $\mu\text{m}$  separation between the high doping

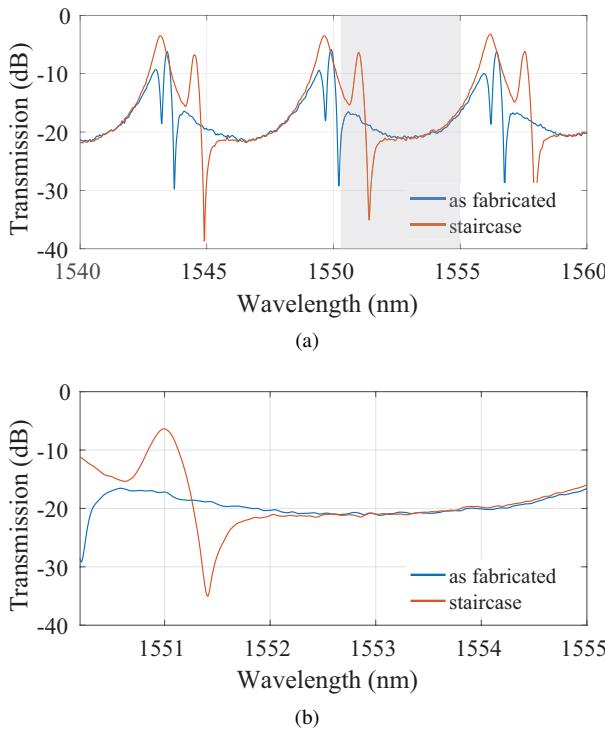


Fig. 27. (a)  $2 \times 2$  ring-based optical switch spectrum, as fabricated, and post tuning the rings to the laser's wavelength at 1551 nm in a staircase fashion. (b) A zoom-in of the shaded region in the spectrum in (a).

regions instead of the  $5 \mu\text{m}$  separation shown here) in an MPW foundry [81], showing a  $5 \times$  greater photoconductive gain.

Automatic patterning techniques such as EBL and direct-write laser lithography can achieve improved overlay accuracy compared to manual alignment, but each of these techniques has benefits and drawbacks. Direct-write laser lithography can pattern thick masks that are well-suited for blocking dopants during the implantation process, but is limited in overlay accuracy to approximately 200 nm [88]. EBL can achieve superior  $3\sigma$  overlay accuracy as low as 20 nm [89], however the e-beam resist must be spin-coated thinly enough to reliably resolve alignment marks through the resist but also be thick enough to block dopants from reaching the silicon during implantation. EBL is also an expensive process that is limited in speed when patterning large regions. A hybrid approach of e-beam patterning for layers with tight overlay tolerance and lower dopant concentration (such as p-n junctions in modulator devices) and direct-write laser patterning for heavily-doped contact regions may be appropriate for rapid and economical prototyping of active photonic circuits.

### B. Broader Impacts of an Open-Source PDK

The design approaches pioneered by the SiEPIC-EBeam PDK have been adopted by other silicon photonic MPW services. Recently, the National Institute of Standards and Technology (NIST) released a PDK describing their superconducting optoelectronic networks (SOEN) platform [90]. The SOEN platform is designed for cryogenic neuromorphic photonics [91] and quantum optics applications. It combines superconducting nanowire single-photon detectors

(SNSPDs) [92], nanocryotron (nTron) amplifiers [93], and all-silicon light sources [94]. NIST's SOEN PDK follows the format of SiEPIC's EBeam PDK such that it integrates with KLayout and benefits greatly from the design tools described in Section IV. The fact that unaffiliated MPW enterprises are adopting the SiEPIC PDK format evinces its value, accessibility, and extensibility. It furthermore suggests that others, perhaps even foundries, could come to improve their PDKs by adopting principles of the SiEPIC PDKs.

## VIII. CONCLUSION

In conclusion, rapid prototyping fabrication of passive and active photonic integrated circuits, where the performance and process parameters are similar to foundries, allows one to prototype not only individual components, but also complex systems. After demonstrating novel functionality, the design can be translated to a high-volume manufacturing foundry.

The design of photonic integrated circuits is supported by a process design kit. The SiEPIC-EBeam-PDK for electron beam lithography-based fabrication has numerous components with excellent performance, and the library is publicly available in an open-source manner to which external users can contribute.

The KLayout design tool, with SiEPIC-Tools and the SiEPIC-EBeam-PDK, which are open-sourced, allows for GUI-based layout and procedural script-based layout. This environment makes it easy for new users to get started, and is also scalable to design teams building complex systems such as neuromorphic photonic processors and optical switches discussed here.

The layout flow based on parametric design with tools such as KLayout and SiEPIC-Tools offers comprehensive functionality while being flexible to custom modifications by virtue of being open-source. Essential features include native support of PCells, editing macros, DRC, native support of a modern programming language (Python), unit testing, functional verification, and circuit simulations from a physical layout. The last four in particular are not readily available in commercial tools, but are key to enable large-scale photonic integrated circuit design in an efficient and cooperative manner. Widely available open-source tools leverage great value from an ample knowledge base, community support, and community collaboration.

## APPENDIX A MASK DATA PREPARATION

This section describes the data processing that takes places on the designer's layout (e.g., GDS file). This processing is performed by the foundry (or mask shop), and normally the designer is neither involved nor aware of this step.

After a design is completed, the design data must be prepared for the intended exposure tool, whether that be a direct-write EBL tool or a mask-making system for optical lithography. A key process in this data preparation step is the decomposition of the design data into low-level primitive shapes which can then be written by the lithography tool. In this data processing step, generically called "fracturing",

the capabilities and writing parameters of the writing tool must be considered, so that the on-wafer pattern is as close as possible to the designer's intent. Tool parameters such as the available primitive writing shapes, the data placement grid, and the writing increment grid all must be taken into account for best results. In the case of EBL, compensation for proximity effects must also be applied. And importantly, the common design data interchange formats such as GDS-II do not directly support curved shapes, which instead must be piece-wise approximated by multi-segment polygons. In sum, the data preparation tasks are complex, and it has been shown the careful attention and optimization of parameters can result in significant performance improvements for photonic devices.

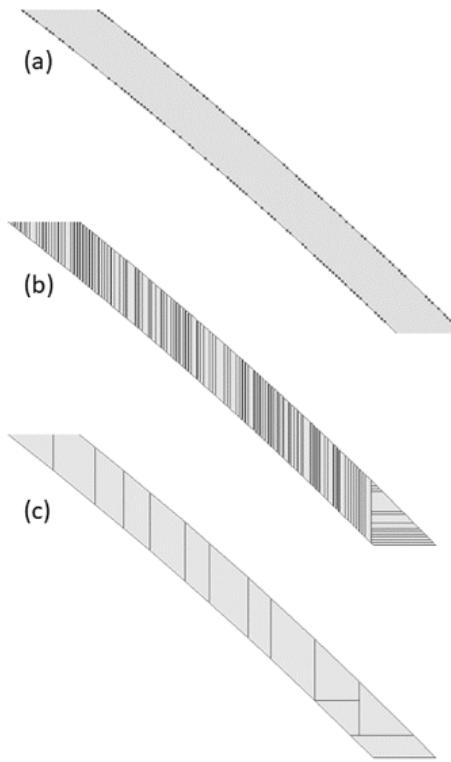


Fig. 28. A segment of curved waveguide in (a) CAD format (GDS-II), as a polygon representation of a curve, with polygon vertices shown, (b) EBL writing format with conventionally fractured Manhattan primitives, and (c) EBL writing format with intelligently fractured polygons using a curve recreated from the polygon approximation, and awareness of the writing tool's grid.

For example, consider the waveguide segment illustrated in Fig. 28. Inset (a) shows the vertex placement from a typical CAD drawing of a curved arc segment, while (b) shows this design when fractured to e-beam writing primitives using a conventional Manhattan algorithm which considers each digitized vertex to be an intended point in the approximating polygon. The writing of this waveguide will be less than optimal on e-beam writing tools in that the extra shapes both increase the waveguide edge roughness due to shape placement jitter, and the writing time overhead is increased from additional overhead of additional shapes. The same waveguide segment fractured using a modern, tool-aware curved fracturing algorithm is shown in inset (c); the reduction

in shape count with no loss in edge accuracy from the original curved design is immediately apparent.

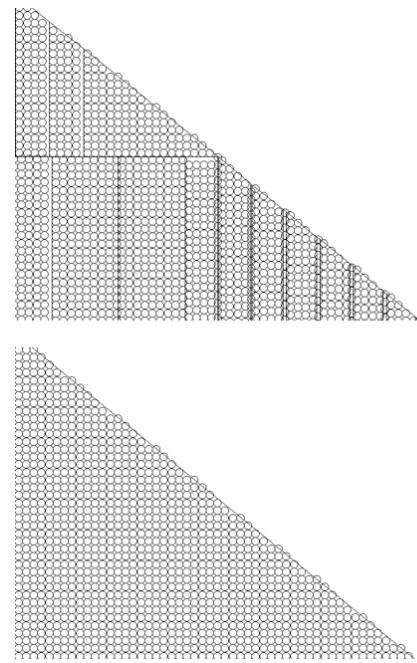


Fig. 29. EBL pixel placement for writing without (top) and with (bottom) intelligent fracturing considering the tool writing grid.

On an even finer dimensional scale, but also of significant effect on waveguide sidewall roughness, the tool writing parameters must be considered when fracturing into primitive shapes. Fig. 29 shows a closeup of one edge of the waveguide segment, with the placement of each pixel (beamstep) in the e-beam writing sequence drawn, for an 8 nm beam step spacing, typical conditions for higher-speed direct-write EBL. Inset (a) shows the pixel placement for a conventional, Manhattan fracturing technique which does not take into account this 8 nm stepping, and the resulting non-uniform placement of the beam shots, with gaps and overlapping pixels noted, as well as non-uniform shot placement along the waveguide edge, which is most sensitive to writing nonuniformities. Inset (b) shows the same segment when fracturing with a curved algorithm and with knowledge of the intended 8 nm pixel spacing for writing. In this case, the data is intelligently fractured to both avoid the non-uniformities in pixel placement by ensuring that all primitive shapes are sized an integer multiple of the 8 nm beam step spacing, which also results in more uniform shot spacing along the waveguide edge.

Beyond the basic fracturing techniques just described, more advanced pattern data processing techniques have shown improvement in performance of photonic devices. Large reductions in waveguide loss patterned by direct-write EBL have been shown by application of a multi-pass writing strategy, in which the designs are over-written multiple times, with each pass being written with a dose of a proportional fraction of the total writing dose [13]. Multi-pass writing effects temporal averaging in the writing, to reduce some time-varying noise effects. Further improvements are seen by also shifting the e-beam write field between the passes, effecting spatial

averaging to reduce effects of position-dependent aberrations such as field-stitch boundaries. In that study, the application of 2-pass writing with a 50% field shift between passes showed a reduction in loss in straight waveguides from -4.2 dB/cm to -3.3 dB/cm, and for curved waveguides from -12.6 dB/cm to -9.3 dB/cm. The improved photonic performance is attributed to smoothing of the structure edges by reducing lithographic noise by the averaging effect of the multiple beam-writing passes.

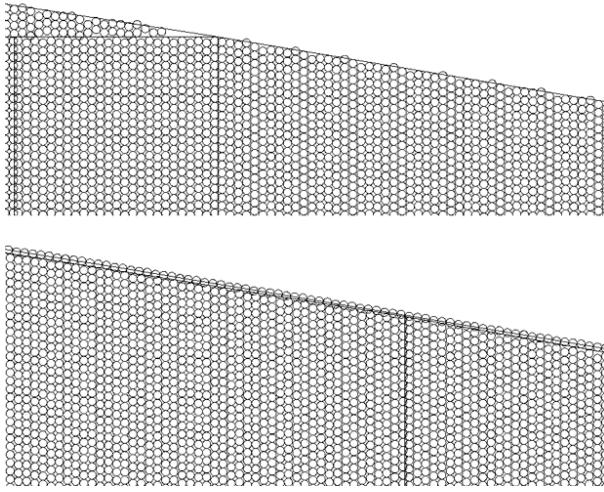


Fig. 30. Close-up depictions of pixel placement at waveguide edges for Normal (top) and SLS (bottom) writing strategies.

More recently, an additional advanced fracturing technique has shown even further reduction in waveguide loss, by using an advanced fracturing technique which places a special, tool-specific single-line EBL primitive shape along the outer waveguide edges [27]. This technique reduces the lithographic edge roughness due to individual pixel placement variation due to the all-angle property of the single-line primitive, as illustrated in Fig. 30. When applied in addition to the multi-pass writing described above, this Single-Line Smoothing technique demonstrated a further reduction in waveguide loss of 0.5 dB/cm for straight waveguides and 1.5 dB/cm for curved waveguides.

The seemingly simple task of converting design data from CAD format to machine-specific format for fabrication has been shown to have significant effects on final device performance, and as such, the data fracturing techniques and parameters used should be carefully considered. The fracturing operations work best when matched with the writing capabilities and parameters of the exposure tool to be used.

Not described in this section, there are additional data preparation steps prior to patterning the resist. One of the most important is proximity correction, to compensate for feature size changes due to the local pattern density.

#### ACKNOWLEDGMENT

The authors would like to thank JEOL for the rapid commissioning of the electron-beam lithography tool, staff at the

UBC Stuart Blusson Quantum Matter Institute Nanofabrication Facility who facilitated the tool installation, and CMC Microsystems for providing access to Mentor Graphics tools.

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