Reliability Analysis of a Delay-Locked Loop Under HCI and BTI Degradation

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***Abstract*—This paper studies the impact of hot carrier injection and bias temperature instability on a mixed-signal delay locked loop, at the block and system levels. Aging affects delays on the reset line of the phase detector, degrading sensitivity to input phase differences. Aging also increases threshold voltage mismatch in the charge pump, causing the control voltage of the voltage-controlled delay line to drift, reducing the acquisition time. Numerical results on a 45nm CMOS process are presented.**

I. Introduction

While there has been much research on aging in digital circuits, analog/mixed-signal (AMS) circuit aging has received less attention. AMS circuits are more susceptible to variation than digital circuits and are increasingly integrated into performance-critical systems. Due to the presence of feedback loops, the impact of bias conditions, and sensitivity to reactive components, an analysis of aging on the performance of AMS circuits differs from that of digital designs and requires in-depth circuit-specific understanding.

Prior efforts have analyzed the aging-induced performance degradation of AMS modules, including standalone analog blocks [1], low noise amplifiers (LNAs) [2], LC oscillators and phase-locked loops [3], and current-starved voltage-controlled delay lines [4]. Much of the past work has been confined to the analysis of relatively small, isolated blocks. In general, these works fail to clearly separate the impact of bias temperature instability (BTI) and hot-carrier injection (HCI), which could provide insights to counter aging.

In this work, we use a representative circuit to show how aging can be analyzed at various hierarchical levels of an AMS design. We address the problem of aging in delay-locked loops (DLLs), a critical component of high-speed blocks, used in circuits for clock/data recovery, clock generation, frequency synthesis, and signal synchronization. We present a structured and comprehensive study of the effects of BTI and HCI on a DLL architecture (Fig. 1). Functionally, a DLL delays an input signal S_{ref} by a clock cycle to produce an aligned output signal S_0 using an architecture that includes:

- a phase detector (PD) that compares S_0 with the S_{ref}, and outputs *Up* and *Dn* that indicate the phase relation.
- a charge pump (CP), which uses *Up* and *Dn* to generate voltage $V_{control}$ and drives a capacitive loop filter (LF).
- a voltage controlled delay line (VCDL) whose delay is adjusted, depending on the value of $V_{control}$.

Transistor aging degrades the precision of a DLL over time by increasing the misalignment between S_{ref} and S_0 at steady state. Over time, this could make the DLL inoperable. We investigate the effect of aging on a DLL at multiple levels of hierarchy: individually on each component of the DLL, and then on the DLL as a whole. We identify blocks and transistors of the circuit that are more susceptible to aging effects to provide insights that can guide optimization. Although we address DLLs specifically in this work, the components that we study are often used as building blocks of other structures. Moreover, our approach systematically considers the impact of feedback loops with constraints on timing and voltages in mixed digital/analog subcircuits.

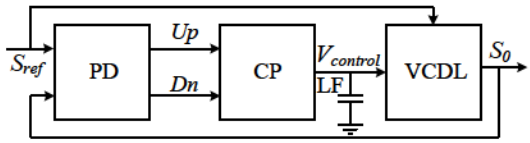

Fig. 1. Block diagram showing the architecture of a DLL.

II. Aging in DLL circuits

We discuss reliability concerns for each module of the DLL, showing the impact of aging (under device aging models described in the Appendix), based on 45nm NCSU MOSFET parameters at room temperature, a 1V power supply, and an S_{ref} clock period, $T_{clk} = 1$ ns [5].

We consider a worst-case switching excitation, where S_{ref} always leads S_0, or vice versa. In normal operation, this may not happen as the signals lock, but it is a realistic worst-case scenario, e.g., as a viable side-channel attack from a malicious actor to cause excessive DLL aging and system failure.

A. Phase detector (PD)

Transistor aging forces the pulse width difference of the output signals of the PD to be sensitive to the internal gate delays. Intuitively, PD failure may be caused due to delay changes on internal feedback paths. This subsection illustrates the process.

Circuit structure The architecture of the PD (Fig. 2(a)) shows an interconnection of digital logic gates with feedback [6]. The gate pairs (G_5, G_6) and (G_7, G_8) form a pair of set-reset (SR) latches labeled as L_1 and L_2, respectively. The circuit is symmetric about an imaginary horizontal line through its middle: the pairs (G_1, G_2), (G_3, G_4), (G_5, G_8), (G_6, G_7), (G_{10}, G_{11}), (G_{12}, G_{13}), and (G_{14}, G_{15}) are ideally identical. The gates are designed to have equal rise and fall times. Hence, the paths from S_{ref} and S_0 to G_9 are similar.

The PD generates two output signals, *Up* and *Dn*, that switch from their steady state value of logic 0 to logic 1 when they sense the positive edges of S_0 and S_{ref}, respectively. These pulses go low, ideally simultaneously, by an active-low *Reset* signal, generated when phase detection is complete. The circuit then awaits the next edge of S_{ref} and S_0. The relative pulse width of *Up* and *Dn* indicates the lag-lead relation as well as the phase difference between S_{ref} and S_0: if the pulse width for *Dn* is larger than that for *Up*, then S_{ref} leads S_0.

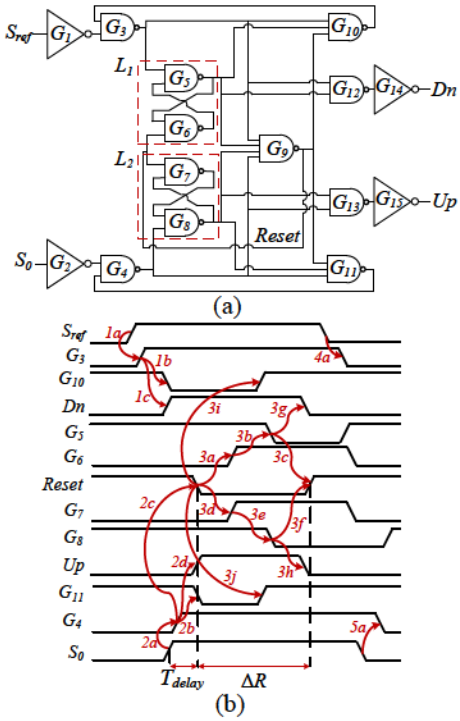

Fig. 2. (a) Block diagram and (b) timing diagram for the PD.

Operating principle Initially, *Up* and *Dn* are both low. We assume S_{ref} leads S_0 (Fig. 2(b)); the opposite case is analogous.

Initially, prior to the edge on S_{ref} or S_0, when both signals are low, they are complemented by G_1 and G_2. We temporarily assume that G_{10} and G_{11} are high (and later show this to be self-consistent): as a result, G_3 and G_4 are low. The outputs of G_5, G_8, G_{10} and G_{11} are thus high, confirming our assumption. Due to the SR latch behavior of L_1 and L_2, G_6 and G_7 are low, so that the *Reset* signal from G_9 is high. The signals *Up* and *Dn* are both initially low due to the logic value of G_4 and G_3, respectively. The initial gate outputs are:

G_1 G_2	G_3 G_4	G_5 G_8	G_6 G_7	G_{10} G_{11}	G_{12} G_{13}	$G_{14}(Dn)$ $G_{15}(Up)$	G_9 (*Reset*)
1	0	1	0	1	1	0	1

The circuit operates as follows when S_{ref} precedes S_0:

Step 1: The positive edge of S_{ref} propagates through G_1 and pulls G_3 high. Since all inputs of G_{10} are now high, its output switches from high to low, thus locking G_3 at high. With both inputs to G_{12} high, *Dn* switches to high. Symbolically, denoting a rising edge as $\uparrow$ and a falling edge as $\downarrow$, this corresponds to the following labeled transitions in Fig. 2(b):

$$S_{ref}\uparrow \xrightarrow{1a} G_3\uparrow; G_3\uparrow \xrightarrow{1b} G_{10}\downarrow; G_3\uparrow \xrightarrow{1c} Dn\uparrow$$

Step 2: The system changes at the $S_0\uparrow$. Analogous to Step 1, $S_0\uparrow$ traverses G_2 and G_4 and lowers G_{11}, locking G_4 to high. As both inputs to G_{13} are high, *Up* also goes high. Now that all inputs to G_9 are high, *Reset* goes low. These are seen in the figure as:

$$S_0\uparrow \xrightarrow{2a} G_4\uparrow; G_4\uparrow \xrightarrow{2b} G_{11}\downarrow; G_4\uparrow \xrightarrow{2c} Reset\downarrow; G_4\uparrow \xrightarrow{2d} Up\uparrow$$

Step 3: As *Reset* falls low, it triggers events that ready the PD for detecting the next edge on S_{ref} or S_0. Specifically, G_6 and G_7 rise to high, allowing G_3 [G_4] to propagate through G_5 [G_8]. A low signal on any one of G_3, G_4, G_5 and G_8 is sufficient to switch *Reset* back to high, thus returning the PD to the initial state. After G_5 and G_8 go low, *Up* and *Dn* revert to low. As *Reset* falls, G_{10} and G_{11} also rise to high. Besides, as G_5 and G_8 change to low, G_{10} and G_{11} stay high even after *Reset* rises to high. This allows S_{ref} and S_0 to propagate through G_3 and G_4, respectively, again. In the figure,

$$Reset\downarrow \xrightarrow{3a} G_6\uparrow \xrightarrow{3b} G_5\downarrow \xrightarrow{3c} Reset\uparrow; G_5\downarrow \xrightarrow{3g} Dn\downarrow$$
$$Reset\downarrow \xrightarrow{3d} G_7\uparrow \xrightarrow{3e} G_8\downarrow \xrightarrow{3f} Reset\uparrow; G_8\downarrow \xrightarrow{3h} Up\downarrow$$
$$Reset\downarrow \xrightarrow{3i} G_{10}\uparrow; Reset\downarrow \xrightarrow{3j} G_{11}\uparrow$$
$$S_{ref}\downarrow \xrightarrow{4a} G_3\downarrow; S_0\downarrow \xrightarrow{5a} G_4\downarrow$$

A second path to *Dn* goes from *Reset* through G_{10}, G_3 (if $S_{ref} = 0$), G_{12} and G_{14}; a symmetric path exists for *Up*. Under perfect symmetry, *Up* and *Dn* go down together.

Impact of aging We consider the worst-case switching activity scenario for PD aging, when one signal always leads another. As before, we consider S_{ref} leading S_0; the opposite case is analogous. The effects of aging on the PD cause:

(i) **Reduced operating frequency**: The key timing parameters for the PD (illustrated in Fig. 2(b)) are (1) propagation delay, T_{delay}, between the later of $\{S_0\uparrow, S_{ref}\uparrow\}$ and *Reset*$\downarrow$, and (2) pulse width ΔR of the *Reset* signal. These two parameters place an upper bound on the allowable frequency of S_{ref}, which degrades with time as aging increases gate delays. Our simulations, to be summarized in Fig. 3, show that the reset operation takes 42.6% more time to complete after 10 years.

When S_{ref} leads S_0, T_{delay} is activated by the path $S_0\uparrow\rightarrow G_2\downarrow\rightarrow G_4\uparrow\rightarrow G_9\downarrow$. BTI aging slows down the PMOS transistors while HCI slows down the NMOS transistors. Both the fall time and rise time of the gates increase, causing higher T_{delay}. In the short term, BTI degradation is much higher than HCI (Fig. 3(a)), but over time, HCI becomes significant (since $n_{hci} > n_{bti}$), and the T_{delay} envelope is shaped by HCI.

The same observation is also true for ΔR in Fig. 3(b). HCI aging is more significant in ΔR compared to T_{delay} as ΔR has higher dependence on fall transitions, and the slew of S_0 is sharper than that of *Reset*. The *Reset*$\downarrow$ signal triggers switching events in L_1 and L_2 that cause *Reset* to eventually rise through paths *Reset*$\downarrow\rightarrow G_6\uparrow, G_7\uparrow\rightarrow G_5\downarrow, G_8\downarrow\rightarrow$ *Reset*$\uparrow$, irrespective of the lag-lead relationship between S_{ref} and S_0.

(ii) **Increased PW_{Up} and PW_{Dn}**, which are the pulse widths of *Up* and *Dn*, respectively: Since the rising edge of each of *Up* and *Dn* propagates through fewer gates than its falling edge, for similar aging for each gate, PW_{Up} and PW_{Dn} increase.

(iii) **Changed difference between PW_{Up} and PW_{Dn}**: The relative pulse widths indicate the lead/lag relationship between

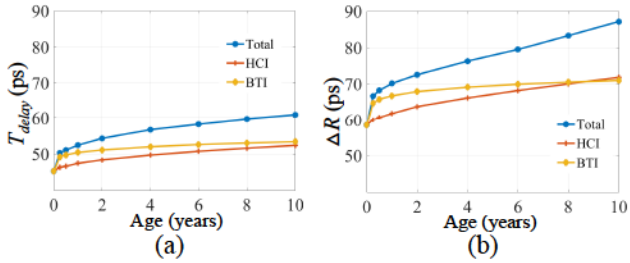

Fig. 3. Effects of aging on (a) T_{delay} and (b) ΔR.

S_{ref} and S_0: when S_{ref} leads S_0, $PW_{Dn} > PW_{Up}$. We show that this may not hold under aging, resulting in PD failure.

In ideal PD operation with identical gate delays, the difference between PW_{Up} and PW_{Dn} is equal to ΔG, the phase difference between S_{ref} and S_0. Realistically, the pulse width difference is affected by process and aging. We can write:

$$\Delta PW = PW_{Dn} - PW_{Up} = \Delta\text{Rise} + \Delta\text{Fall} \quad (1)$$

$$\Delta\text{Rise} = \Delta G + \Delta PV_1; \quad \Delta\text{Fall} = \Delta E + \Delta PV_2 \quad (2)$$

where ΔRise [ΔFall] is the phase difference between the rising [falling] edges of *Up* and *Dn*. Here, $\Delta PV_{1/2}$ are components of process variation and ΔE is caused by aging. Aging does not significantly affect ΔRise because $S_{ref} \uparrow$ and $S_0 \uparrow$ go through a symmetric set of gates that age almost identically as their corresponding excitations nearly have the same duty cycle. Since process variations are baked into a circuit after it is manufactured, $\Delta PV_{1/2}$ are constant. For a fixed ΔG, from (1) and (2), ΔPW varies over time solely due to ΔE. Initially, $G_5 \downarrow$ leads $G_3 \downarrow$, and $G_8 \downarrow$ leads $G_4 \downarrow$. The path that triggers $G_5 \downarrow$ traverses more gates than the one for $G_3 \downarrow$:

$$S_0 \uparrow \xrightarrow{2a} G_4 \uparrow \xrightarrow{2c} Reset \downarrow \xrightarrow{3a} G_6 \uparrow \xrightarrow{3b} G_5 \downarrow; \quad S_{ref} \downarrow \xrightarrow{4a} G_3 \downarrow$$

$$S_0 \uparrow \xrightarrow{2a} G_4 \uparrow \xrightarrow{2c} Reset \downarrow \xrightarrow{3d} G_7 \uparrow \xrightarrow{3e} G_8 \downarrow; \quad S_0 \downarrow \xrightarrow{5a} G_4 \downarrow$$

Hence, as the gates age, $\Delta T_{(G_5\downarrow,G_3\downarrow)}$, the gap between the transitions $G_5 \downarrow$ and $G_3 \downarrow$ reduces over time. A parallel argument can be made to show that $\Delta T_{(G_8\downarrow,G_4\downarrow)}$, the gap between $G_8 \downarrow$ and $G_4 \downarrow$, is also reduced by aging. These two reductions are responsible for ΔE of equation (1) and (2).

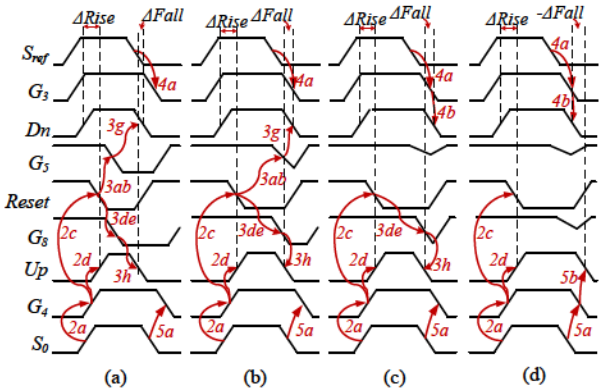

Fig. 4. Impact of aging on PD outputs. Fall transitions of *Dn* and *Up* are controlled by: (a) aligned $G_5 \downarrow$ and $G_8 \downarrow$, (b) nonaligned $G_5 \downarrow$ and $G_8 \downarrow$, (c) $G_3 \downarrow$ and $G_8 \downarrow$, (d) $G_3 \downarrow$ and $G_4 \downarrow$.

Fig. 4(a): Without aging or PV, while the *Reset* signal has symmetric paths to $G_5 \downarrow$ and $G_8 \downarrow$, $G_3 \downarrow$ leads $G_4 \downarrow$ because S_{ref} leads S_0. Hence, $\Delta T_{(G_5\downarrow,G_3\downarrow)} < \Delta T_{(G_8\downarrow,G_4\downarrow)}$. At this time, $\Delta T_{(G_5\downarrow,G_3\downarrow)}$ is sufficiently large so that the output of G_3 stays at high at $G_5 \downarrow$. Similarly, the output of G_4 stays at high at $G_8 \downarrow$. The falling edges of *Up* and *Dn* are controlled by the concurrent transitions $3h$ and $3g$, respectively.

Fig. 4(b): With aging, $\Delta T_{(G_5\downarrow,G_3\downarrow)}$ reduces, as explained above, and $G_5 \downarrow$ begins to overlap with $G_3 \downarrow$. As G_3 is an input to G_5, $G_5 \downarrow$ slows down. This breaks the symmetry between G_5 and G_8,[1] and the fall time of G_5 becomes larger than that of G_8, and $\Delta E > 0$. As the overlap between $G_3 \downarrow$ and $G_5 \downarrow$ increases, ΔE increases, causing ΔFall to increase.

[1] $\Delta T_{(G_8\downarrow,G_4\downarrow)}$ also reduces, but $G_4 \downarrow$ trails $G_3 \downarrow$ and affects $G_8 \downarrow$ later.

Fig. 4(c): With further aging, $G_5 \downarrow$ cannot complete its transition as $G_3 \downarrow$ maintains the output of G_5 to high, with a small noise blip. Now, *Dn* $\downarrow$ is caused by $G_3 \downarrow$ rather than $G_5 \downarrow$, and *Up* $\downarrow$ and *Dn* $\downarrow$ are controlled non-symmetrically:

$$S_{ref} \downarrow \xrightarrow{4a} G_3 \downarrow \xrightarrow{4b} Dn \downarrow; \quad Reset \downarrow \xrightarrow{3d} G_7 \uparrow \xrightarrow{3e} G_8 \downarrow \xrightarrow{3h} Up \downarrow$$

Fig. 4(d): As the path to *Up* $\downarrow$ becomes longer than that to *Dn* $\downarrow$, the aging-induced delay increase to *Up* $\downarrow$ grows faster. As a result, $\Delta Fall$ starts to decrease and eventually becomes negative. In this state, $\Delta Fall$ could eventually becomes equal to the negative of $\Delta Rise$, and from (1), ΔPW becomes zero, making the PD nonfunctional. With time, G_8 also fails to complete its falling transition as it overlaps with $G_4 \downarrow$, just as $G_3 \downarrow$ caught up with $G_5 \downarrow$. Now *Dn* $\downarrow$ is controlled by $G_3 \downarrow$ and *Up* $\downarrow$ is controlled by $G_4 \downarrow$, restoring symmetry:

$$S_0 \downarrow \xrightarrow{5a} G_4 \downarrow \xrightarrow{5b} Up \downarrow$$

Fig. 5 displays impact of aging on PW_{Up}, PW_{Dn}, $\Delta Rise$, and $\Delta Fall$. As predicted above, both PW_{Up} and PW_{Dn} expand with age, and due to the symmetry of the paths, aging does not have any significant impact over $\Delta Rise$. The variation of $\Delta Fall$ also proceeds as predicted: it is initially positive, but then begins to drop when the PD reaches the state in Fig. 4(c), Over a long time, or at higher frequencies, $\Delta Fall$ can turn negative and as in Fig. 4(d).

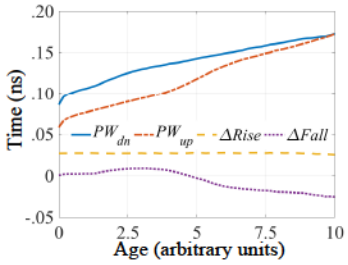

Fig. 5. Impact of transistor aging on the outputs of the PD.

B. Charge pump (CP) and loop filter (LF)

The CP and LF set $V_{control}$, which aligns S_0 with S_{ref}, and keeps its value steady after S_0 and S_{ref} are aligned. However, aging-induced mismatches perturb $V_{control}$ over time.

Circuit structure The structure of the CP and LF is shown in Fig. 6. The CP follows a single-ended, zero-offset topology, and is implemented with two identical devices, $T_{0,CP}$ and $T_{1,CP}$, in a source-coupled configuration. These transistors act as switches controlled by the PD outputs, *Up* and *Dn*. A current source, I_{CP}, is connected to a NMOS current mirror pair that includes matched transistors $T_{4,CP}$ and $T_{5,CP}$. The LF is implemented as a capacitive load to the CP.

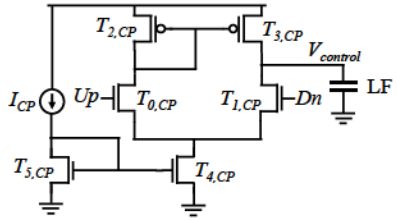

Fig. 6. Single-ended CP architecture with LF.

Operating principle Under identical and periodic *Up* and *Dn* signals, $V_{control}$ will adjust to a steady-state voltage, V_{steady}, which ensures that the currents through $T_{0,CP}$ and $T_{1,CP}$ are

equal. In the steady state, as $T_{2,CP}$ carries the current of $T_{0,CP}$ (identical to that of $T_{1,CP}$), and $T_{3,CP}$ mirrors the current through $T_{2,CP}$, there will be no net charge flow to the LF, and V_{steady} is unchanged. If the inputs are not identical, $V_{control}$ shifts from V_{steady}: it rises when *Up* is high ($T_{0,CP}$ is on) and *Dn* is low ($T_{1,CP}$ is off), and falls if the reverse is true.

Impact of aging To ensure reliable CP performance, it is important to preserve the transistor matching properties. While $T_{5,CP}$ always carries a constant current I_{CP}, $T_{4,CP}$ carries current through it only when $T_{0,CP}$, and $T_{1,CP}$ are ON. Hence, $T_{5,CP}$ faces higher HCI aging than $T_{4,CP}$, which then experiences lower V_{th} shift than $T_{5,CP}$. Hence, for a fixed I_{CP}, current through $T_{4,CP}$ increases with time due to aging.

Fig. 7(a) shows the results of a simulation showing the impact of aging-induced V_{th} degradation of the transistors under unit inverter sizing. For a standalone analysis of the CP, the driving current, I_{CP}, is kept to 10μA to ensure that $V_{control}$ reaches V_{steady} in a few clock cycles, and *Up* and *Dn* are kept identical and periodic with 50% duty cycle. The simulation shows the significant mismatch induced between $T_{4,CP}$ and $T_{5,CP}$, 73% in 10 years, due to asymmetric HCI aging. It is also seen that $T_{0,CP}$ and $T_{1,CP}$ age at similar rates, which is unsurprising as *Up* and *Dn* are identical.

Transistors $T_{2,CP}$ and $T_{3,CP}$ undergo BTI stress when $T_{0,CP}$ is on. The stress voltage depends on the driving current of the CP, and for the value used here, PMOS BTI aging is negligible. The impact of I_{CP} on transistor aging is further studied in Fig. 7(b). Larger driving currents result in larger current densities in the NMOS transistors, increasing HCI. Moreover, when $T_{0,CP}$ is on, larger I_{CP} increases the current through $T_{2,CP}$ and $T_{3,CP}$, raising their overdrive voltage. This raises the BTI stress and hence, higher V_{th} shifts.

With a fixed I_{CP}, transistor sizing of the CP also plays a significant role in aging, as shown in Fig. 7(c). With a fixed driving current of 10μA, a larger transistor width reduces HCI-induced ΔV_{th} in the NMOS transistors as current density reduces. At constant current, wider PMOS devices imply that the overdrive voltage reduces, lowering BTI stress and aging.

As stated earlier, higher currents through $T_{2,CP}$ require higher overdrive voltages. As aging increases the current through $T_{4,CP}$, the gate voltage of $T_{2,CP}$ drops, and $V_{control}$ drops to balance current through $T_{0,CP}$ and $T_{1,CP}$. Fig. 7(d) shows how $V_{control}$ varies with aging under identical *Up* and *Dn*: $V_{control}$ drops with time, instead of remaining constant.

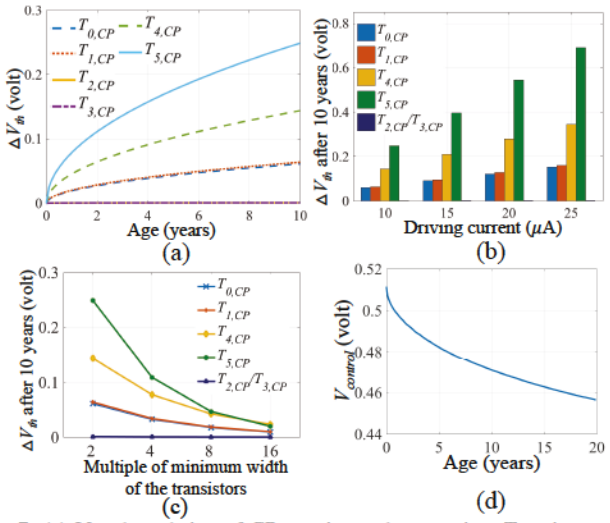

Fig. 7. (a) V_{th} degradation of CP transistors due to aging; Transistor aging trends with (b) current, I_{CP}, (c) transistor width; (d) $V_{control}$ under aging.

C. Voltage controlled delay line (VCDL)

We now show how aging shifts the delay range of the VCDL and degrades signal propagation through the VCDL.

Circuit structure Fig. 8 represents the architecture of a VCDL block, based on a shunt capacitor topology [7]. A shunt transistor, $T_{3,VCDL}$, is used as the variable resistance to connect an inverter output to a capacitive load, $T_{4,VCDL}$. The voltage, $V_{control}$, at its gate regulates the resistance of the shunt transistor and controls the effective load to the inverter. A higher $V_{control}$ lowers resistance and raises the effective load capacitance, increasing the inverter delay. Two such inverters are connected to form a buffer (Fig. 8(a)) and n units of such buffers are cascaded to form a n-stage VCDL that generates a delayed replica of the reference signal (Fig. 8(b)).

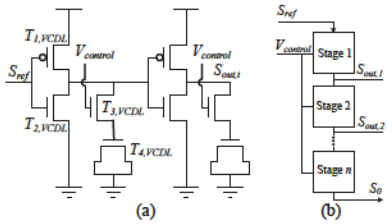

Fig. 8. (a) A buffer stage of a VCDL. (b) A n-stage VCDL.

Operating principle To achieve this designated delay with reference to an edge in S_{ref}, the VCDL must be within a specified delay band. If S_{ref} has a period of T_{clk}, then the VCDL must maintain the following constraints to stably create the one-cycle phase difference:

$$0.5\,T_{clk} < Delay_{min} < T_{clk} \quad (3)$$

$$T_{clk} < Delay_{max} < 1.5\,T_{clk} \quad (4)$$

where $Delay_{min}$ and $Delay_{max}$ are the delay under the minimum and maximum $V_{control}$, respectively. If these bounds are not obeyed, then the negative feedback mechanism of the DLL could cause S_0 to lock with an unintended edge of S_{ref} resulting in a phase difference that is larger or smaller than one clock cycle, referred to as the "stuck problem" [8]. The VCDL delay range can be controlled either with varying the delay per unit inverter or number of stages of the VCDL. The inverter delay depends on the sizes of $T_{3,VCDL}$ and $T_{4,VCDL}$.

Impact of aging In Fig. 8, when $V_{control} = 0$, the load on the inverter in each stage, provided by $T_{3,VCDL}$, should be large enough to meet constraint (3). This large load results in a high current density through the inverter, which grows larger when the effective load is increased by setting $V_{control} > 0$. Hence, HCI-induced V_{th} degradation of $T_{2,VCDL}$ is dependent on $V_{control}$ as well as the sizes of $T_{3,VCDL}$ and $T_{4,VCDL}$.

We analyze the reliability of a 10-stage VCDL whose $Delay_{min} \approx 0.5 \cdot T_{clk}$ and $Delay_{max} \approx 1.5 \cdot T_{clk}$, where $T_{clk} = 1$ns. When both $T_{1,VCDL}$ and $T_{2,VCDL}$, are 2× and 1× of min-size, respectively, $T_{3,VCDL}$ must be sized to 27×.

Fig. 9(a) shows the degradation ΔV_{th} of each transistor of a shunt capacitor inverter when $V_{control} = 0$. The HCI induced V_{th} shift of $T_{2,VCDL}$ is compared with that of a transistor, $T_{2,Inverter}$, in an identical inverter, but without the tunable load: this lower load implies less current, and lower

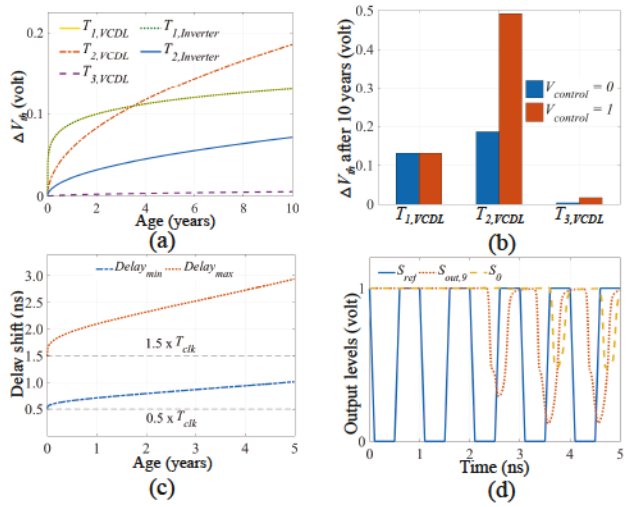

Fig. 9. a) ΔV_{th} of transistors in Fig. 8(a) after aging. (b) Comparison of ΔV_{th} at minimum and maximum $V_{control}$. (c) Change in delay range of the VCDL with aging. (d) Failure in VCDL operation due to aging.

degradation, as seen in the plot. On the other hand, if we compare the PMOS transistor, $T_{1,VCDL}$ with an analogously defined $T_{1,Inverter}$, they experience the same aging, since they are primarily affected by BTI, which is dependent on the identical bias in both scenarios, and not by HCI. Even though $T_{3,VCDL}$ carries current in each half-cycle, while $T_{2,VCDL}$ carries current only in the falling half-cycle, degradation of the former is lower than that of the latter. This is primarily due to the large size of $T_{3,VCDL}$, which reduces the current density (7.4% of that through $T_{2,VCDL}$), and hence HCI aging.

Fig. 9(b) compares ΔV_{th} at the minimum (0V) and maximum (1V) value of $V_{control}$. The latter corresponds to a high load, and hence a high current, causing high aging in $T_{2,VCDL}$, while $T_{3,VCDL}$ is barely affected due to its large size, and $T_{1,VCDL}$, a PMOS device, is unaffected by HCI.

The BTI- and HCI-induced V_{th} degradation of $T_{1,VCDL}$ and $T_{2,VCDL}$, respectively, will increase the VCDL delay at constant $V_{control}$, meaning that $Delay_{min}$ and $Delay_{max}$ will rise, potentially violating (3) and (4). As shown in Fig. 9(c), both $Delay_{min}$ and $Delay_{max}$ rise by ∼100% in 5 years. The BTI transient causes a steep initial rise in both $Delay_{min}$ and $Delay_{max}$, while HCI dominates in the longer term. Both events conspire to send the VCDL in the "stuck problem" defined above. While some margin may be added to avoid this, it means that $Delay_{max}$ must be reduced, implying that the range in which the VCDL can operate is more limited.

Fig. 9(d) shows another way that aging can render a VCDL inoperable. If delays increase sufficiently, the inverters are unable to complete their output swings. An incomplete swing at the output of any inverter stage is propagated to subsequent stages, resulting in an even more distorted output. At some point, an intermediate inverter stage may even fail to switch.

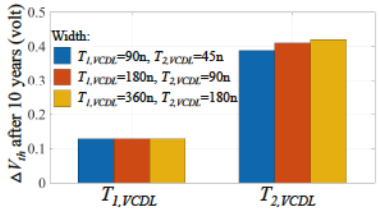

Fig. 10. ΔV_{th} for various VCDL transistor sizes after 10 years.

Unlike the CP, aging induced V_{th} shifts in this VCDL cannot be reduced by transistor sizing. In a n-stage VCDL with a $Delay_{min}$ and $Delay_{max}$ of $0.5 \times T_{clk}$ and $1.5 \times T_{clk}$, respectively, each stage has to contribute a minimum delay of $(0.5 \times T_{clk})/n$ and a maximum delay of $(1.5 \times T_{clk})/n$. Hence, the sizing of $T_{3,VCDL}$ and $T_{4,VCDL}$ are dependent on the sizing of $T_{1,VCDL}$ and $T_{2,VCDL}$. A higher width for $T_{1,VCDL}$ and $T_{2,VCDL}$ will require higher width for $T_{3,VCDL}$ and $T_{4,VCDL}$, implying that the NMOS transistors must drive higher currents, inducing more HCI aging. This keeps ΔV_{th} almost unchanged, as validated by our simulations in Fig. 10.

III. DLL-LEVEL IMPACT

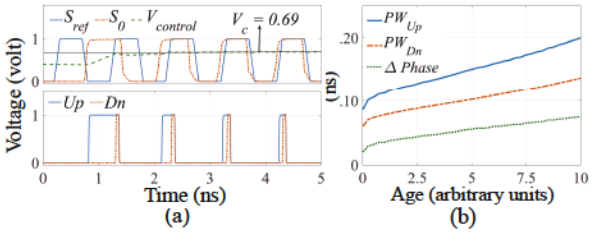

Fig. 11. (a) Transients of DLL operation without aging. (b) Phase difference between S_{ref} and S_0 after alignment with aging.

We now explore the impact of these block-level variations at the DLL level. As before, a delay of one cycle is specified between S_{ref} and S_0 and $T_{clk} = 1$ns. At first, the VCDL supplies a not-yet-synchronized S_0 signal, and the PD generates asymmetric *Up* and *Dn* signals, causing $V_{control}$ to rise or fall from its initial value to a voltage V_c that moves S_0 closer to a one-cycle delay. However, $V_{control}$ fails to remain at V_c due to the overlap between *Up* and *Dn* over a time frame, $T_{overlap}$, which causes transistors $T_{0,CP}$ and $T_{1,CP}$ to be on simultaneously. During $T_{overlap}$, $V_{control}$ tries to return to V_{steady} (Section II-B) from V_c, creating an offset between $V_{control}$ and V_c. This causes a misalignment ($\Delta Phase$) between S_{ref} and S_0 as reflected in Fig. 11(a).

In Fig. 11(b), PW_{Up} and PW_{Dn} increase due to PD aging. As ΔRise and ΔFall are much smaller than increases in PW_{Up} and PW_{Dn}, $T_{overlap}$ increases with aging. Hence, the $\Delta Phase$ increases with time.

This problem worsens further: due to the misalignment of S_{ref} and S_0, *Up* and *Dn* signals remain asymmetric, causing uneven current densities through $T_{0,CP}$ and $T_{1,CP}$, thus creating mismatches between them due to HCI, as shown in Fig. 12(a). However, the magnitude of this mismatch is relatively low, and can be reduced even further if the drive current is reduced, or wider transistors are used. Due to transistor aging in PD, V_{th} degradation of $T_{0,CP}$ and $T_{1,CP}$ increase although their mismatch remains almost unchanged.

The aging-induced mismatch between $T_{4,CP}$ and $T_{5,CP}$ (Section II-B) has a positive side-effect as it causes currents

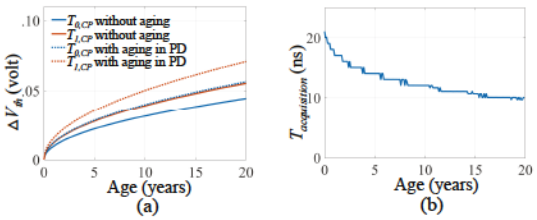

Fig. 12. (a) Mismatch induced by DLL operation between $T_{0,CP}$ and $T_{1,CP}$. (b) Change of $T_{acquisition}$ due to transistor aging.

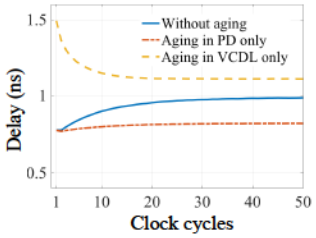

Fig. 13. Delay between the S_{ref} and S_0 in different circumstances.

through $T_{4,CP}$ to increase with time. Hence, $T_{acquisition}$, the time taken by CP to reach V_c, reduces with aging (Fig. 12(b)).

Fig. 13 shows the impact of aging on the DLL. Without aging, when $V_{control}$ is at the mid-point (∼0.5V) of its range initially, if the DLL restarts its operation S_0 aligns itself to S_{ref} with a delay of 1ns (blue curve). We show the behavior of the DLL in the worst-case scenarios if we consider the impact on the DLL of: (i) aging in the PD only (red curve): the phase difference does not reduce as the PD faces the situation explained in Fig. 4(d), (ii) aging in the VCDL only (orange curve): the initial delay is below $1.5\times T_{clk}$, and the DLL pulls S_0 down and tries to align with S_{ref} keeping a 1ns delay. However, the DLL fails in this case too as $Delay_{min}$ has risen above 1ns. In both cases, the DLL faces functional failure.

IV. Conclusion

This paper analyzes HCI- and BTI-induced aging in a DLL at the block level and the system level. At 1GHz, aging is found to delay the reset operation of the PD by 42.6% in 10 years. This degrades the sensitivity of the PD to the phase difference of its inputs and could result in a functional failure, and increases steady-state misalignment between the output and reference signal of DLL. For the CP, aging creates a ≥73% threshold voltage mismatch for a driving current of ≥10 μA after 10 years, causing the VCDL control voltage to drop, and reduces the CP acquisition time by ∼40% in 10 years. Further, aging can result in a ∼100% rise in the VCDL delay after 5 years, and could even cause the VCDL to fail. Together, these can result in parametric or functional failure.

Appendix

A. Bias temperature instability (BTI)

Negative BTI (NBTI) affects PMOS devices when the gate-to-source voltge, V_{gs}, is smaller than its threshold voltage, V_{th}. The negative voltage stress across the gate stack degrades V_{th} over time, resulting in lower drive current. Positive BTI (PBTI) in NMOS devices is analogous, but is often negligible.

We use the dynamic NBTI model from [9], which models two phases: *stress*, where V_{th} degrades, and *recovery*, where it partially recovers. The degradation, $\Delta V_{th}(t)$, is:

$$\Delta V_{th}(t) = \begin{cases} \left(K_v(t-t_0)^{1/2} + (\Delta V_{th}(t_0))^{1/2n_{bti}}\right)^{2n_{bti}} & (stress) \\ \Delta V_{th}(t_1)\left(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(t-t_1)}}{2t_{ox}+\sqrt{Ct}}\right) & (recovery) \end{cases} \quad (5)$$

$$K_v = \left(\frac{qt_{ox}}{\epsilon_{ox}}\right)^3 K^2 C_{ox}|V_{gs}-V_{th}|\sqrt{C}\exp\left(\frac{2E_{ox}}{E_0}\right)$$

$$C = T_0^{-1}\exp\left(-\frac{E_a}{kT}\right);\ \ E_{ox} = \frac{V_{gs}-V_{th}}{t_{ox}} \quad (6)$$

$$t_e = \begin{cases} t_{ox}, & (t-t_0) \geq t_1 \\ t_{ox}\sqrt{\frac{t-t_0}{t_1}} - \frac{\sqrt{\xi_2 C(t-t_0)}}{2\xi_1}, & \text{otherwise} \end{cases}$$

Here, t_0 and t_1 specify the start for *stress* and *recovery*; $n_{bti} = 1/6$; t_{ox}, t_e, ϵ_{ox}, and C_{ox} are the thickness, effective thickness, permittivity, and capacitance of the oxide, respectively; E_{ox} is the electric field across the gate; T is the temperature; q, E_a, and k are, respectively, the electron charge, activation energy, and Boltzmann's constant; ξ_1, ξ_2, K, E_0, and T_0 are constants.

B. Hot carrier injection (HCI)

Hot carriers (HCs) are electrons/holes with sufficient energy and momentum to generate oxide interface charge. For a stress time, t_{st}, HCI degradation can be modeled as:

$$\Delta V_{th} = A(age)^{n_{hci}};\ age = R_{it}t_{st} \quad (7)$$

Here, n_{hci}=0.5, A is a constant, and the interface trap generation rate, R_{it}, is given by the energy-driven framework of [10]:

$$\begin{aligned} R_{it} \ = \ & K_{SVE}\left[\frac{I_{ds}}{W}\right]^{a_1}\left[\frac{I_{bs}}{I_{ds}}\right]^{m} + K_{EES}\left[\frac{I_{ds}}{W}\right]^{a_2}\left[\frac{I_{bs}}{I_{ds}}\right]^{m} \\ & + K_{MVE}V_{ds}^{a_3/2}\left[\frac{I_{ds}}{W}\right]^{a_3}\exp\left[-\frac{E_{emi}}{kT}\right] \end{aligned} \quad (8)$$

The three terms correspond to the degradation under single vibrational excitation (SVE), electron-electron scattering (EES) and multiple vibrational excitation (MVE), respectively, with the corresponding constants, K_{SVE}, K_{EES}, and K_{MVE}. The constants, m, a_1, a_2, a_3, and E_{emi} are defined in [10]; I_{bs}/I_{ds} is the impact ionization ratio; where I_{bs} and I_{ds}/W are the substrate current and drain current density, respectively.

As the transistor I_{ds} changes during circuit operation, R_{it} is also time-dependent. In steady state, for DLL blocks with signals of period T_{clk}, the increase in transistor age, AG, after a clock cycle, and the corresponding age over time t_{st} are [11]:

$$AG = \left(\sum_{n=1}^{N} R_{it,n}\right)\Delta t\ \ ;\ \ age = AG \times t_{st}/T_{clk} \quad (9)$$

Here, Δt is the sampling period, and $N = T_{clk}/\Delta t$.

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