

# $\beta$ -Ga<sub>2</sub>O<sub>3</sub> Delta-Doped Field Effect Transistors with Current Gain Cutoff Frequency of 27 GHz

Zhanbo Xia<sup>1</sup>, Hao Xue<sup>1</sup>, Chandan Joishi<sup>1,3</sup>, Joe McGlone<sup>1</sup>, Nidhin Kurian Kalarickal<sup>1</sup>, Shahadat H

Sohel<sup>1</sup>, Mark Brenner<sup>1</sup>, Aaron Arehart<sup>1</sup>, Steven Ringel<sup>1,2</sup>, Saurabh Lodha<sup>3</sup>, Wu Lu<sup>1</sup>, Siddharth Rajan<sup>1,2</sup>

**Abstract**— As an ultra-wide bandgap semiconductor,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> has attracted great attention for high power, high voltage, and optoelectronic applications. However, until now, high frequency performance of Gallium Oxide devices has been limited to relatively low **current gain cutoff frequencies** below 5 GHz. Here we show that highly localized delta-doping designs can enable high sheet charge density to enable devices with short gate lengths that allow high frequency operation. Field effect transistors with a gate length of 120 nm on such delta-doped  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> are reported here with **extrinsic** unity current gain frequency of 27 GHz. The device has a peak drain current of 260 mA/mm, transconductance (gm) of 44 mS/mm, and 3-terminal off-state breakdown voltage of 150 V. These results demonstrate the potential of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> for future RF and millimeter-wave device applications.

**Index Terms**— Ga<sub>2</sub>O<sub>3</sub> MESFET, High frequency, RF device, MBE, wide bandgap

## I. INTRODUCTION

$\beta$ -Ga<sub>2</sub>O<sub>3</sub> has recently attracted attention as an ultra-wide bandgap (4.5–4.9 eV) semiconductor that can be controllably doped, and grown directly from the melt in single crystal form. Commercially available melt-grown  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> wafers can be obtained with crystal surfaces oriented along various directions. The ease of n-type doping with tetravalent cations, a wide variety of bulk single crystal [1,2,3,4], and epitaxial film growth techniques [5,6,7,8,9,10,11] have triggered worldwide interest in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. The predicted breakdown electric field (6–8 MV/cm) [12] is higher than that of GaN or SiC (~3 MV/cm), which when combined with electron mobility (predicted ~250–350 cm<sup>2</sup>/Vs [13]) and electron velocity (1.2×10<sup>7</sup> cm/s [14]) yields amongst the best figures of merit for power electronic and high frequency devices. As a result,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> possesses potential for future electronic and optoelectronic [15] applications.

Excellent performance has been reported for early  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices, including Schottky diodes [16,17], MOSFETs [18,19,20], MESFETs [11,21] and HEMTs [22,23,24]. In particular, experimental observations of high breakdown fields above 5 MV/cm [16,17,25,] have been reported for both lateral MOSFET transistors and vertical Schottky diodes. Ga<sub>2</sub>O<sub>3</sub> RF

MOSFET with current gain cut-off frequency of 5.1 GHz has been demonstrated [26]. To maintain high electron mobility, most previous work on  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> employed thick channels (> 200 nm) with low n-type doping (< 1×10<sup>18</sup> cm<sup>-3</sup>) [12,18,25,27]. However, due to aspect ratio considerations, such thick channel designs are not optimal for higher frequency applications of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> transistors. In high frequency devices, where the gate lengths would need to be scaled well into the sub-micron regime, the gate would not be able to control the thick channel because of the poor aspect ratio. Therefore, in this work, our objective is to realize vertically and laterally scaled field effect transistors with high sheet-charge density delta-doped channels. These results demonstrate the potential of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> for future high power RF and millimeter-wave device applications.

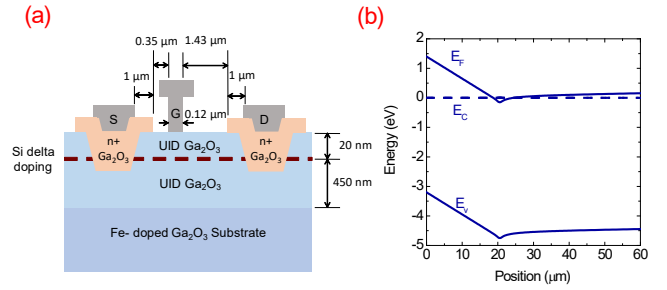


Figure 1 (a) Device schematics (b) Energy band diagram of delta doped MESFET

## II. DEVICE GROWTH AND FABRICATION

The structure (Figure 1) used in this work was grown by O<sub>2</sub> plasma assisted molecular beam epitaxy on commercially available Fe-doped semi-insulating Ga<sub>2</sub>O<sub>3</sub> (010) substrate. Before starting growth, the substrate was cleaned by O<sub>2</sub> plasma (300 W, 1.5×10<sup>-5</sup> Torr) at 800 °C for 20 min for interface impurity removal. The substrate was kept at 700 °C during growth. 300 W O<sub>2</sub> plasma, 1.55×10<sup>-5</sup> Torr chamber pressure, and Ga beam equivalent pressure of 8.2×10<sup>-8</sup> Torr were maintained to achieve an O-rich growth condition with 2.7 nm/min growth rate. 450 nm of unintentionally doped Ga<sub>2</sub>O<sub>3</sub> was first grown on the substrate. Then the Si shutter was opened for 3 seconds to realize a sub-monolayer of Si doping. The Si cell temperature was kept at 950 °C. 20 nm of unintentionally

This work is supported by the Department of the Defense, Defense Threat Reduction Agency (Grant HDTRA11710034) and NSF ECCS-1809682.

Zhanbo Xia, Hao Xue, Chandan Joishi, Joe McGlone, Nidhin Kurian Kalarickal, Shahadat H Sohel, Mark Brenner, Aaron Arehart, Steven Ringel Wu Lu and Siddharth Rajan are with Department of Electrical and Computer Engineering, Ohio State University, OH, USA.

Siddharth Rajan and Steven Ringel are with Department of Material Science Engineering, Ohio State University, OH, USA.

Chandan Joishi and Saurabh Lodha are with Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai, India. E-mail: xia.104@osu.edu, Phone: +1-614-962-2427

doped  $\text{Ga}_2\text{O}_3$  was continuously grown for 7.4 min after Si delta doping for the gate barrier. Smooth surface morphology with an RMS of 0.9 nm was obtained.

Heavily doped n-type  $\text{Ga}_2\text{O}_3$  with doping concentration of  $2 \times 10^{20} \text{ cm}^{-3}$  was regrown by MBE in source and drain region to achieve low contact resistance. The ohmic contact regrown process was discussed in our previous report [19]. A Ti/Au/Ni metal stack (30 nm/ 100nm/ 30nm) was deposited by e-beam physical vapor deposition followed by annealing at 470 °C for 1 min. 160 nm mesa recessing was carried by  $\text{BCl}_3$  based ICP-RIE dry etching (ICP power = 200 W, RIE power = 30 W, Pressure = 15 mTorr). Vistec EBP5000 electron beam lithography system was used to define a T-shaped gate on PMMA/MMA/PMMA resist stack. The Schottky gate contact was formed with an e-beam evaporated Ni/Au metal stack (30 nm/ 150 nm). The fabricated device is shown in Figure 2 by scanning electron microscope imaging.

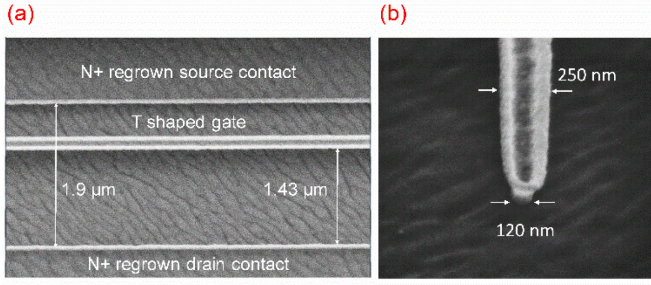


Figure 2 (a) Plan-view SEM image of the fabricated device (b) Side-view SEM image of 120nm T-shaped gate

### III. RESULTS AND DISCUSSION

Contact resistance of  $0.4 \Omega\text{-mm}$  and sheet resistance of  $7.5 \text{ k}\Omega/\square$  were measured from transfer length method (TLM) patterns defined on MESFET structure. Measurements of a TLM pattern on n+ regrown layer showed  $0.1 \Omega\text{-mm}$  metal to semiconductor contact resistance. Hall measurements carried out on isolated van der Pauw structures revealed a sheet carrier density of  $1.13 \times 10^{13} \text{ cm}^{-2}$  with Hall mobility of  $70 \text{ cm}^2/\text{Vs}$  at room temperature. Small-signal capacitance-voltage measurements were carried out using an Agilent B1500A at a frequency of 100 kHz. The gate capacitance (Figure 3) shows accumulation characteristics with nominal depletion distance at zero gate bias of 20 nm, as expected from the epitaxial design. The carrier density profile extracted (inset of Figure 3) shows a narrow electron distribution corresponding to a 2-dimensional electron gas with an integrated sheet carrier density of  $9.9 \times 10^{12} \text{ cm}^{-2}$  (Figure 3) at zero gate bias.

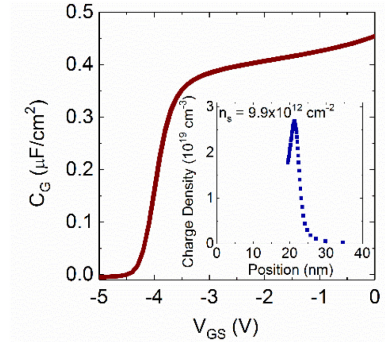


Figure 3 Capacitance-voltage characteristics of delta doped MESFET and (inset) electron concentration profile extracted from CV measurements

DC electrical characteristics of the delta doped MESFET were measured on a  $0.12 \mu\text{m}$  gate length device. The device reported here was a two finger structure ( $2 \times 50 \mu\text{m}$ ), with source-drain spacing of  $1.9 \mu\text{m}$ , and gate-drain spacing of  $1.4 \mu\text{m}$ . A maximum drain current  $I_{\text{DS, MAX}}$  of  $0.26 \text{ A/mm}$  was measured at  $V_{\text{GS}} = 2 \text{ V}$  and  $V_{\text{DS}} = 12 \text{ V}$ , and maximum transconductance  $g_{\text{m, max}}$  of  $44 \text{ mS/mm}$  measured at gate bias of  $-2.5 \text{ V}$  (Figure 4(a), (b)). The channel conduction was pinched off at  $V_{\text{G}} = -6 \text{ V}$ , which is more negative than the pinch-off voltage from capacitance measurements. This is attributed to short channel effects. An  $I_{\text{ON}}/I_{\text{OFF}}$  ratio of  $10^8$  was measured at a drain bias of  $12 \text{ V}$ . The three-terminal breakdown voltage (using  $0.1 \text{ mA/mm}$  drain current as breakdown condition) was estimated to be  $150 \text{ V}$  (Figure 5) at gate bias of  $-10 \text{ V}$ , while the two-terminal Schottky gate-drain breakdown voltage was  $164 \text{ V}$  on the same device. Gate current remained  $8 \mu\text{A/mm}$  when three terminal breakdown happened. This suggests that the breakdown is caused by source-drain punch through due to non-ideal gate-to-channel aspect ratio.

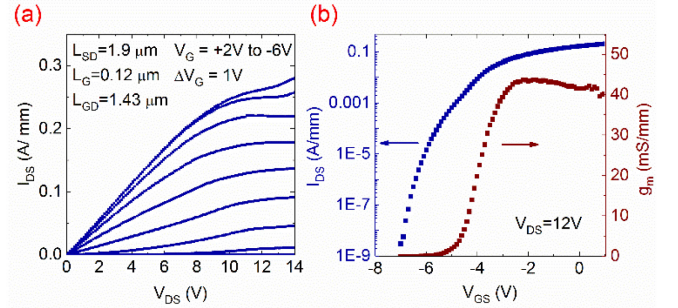


Figure 4 (a) Measured output characteristics (b) Transfer characteristics of delta doped MESFET showing FET operation (d) Three terminal breakdown characteristics

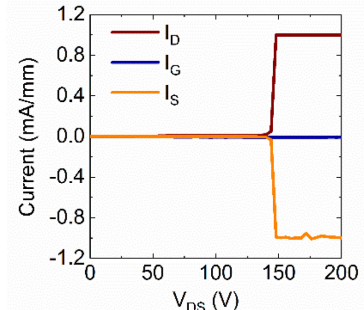


Figure 5 Three terminal breakdown characteristics showing breakdown voltage of  $150 \text{ V}$

The high frequency small-signal performance was characterized between 1 GHz and 40 GHz using an Agilent 8722ES vector network analyzer, and on-wafer ground-signal-ground (GSG) probes. Network analyzer calibration was carried out using the through-reflect-load (TRL) method on a standard calibration substrate (Cascade Microtech). The parasitic pad capacitances were de-embedded using an isolated GSG device patterns on the device wafer. Figure 6(a) shows the short-circuit current gain ( $h_{21}$ ) and unilateral power gain (U). 27 GHz peak current gain cut-off frequency ( $f_T$ ) and associated peak maximum oscillation frequency ( $f_{MAX}$ ) of 16 GHz were measured at gate bias of -2 V and drain bias of 12 V. The cutoff frequency without de-embedding pad capacitance was 26 GHz. The dependence of the cutoff frequency on gate bias (shown in Figure 6(b)) follows the same trend as the transconductance.

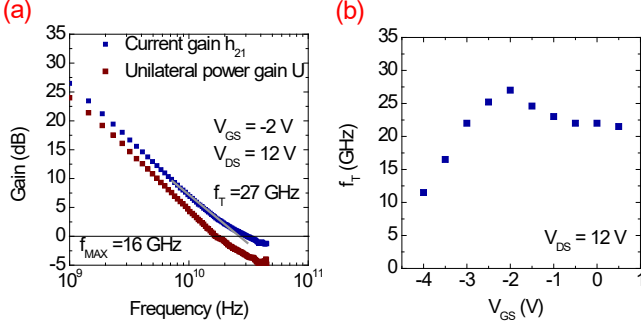


Figure 6 (a) Measured small signal performance of 120 nm gate length delta doped MESFET (b) Measured cutoff frequency  $f_T$  as a function of gate voltage measured at 12 V drain bias.

We now discuss the effect of parasitic resistance on the performance of the device. To estimate the device source resistance the following method was used [28]. The source current was swept from 25 mA/mm to 175 mA/mm while the gate was forward biased to keep a 1  $\mu$ A/mm forward current. The source resistance was estimated as the differential of the gate voltage with respect to source current (Figure 7). Based on this method, a source resistance of 7.4  $\Omega$ -mm was extracted. This resistance is significantly higher than that estimated from TLM measurement (3  $\Omega$ -mm), and we attribute it to either surface depletion in the source access region or mobility degradation at high fields [29]. Further investigations are needed to understand the physical phenomenon that cause the resistance increase. Equivalent RF gate resistance of 233  $\Omega$ /mm [30] was extracted using test structures fabricated on the same substrate. The relatively high gate resistance is attributed to a thin gold layer used in the gate, as well as a narrow T-gate cap layer. Using these measured parameters for the source and gate resistance, a small-signal circuit model was extracted [31], and the parameters at 10 GHz are shown in Table 1. Based on the simplified analytical expression for the power gain cutoff frequency  $f_{MAX}$

$$f_{MAX} = \frac{1}{2} \frac{f_T}{\sqrt{\frac{2\pi g_m C_{gd}(R_s + R_d)}{C_{gs} + C_{gd}} + \frac{R_g + R_s}{r_{ds}}}}$$

, where  $r_{ds}$  is output resistance, the high gate and source resistance were found to be the principal reasons for the  $f_{MAX}/f_T$  ratio being 0.6. Future design of the transistor to reduce source resistance (by increasing access region conductance),

and gate resistance (through gate design), could enable higher power gain cutoff frequency.

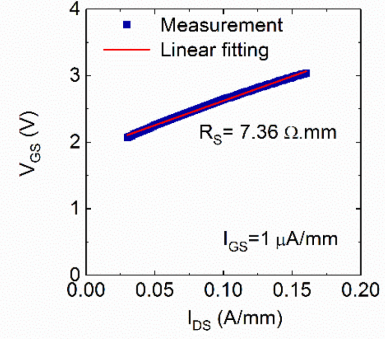


Figure 7 Dynamic source resistance measurement. Gate bias applied to keep a constant 1  $\mu$ A/mm gate forward current with drain changing from 25 mA/mm to 175 mA/mm

The current gain cut-off frequency of 27 GHz measured here corresponds to  $f_T \cdot L_G$  product of 3.2 GHz- $\mu$ m, whereas, based on the predicted saturated electron velocity in  $\text{Ga}_2\text{O}_3$  (greater than  $1 \times 10^7$  cm/s [13,32]), it is expected to be significantly higher. We attribute the discrepancy to the large dynamic source resistance, which leads to depletion of the charge at the source edge of the gate. The device performance is therefore limited by source choking effect instead of electron saturation velocity. Further study is needed to understand the mechanism of the source resistance for future high-frequency  $\text{Ga}_2\text{O}_3$  field effect transistor.

#### IV. CONCLUSION

In conclusion, we have demonstrated a delta-doped  $\beta$ - $\text{Ga}_2\text{O}_3$  MESFET with cut-off frequency of 27 GHz. A peak transconductance of 44 mS/mm and peak current density of 0.26 A/mm were obtained. While the performance of this device represents significant progress for this material technology, our work also shows that further understanding of the device and material physics are needed to fully explain the device characteristics. The device structure discussed here demonstrates a promising platform to study the fundamental transport properties of  $\beta$ - $\text{Ga}_2\text{O}_3$ , and to explore the potential of this material system for RF and millimeter-wave device applications.



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