INVITED PAPER

Codesign Methodologies and Tools for Cyber–Physical Systems

In this paper, the authors propose to codesign cyber and physical components of CPSs in a holistic environment. They present a number of codesign approaches in modeling, simulation, synthesis, verification, and validation. They also discuss open challenges in CPS codesign and possible future directions for addressing them.

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ABSTRACT | Cyber–physical system (CPS) analysis and design are challenging due to the intrinsic heterogeneity of those systems. Today, CPSs are often designed by leveraging existing solutions and by adding cyber components to an existing physical system, thus decomposing the design into two separate phases. In this paper, we argue that the codesign of the cyber and physical components would expose solutions that are better under all aspects, such as safety, efficiency, security, performance, reliability, fault tolerance, and extensibility. To do so, automated codesign tools are a necessity due to the complexity of the problems at hand. In the paper, we will discuss the key needs and challenges in developing modeling, simulation, synthesis, validation, and verification tools for CPS codesign, present promising codesign approaches from our teams and others, and point out where additional research is needed.

KEYWORDS | Codesign; cyber–physical systems (CPSs); design automation; modeling; synthesis; verification

I. INTRODUCTION

Cyber–physical systems (CPSs) such as autonomous vehicles, industrial robots, medical devices, smart buildings, and smart infrastructures promise substantial economic and societal benefits. The design of these systems, however, faces serious challenges from the fast increase of system scale and complexity, the close interaction with dynamic physical processes, the adoption of advanced and distributed embedded platforms, and the stringent requirements on a variety of design metrics such as performance, safety, security, fault tolerance, extensibility, energy consumption, and cost.

A key principal in tackling these challenges is to codesign various cyber and physical components of the system, i.e., to model, simulate, synthesize, and validate the sensing, control, computation, and communication algorithms, the software and hardware implementation platform, the mechanical components and processes, and the surrounding physical environment and human activities in a holistic environment. In fact, the term "cyber–physical systems" itself shows a unified view of heterogeneous cyber and physical components, and emphasizes the importance of analyzing their interactions to achieve better system designs.

In current practice, however, CPSs are still designed in isolated stages that address individual elements. For instance, control design is carried out with modeling of the physical processes but usually without consideration of the cyber platform. As control performance and stability significantly depend on the reliability and timing behavior of the underlying computation and communication, such isolation of control design and cyber platform implementation could lead to long production cycles, inferior systems or even infeasible designs.

To facilitate codesign of CPSs, new methodologies and tools are greatly needed. These tools should be able to capture the key interactions among various cyber

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and physical components, and to explore the entire design space in a holistic, quantitative, and automated fashion.

In the rest of the paper, we will discuss the needs and challenges for CPS codesign, and present promising codesign methodologies and tools. We organize the paper based on different design automation technology categories: modeling and simulation (Section II), synthesis (Section III), and verification and validation (Section IV). As we will see, tools in each of these categories are essential to achieve successful codesign of CPSs and ultimately effective and reliable systems.

II. MODELING AND SIMULATION

Modeling and simulation tools set the foundation for codesigning CPSs. They enable designers to capture the behavior of various cyber and physical components, specify design requirements and objectives, evaluate and validate design options based on simulations, and identify design factors that are critical for synthesis and verification.

To facilitate codesign in CPSs, it is particularly important that these tools provide the following capabilities.

- Modeling heterogeneous components in a common environment: Compared to traditional embedded systems, CPSs often involve components that have heterogeneous behavior and could be captured with different models of computation (MoCs). For instance, there are intrinsic differences between discrete cyber components and continuous physical processes. The first step for codesign is to enable modeling heterogeneity in a common environment. The component models do not have to be captured in the same language, but their interfaces should be well defined with clear syntax and semantics.
- Cosimulating heterogeneous components: Simulation is an important capability for reasoning about CPS behavior. It requires cosimulation of components that have different semantics, abstraction levels, and time scales. To enable such cosimulation, clear execution semantics have to be defined at the component interfaces and at the entire system level. Monitors and rollback mechanisms may be introduced to facilitate the simulation.
- Separating design concerns: To effectively and efficiently codesign multiple design components (e.g., a control algorithm and its embedded implementation), clearly separating their models and formalizing the interfaces is important. This separation in modeling provides the benefit of 1) exploring design alternatives of one component while reusing other components' designs; and of 2) identifying the key factors that affect the interactions among components and leveraging these factors in codesign.

In this section, we present several design environments that provide these capabilities, with particular attention to the Berkeley tools.

A. Metropolis and Metro II

The principles of heterogeneous modeling, cosimulation, and separation of concerns had been well established in the paradigm of platform-based design [1], [2], and realized in the design environment Metropolis [3], [4]. Specifically, Metropolis supports various common MoCs (e.g., dataflow, state machine, discrete event, and discrete time) with a unified language, the Metropolis meta-model (MMM). Heterogeneous components can be captured with MMM and cosimulated through a SystemC based engine [5], [6]. Furthermore, a key principle in Metropolis is to separate the modeling of system functionality (i.e., what the system does) from the modeling of architectural platform (i.e., how the system is implemented). The separated functional model and architectural model, both described in MMM along with design constraints, are then brought together through a mapping process, during which different platform implementation of the functionality are explored. This separation also enables function-architecture codesign, where different functional designs or platform choices can be easily explored without changing the other part's model (while considering the other part through mapping).

In Metro II [4], [7], [8], the second generation of Metropolis, these principles facilitating codesign are further strengthened. First, instead of requiring all components to be captured in the same MMM language, Metro II provides wrappers to support integrating and cosimulating components that are described in different languages. This is particularly important for CPSs, as components from different domains often come with their own modeling languages and simulation tools. Second, in addition to the separation of functionality and architecture, Metro II further separates the modeling of logical quantities (e.g., ordering of events) from the modeling of physical quantities (e.g., physical time and energy consumption), through the concepts of schedulers and annotators. In Metropolis, all quantities are modeled through quantity managers. The clearer separation of logical and physical aspects in Metro II helps analyzing the complex interactions among components and identifying the critical factors for codesign.

There are a number of case studies that have demonstrated the effectiveness of using Metropolis and Metro II in system codesign, from more traditional embedded systems in multimedia [9], telecommunication [10] and automotive [11] domains, to CPSs in buildings [12] and aircraft [13]. For instance, in building design automation [4], [14], a controller model described in Simulink [15] and a building plant model described in Modelica [16] are integrated into Metro II, and cosimulated with an architectural model for performance analysis and communication network synthesis.

B. Ptolemy

The Ptolemy II framework [17] is another modeling and simulation environment that facilities CPS codesign with support for heterogeneity and separation of concerns. The framework supports a variety of MoCs, such as process networks, discrete event, dataflow, synchronous reactive and continuous time, through the concept and implementation of directors. Heterogeneous components that are described with different MoCs can be integrated and cosimulated in a hierarchical model with multiple directors. For instance, a controller component governed by a synchronous dataflow (SDF) director can be integrated with a plant model governed by a continuous-time (CT) director, and cosimulated at the system level under a discrete event (DE) director. The framework also develops domain-specific ontologies for identifying misconnected components (e.g., because of unit, semantic or transposition errors) to ensure correct integration of heterogeneous components [18].

In Ptolemy II, different aspects of a system are orthogonalized based on aspect-oriented programming [19], [20], which share similar ideas to quantity managers in Metropolis. Furthermore, while the framework has mostly focused on functional modeling, it provides the capability for integrating and cosimulating architectural models. In particular, the PTIDES [21], [22] programming model enables clear separation of logical time in functional model and physical time in architectural platform, and ensures timing consistency when functionality and architecture are mapped together (a lightweight microkernel PtidyOS is presented in [23] to facilitate such mapping). The architectural models can be built within Ptolemy II as in [20], or integrated from other tools as shown below in the Metronomy project.

C. Metronomy

Leveraging the strength of Metro II and Ptolemy, the integrated Metronomy framework provides heterogeneous modeling and cosimulation capabilities to facilitate CPS codesign, in particular for verifying system timing behavior during design space exploration [13].

In Metronomy, the functional model is captured in Ptolemy, while the architectural model is described in Metro II, as shown in Fig. 1. At the system level, the two models are integrated and cosimulated through a CoSimDirector, which implements the Metro II execution semantics as a Ptolemy director. The functional model may further contain heterogeneous components—as shown in the figure, a discrete controller model and a continuous physical plant model are cosimulated with a customized discrete event director CoSimDEDirector. On the other hand, the Metro II architectural model can be simulated with a SystemC simulation engine. During model integration, it is compiled with SystemC and Metro II libraries into an executable, which is then cosimulated with the functional model via interprocess communication (governed by the CoSimDirector).

With Metronomy, control engineers or other domain experts can leverage the plethora of MoCs in Ptolemy to capture the functional design of the system. Software/hardware engineers can leverage the flexibility and expressiveness (as well as the libraries of schedulers and

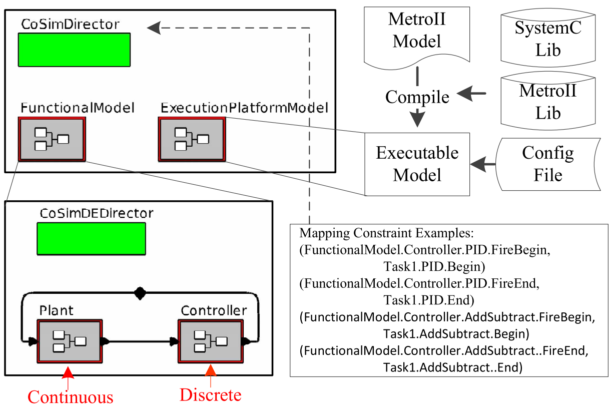
CoSimDirector
FunctionalModel
ExecutionPlatformModel
CoSimDEDirector
Plant
Controller
Continuous
Discrete
MetroII Model
SystemC Lib
Compile
MetroII Lib
Executable Model
Config File
Mapping Constraint Examples:
(FunctionalModel.Controller.PID.FireBegin, Task1.PID.Begin)
(FunctionalModel.Controller.PID.FireEnd, Task1.PID.End)
(FunctionalModel.Controller.AddSubtract.FireBegin, Task1.AddSubtract.Begin)
(FunctionalModel.Controller.AddSubtract..FireEnd, Task1.AddSubtract..End)

Fig. 1. ***Metronomy framework [13].***

annotators) of Metro II to design the architectural platform. System engineers can effectively integrate the two aspects in a cosimulation environment for codesigning various components and verifying the correctness and performance of their designs.

In particular, Metronomy exploits the contract-based design theory [24] to define an interface of timing contracts between the functional model and the architectural model. These contracts can be viewed as a set of timing assumptions and guarantees that are agreed upon between the domain experts who design the system functionality and the software/hardware engineers who implement such functionality on architectural platform. When conducting design space exploration through cosimulation, timing monitors can be implemented in Metronomy to check whether these timing contracts are being satisfied and rule out the infeasible designs.

In [13], Metronomy is applied to the design of two CPSs. In an aircraft electric power system example, a timing contract is set on the end-to-end latency (from sensing to actuation) of a control loop in the system. Through cosimulation of the controller and the implementation platform, different bounds of the timing contract are evaluated with respect to their impact on system performance and stability. The findings are then used to drive the codesign of controller and its implementation platform, e.g., whether a voltage protection mechanism should be added to the controller design when the timing bound is loose, or whether a faster communication bus should be employed in the architectural platform when the bound is tight. In another example of a printing press paper feed system, the sampling period of the paper feed controller and the operating frequency of the implementation processor are codesigned with respect to system performance, also based on cosimulation of the models and verification of the timing contracts.

D. Other Frameworks

There are a number of other academic modeling, simulation and design frameworks for embedded systems and CPSs, such as model-integrated computing

(MIC) [25]–[28], OpenMETA [29], BIP [30]–[32], Compaan/Laura [33], Spade [34], Sesame [35], CAKE [36], ForSyDe [37], MESH [38], Mescal [39], MILAN [40], Giotto [41], CHARON [42], and a compositional real-time scheduling framework [43]–[45] supported by the CARTS tool [46] and the Real-Time Xen visualization platform [47], [48]. There are also popular industrial tools such as MATLAB Simulink [49] and SCADE suite [50], both of which follow the model-based design paradigm [51]–[54].

These frameworks typically start the design with a functional model capturing the system functionality, and then refine it to software and hardware implementations. Some frameworks also provide synthesis tools that explore the design space. For instance, the MIC framework includes a general modeling environment (GME) [55], [56] for creating domain-specific models with a UML-based metamodeling language, a universal data model (UDM) [57] for providing uniform access to the GME metamodels, a graph rewriting and transformation (GReAT) tool [58] for model transformation, and a domain-independent tool DESERT [59]–[61] for generic constraint-based design space exploration. The OpenMETA design automation tool suite [29] provides a model integration platform for precise representation of semantic interfaces among modeling domains and a tool integration platform for automated design space exploration. The model integration platform leverages GME, the model integration language CyPhyML [62] and the formal specification language FORMULA 2.0 [63] to represent components, design spaces and designs, cross-domain interactions, composition constraints, data model interfaces, models of engineering process, and model transformation. The tool integration platform features the DESERT tool for synthesis, and also integrates methods for formal verification, reliability analysis and uncertainty quantification.

The behavior–interaction–priority (BIP) framework provides a rigorous model-based and component-based design flow [30]. As a type of architecture description language (ADL), BIP supports the construction of composite and hierarchically structured components from atomic components, and captures their behavior through layered application of interactions and priorities. More specifically, it uses the concept of connectors to specify interactions between components (as synchronization constraints), and uses priorities to filter possible interactions for further specifying system behavior. The framework has been applied for the modeling and verification of resource-constrained Internet-of-Things (IoT) applications [64], [65]. Recently, DesignBIP [66], a web-based graphical design studio, has been developed to facilitate the specification of BIP models, code generation from the models, and integration with a JavaBIP tool-set [67].

III. SYNTHESIS

Synthesis methods and tools explore a vast and heterogeneous design space, including the sensing, control, computation, and communication algorithms at the functional level, the software and hardware implementation platform, the mechanical components that affect the physical environment, and the human interaction interfaces. The exploration process tries to find feasible or even optimal designs with respect to objectives and constraints on a variety of system metrics, such as performance, safety, security, fault tolerance, reliability, extensibility, energy consumption, and monetary cost.

The synthesis of CPSs has been facing several major challenges.

- The functional complexity of system cyber components is rapidly growing, particularly due to the development of intelligent features and growing system scale. For instance, with the advancement of active safety features, such as those enabling autonomous driving and advanced driver-assistance systems (ADAS), the complexity of automotive electronic systems has increased drastically in the last two decades. Modern vehicles feature about 10–100 million lines of code (up from around 1 million in 2000), thousands of software functions, tens of thousands of functional requirements, and up to 25 GB of data for processing per hour [68]–[70]. Software and electronics were featured in 90% of automotive innovations in 2012, and will continue play a dominant role moving forward [71].
- The architectural platform is becoming more distributed and networked for many CPSs, and using more advanced and complex components. In the automotive domain, the number of electronic control units (ECUs) in luxury cars has more than doubled from under 50 to more than 100 in the past decade [72], and the ECUs are evolving from simple microcontrollers to multicore CPUs with graphics units and hardware accelerators. There is also a fundamental shift from the traditional federated architecture to the integrated architecture, where one function can be distributed over multiple ECUs and multiple functions can be supported on one ECU [73]. This trend leads to significantly more sharing and contention among software functions over the architectural platform, and increases design complexity [74].
- There are strong interdependencies among various components in CPSs. For instance, how effective a control design may affect the physical process significantly depends on the performance and reliability of its cyber implementation with embedded sensing, computation, and communication components. Further, the embedded platform itself is often affected by the physical environment, such as the impact of surrounding temperature on computation and the effect of environmental interference on wireless communication. These interdependencies make it significantly more challenging to explore the design space during synthesis.
- Different system objectives place conflicting requirements on design variables and parameters. For

instance, shorter sampling and control periods usually lead to better sensing and control performance [75], [76], but may be detrimental to schedulability [77]–[81], extensibility, and fault tolerance. Deciding these design variables requires quantitative analysis and careful tradeoffs among various objectives (metrics).

- The physical environment and human activities are dynamic and hard to predict. Consequently, the workload, performance, and requirements for the cyber and mechanical components could change significantly during operation. These uncertainties present great challenges in synthesis—for instance, only considering average case behavior may lead to unreliable or unsafe scenarios, while only addressing worst case behavior could lead to overconservative or even infeasible designs.

These challenges call for new synthesis methodologies and tools that can 1) tackle the functional and architectural complexity with accurate abstractions and efficient design space exploration algorithms; 2) systematically codesign the interdependent cyber and physical components while quantitatively trading off conflicting design metrics; and 3) effectively address the system uncertainties with adaptable, robust, and extensible designs.

Next, we will present our codesign approaches for synthesizing CPSs. These works address codesign in different application domains with a common methodology as follows.

- First, we identify the major factors that affect the interplay among various system components and design metrics, and formulate these factors as a set of interface variables and constraints. The interface variables could be concrete design variables such as sampling periods, or more abstract quantities such as sensing accuracy.
- Second, we analyze and formulate how various design metrics (which may relate to different system components) could be affected by the interface variables and the constraints defined on them.
- Finally, based on the formulation and analysis from the steps above, we develop synthesis algorithms to explore the values of interface variables and constraints as well as other design variables, with respect to design metrics and requirements.

A. HVAC Controller and Sensing Platform Codesign

In [82], we presented an approach to codesign a heating, ventilation, and air conditioning (HVAC) control algorithm and an embedded sensing platform in energy-efficient buildings, as shown in Fig. 2. The codesign is motivated by our observation that the performance and energy cost of HVAC control is significantly affected by the number, location and accuracy of temperature sensors.

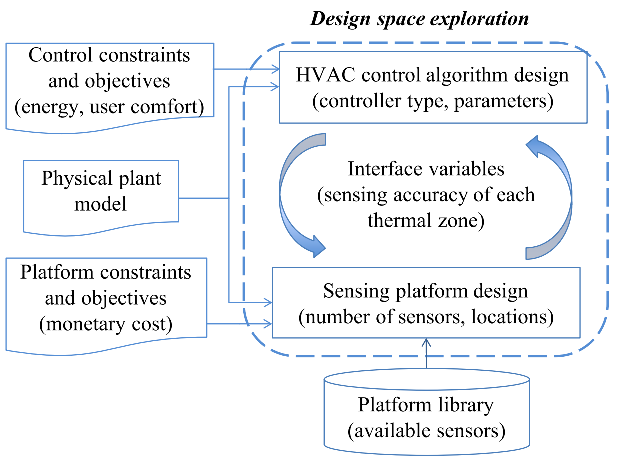
Design space exploration
Control constraints and objectives (energy, user comfort)
HVAC control algorithm design (controller type, parameters)
Physical plant model
Interface variables (sensing accuracy of each thermal zone)
Platform constraints and objectives (monetary cost)
Sensing platform design (number of sensors, locations)
Platform library (available sensors)

Fig. 2. ***Codesign of HVAC control algorithm and embedded sensing platform for energy-efficient buildings.***

In the codesign process, we first define sensing accuracy of each thermal zone, an abstract quantity that depends on the sensor selection and deployment, as the interface variables to capture the interplay between HVAC control and sensing platform design. We then evaluate the control performance (measured by a discomfort index) and energy cost of six control algorithms, ranging from simple ON–OFF control to robust model predictive control (MPC) with extended or unscented Kalman filters, under different levels of sensing accuracy. We leverage the collected data from a building testbed to analyze the relation between the abstract sensing accuracy variable of a thermal zone and the concrete number, location, and accuracy of individual sensors in that zone (which decide the sensing platform cost). Finally, based on these analysis, we explore the codesign of HVAC control algorithm and embedded sensing platform to minimize the energy cost and monetary cost while satisfying the constraints on building tenants' comfort level.

For energy-efficient buildings, holistically addressing heterogeneous components is not only important at design stage but also highly beneficial during operation time. In [83] and [84], coscheduling heterogeneous energy demands (HVAC, electric vehicles charging) and supplies (grid, renewable sources, battery storage) shows a reduction of 4% in energy cost and 15% in peak demand. In [85], coscheduling HVAC control and datacenter operations in mixed-use buildings, with shared energy supplies and cooling infrastructure, shows a reduction of 3%–17% in energy cost and 3% in carbon footprint.

B. Control Performance and Schedulability Codesign

In [81], we presented an algorithm to jointly address control performance and schedulability in controller area network (CAN)-based distributed real-time systems. In this work, the interface variables between the control function-

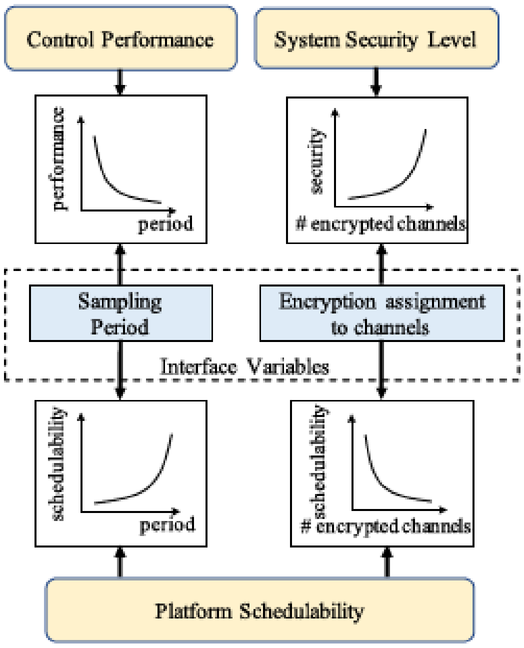

Fig. 3. *Codesign of security, control performance, and schedulability with interface variables [86].*

ality layer and the embedded implementation layer are the activation periods of tasks and messages. These are concrete design variables being explored in our codesign algorithm.

Intuitively, shorter periods for sensing and control tasks often provide better performance, but increase system load and may jeopardize schedulability (assuming the computation time stays at the same). To quantitatively address this tradeoff, the codesign algorithm first approximates the performance of each control loop in the system with a piecewise-linear function of its sampling period and end-to-end delay, and then optimizes the periods of tasks and messages by exploring the linear partitions of the approximated functions and solving a series of geometric programming (GP) problems. The optimization process sets system-level control performance as the objective function, and uses schedulability of tasks and messages as design constraints, along with latency deadlines of functional paths.

C. Security, Control, and Schedulability Codesign

In [86], we presented a cross-layer codesign framework that addresses the tradeoff between security and control performance, while guaranteeing platform schedulability for CPSs. We consider systems where multiple control loops share a common embedded platform, with messages transmitted from sensors (vision sensors, global positioning system, ultrasound, etc.) to controllers and from controllers to actuators. Attackers may eavesdrop on the message communication medium and further reconstruct the system state. This would not only result in a loss of privacy but also lead to other malicious attacks. Security techniques such as message encryption could be applied to mitigate risk, however they will also introduce computation and communication overhead, through the elongation of message transmission time, the addition of decryption tasks on computation units, and consequently the execution time increase of control tasks on the same units due to resource contention. This overhead will in turn have significant impact on system schedulability and control performance, as detailed in [86].

To quantitatively analyze the interplay among control, security, and schedulability, we identify the sampling periods of control tasks and the selection of sensing messages for encryption as the interface variables (Fig. 3). Similarly as discussed above in [81], shorter sampling periods lead to better control performance but worse schedulability, and *vice versa*. Selecting more messages for encryption enhances system security however also worsens schedulability because of the added overhead, in which case the sampling periods may have to be increased to help schedulability (i.e., to ensure each sample can be processed within its period) and thereby lead to worse control performance.

We mathematically formulated the relations between design metrics (security, control performance, schedulability) and interface variables (sampling periods, encryption assignment to messages) in [86]. In particular, the system security level is measured based on either observability Gramian or Kalman filter, and takes into account which messages are encrypted and to what extent. Based on this formulation, a simulated-annealing-based algorithm is developed to optimize security or control performance under schedulability constraints.

Fig. 4 shows the tradeoff between security and control performance when our approach is applied to an industrial example in the automotive domain. The generated Pareto

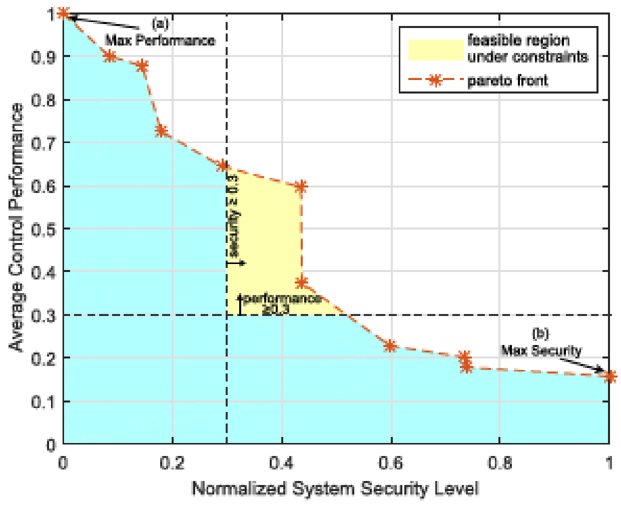

Fig. 4. *Pareto front between normalized security level and control performance for an industrial example [86]. An example feasible region denotes all feasible solutions under requirement that control performance ≥ 0.3 and security level ≥ 0.3.*

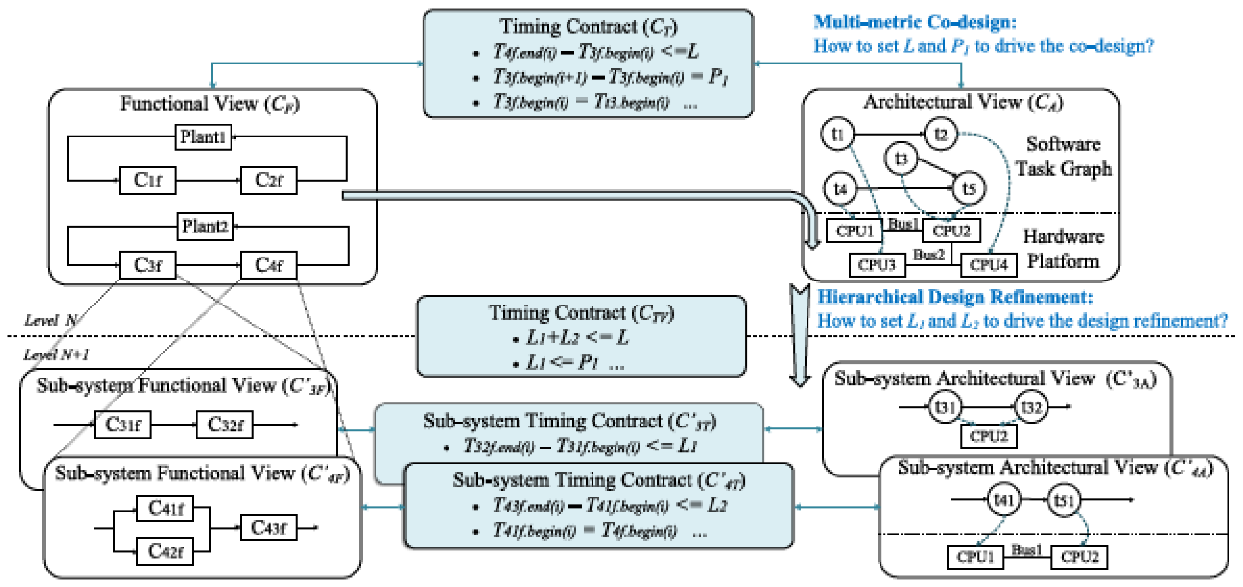
Timing Contract (C_T)
$T_{4f.end(i)} - T_{3f.begin(i)} <= L$
$T_{3f.begin(i+1)} - T_{3f.begin(i)} = P_1$
$T_{3f.begin(i)} = T_{t3.begin(i)}$ ...
Multi-metric Co-design:
How to set L and P_1 to drive the co-design?
Functional View (C_F)
Plant1
C1f
C2f
Plant2
C3f
C4f
Architectural View (C_A)
Software Task Graph
Hardware Platform
CPU1
Bus1
CPU2
Bus2
CPU3
CPU4
Level N
Level N+1
Timing Contract (C_{TF})
$L_1+L_2 <= L$
$L_1 <= P_1$ ...
Hierarchical Design Refinement:
How to set L_1 and L_2 to drive the design refinement?
Sub-system Functional View (C'_{3F})
C31f
C32f
Sub-system Timing Contract (C'_{3T})
$T_{32f.end(i)} - T_{31f.begin(i)} <= L_1$
Sub-system Architectural View (C'_{3A})
Sub-system Functional View (C'_{4F})
C41f
C42f
C43f
Sub-system Timing Contract (C'_{4T})
$T_{43f.end(i)} - T_{41f.begin(i)} <= L_2$
$T_{41f.begin(i)} = T_{4f.begin(i)}$ ...
Sub-system Architectural View (C'_{4A})

Fig. 5. *An illustrating example of timing contracts and their roles in synthesis.*

front provides a quantitative measurement of the tradeoff and identifies a feasible region that is important for making design decisions. For instance, an example feasible region shown in the figure meets the requirements that the normalized control performance should be no less than 0.3 and the system security level should be no less than 0.3. Without codesign, the designers might get a solution that violates security requirement if they only optimize for control performance [point (a) in the figure], or a solution that violates performance requirement if they simply choose to encrypt all messages [point (b)]. This example shows the close interdependency among various design metrics in CPSs and the importance to codesign them.

D. Timing Contracts for Codesign

Timing is a central element in CPS synthesis, affecting both functional correctness and various design metrics. Thus, timing variables and constraints are often identified as the interface to drive the codesign. Two examples are already introduced above—task and message activation periods along with end-to-end delays are the interface variables to drive the control performance and schedulability codesign in [81], while control sampling periods are part of the interface variables to drive the codesign of security, control performance, and schedulability in [86]. There could be many other types of timing variables and formulations of timing constraints. Below, we present a general methodology for timing-driven codesign and synthesis based on exploration of timing contracts.

The paradigm of contract-based design provides the general methodology of using contracts to reduce design complexity and represent design refinement [24], [87]–[91]. However, the exploration of timing contracts has typically been done manually or is limited to simulation-based approaches (as in our prior work [13] introduced in Section II), and it has not been used sufficiently to drive the synthesis process. Next, we use an illustrating example to demonstrate our ideas in timing contracts exploration for synthesis.

1) Multimetric Codesign With Timing Contracts: In Fig. 5, at abstraction level N, a functional view (viewpoint) C_F, and an architectural view C_A are defined to capture the system's functional behavior and architectural platform, respectively. In the contract-based design paradigm, both C_F and C_A can be defined as contracts that provide guarantees under assumptions, where guarantees and assumptions are specified as a set of assertions/constraints. In addition to C_F and C_A, a timing contract/view C_T is defined to capture the system's timing behavior and constraints.[1]

The conjunction of C_F and C_T (denoted as $C_F \sqcap C_T$, with formal definition introduced in [24] and [87]) defines the system's functional behavior under timing assumptions/constraints defined in C_T. For instance, in the figure, it defines the functional behavior when the end-to-end (sensor-to-actuator) latency of a control loop including components (subsystems) C_{3f} and C_{4f} is within L, and when the control loop's sampling period is P_1 (corresponding to the activation period of sensing component C_{3f}, where $T_{3f.end(i)}$ denotes the time associated with the end of the ith execution of C_{3f}, with other notations similarly defined). This behavior relates directly to the system's functional correctness, control performance, sensing accuracy, and other metrics related to functionality and timing.

[1]C_T may be further refined into functional and architectural timing contracts to facilitate analysis and function-architecture cosimulation as in [13].

The conjunction of C_A and C_T (i.e., $C_A \sqcap C_T$) defines the system's architectural behavior under timing constraints. This may relate directly to metrics such as schedulability, extensibility, and fault tolerance.

Often the timing constraints have opposite impact on different metrics. As discussed above, shorter end-to-end latencies and sampling periods (e.g., smaller values of L and P_1 in Fig. 5) usually lead to better performance but worse schedulability. The goal in codesign with timing contracts is to answer: how to systematically set the timing constraints as contracts between different views when considering multiple conflicting design metrics? For instance, what values should L and P_1 be to provide the best control performance while ensuring schedulability? What about to ensure certain control performance level while providing the best extensibility?

Our work introduced above [81], [86] is a first attempt at addressing these questions. The general methodology includes the following aspects.

- Timing contracts formulation: Depending on system characteristics and design focus, the constraints in timing contracts could take various mathematical formalisms. Linear, quadratic, exponential, or other functions can be used to form constraints on timing-related variables. Logic operators (e.g., conjunction, inclusive or exclusive disjunction, existential qualification) can be used for defining logic relations, particularly those related to resource contentions. More generally, formalisms such as linear temporal logic (LTL) [92], real-time logic (RTL) [93], signal temporal logic (STL) [94], logic of constraints (LOC) [95], and logical execution time (LET) [41] can be used to capture the complex requirements on timing variables and events. Leveraging these mathematical formalisms, the key in defining contracts is to identify the critical timing factors for codesign, and choose the right abstraction levels and formalisms to capture them with constraints. For instance, sensitivity analysis based on estimation and simulation can be used to evaluate whether end-to-end latencies have significant impact on extensibility, and if so, which path latencies are the most critical. Timing constraints are defined at event level (e.g., timing order between events) in [13] to drive simulation-based exploration, and defined at task and component (functional block) levels in [81], [86], and [96] to facilitate analytical synthesis algorithms. Different activation patters (e.g., periodic, sporadic, or aperiodic) and timing models (e.g., worst case, average case, or probabilistic models) could be used to define events, components, and tasks. Constraints could include hard, firm, or soft deadlines, or weakly hard deadlines that are allowed to be violated based on a defined pattern (e.g., at most m violations in any k consecutive instance) [97].
- Design metrics modeling and formulation: Once timing contracts are formulated, the next step is to derive the relations between various design metrics and the timing variables/constraints in the contracts. In some cases, these relations can be captured in closed-form formulations, such as the relation between security level and the selection of sensing messages for encryption in [86]. In other cases, approximated formulations, simulation-based curve fitting, or direct integration with simulators may have to be used, such as the relation between control performance and activation periods in [81].

  In addition to control performance, security, and schedulability, many other design metrics significantly depend on system timing behavior and should be addressed in codesign with timing contracts. For instance, extensibility represents how much a system may be changed without major redesign and reverification effort, which is imperative for large-volume and long-lifetime CPSs such as automotive and avionics systems. In our prior work [98]–[100], extensibility metrics are defined to measure how much task (or action) execution time can be increased without violating design constraints. These metrics depend on timing constraints, architectural platform factors, and synthesis choices, and should be codesigned with other metrics. Another important metric is fault tolerance. In [101], a fault tolerance metric measures the likelihood of soft errors being detected and corrected through embedded error detection (EED) or explicit output comparison (EOC) approaches without violating timing constraints. The tradeoff between fault tolerance and other metrics such as extensibility and communication cost are evident in our recent study [102], and should be addressed with timing contracts.
- Multimetric codesign algorithms: Once the timing contracts and the design metrics are formulated, synthesis algorithms need to be developed for exploring timing constraints and other design variables (e.g., task generation, allocation, and scheduling). In general, the exploration can be formulated as a constrained multiobjective optimization problem and is often NP-hard. Randomized algorithms such as simulated annealing can be applied in many cases, however, the complexity usually makes it difficult to obtain good (or even feasible) solutions for practical systems.

  For some systems and metrics, the problem may be formulated in an integrated formulation with closed-form representations of all objectives and constraints. In these cases, techniques such as mathematical programming, greedy heuristic, dynamic programming, or a combinational of them could be applied to balance algorithm optimality and complexity. For instance, mixed-integer linear programming, geometric programming, and their combination with heuristics are used in our prior synthesis work [81], [98], [99], [103]–[107]. In some cases, for complexity concern, it is necessary to develop separate exploration engines for timing constraints, for task generation, allocation and scheduling, for communication synthesis, and for other design variables (e.g., CPU frequencies as architectural variables, control algorithm parameters as functional variables), and to efficiently iterate among these engines for joint optimization.

2) Hierarchical Design Refinement With Timing Contracts: The above timing contracts for codesigning multiple design metrics can be regarded as "horizontal" contracts between different views. There are also "vertical" timing contracts that could be defined to facilitate the design refinement across abstraction levels, which may be viewed as codesign of multiple components (subsystems).

Using Fig. 5 as an example, at the lower abstraction level $N+1$ of the system, each functional component is refined to lower level components. Functional view C'_{3F} and C'_{4F} are refined from components C_{3f} and C_{4f} at level N. Correspondingly, architectural views C'_{3A} and C'_{4A} refine parts of the architectural platform to which C_{3f} and C_{4f} are mapped. For instance, task t_3 may be a virtual task (i.e., not corresponding to a software task in the operating system) at level N, and is refined to lower level tasks t_{31} and t_{32} at level $N+1$. Tasks t_4 and t_5 at level N are refined to tasks t_{41} and t_{51} at level $N+1$, respectively.

During implementation, functional components are mapped to the tasks in architectural views at the corresponding level. For instance, in Fig. 5, C_{3f} is mapped to t_3 at level N, and C_{4f} is mapped to t_4 and t_5. At the lower level $N+1$, C_{31f} and C_{32f} are mapped to t_{31} and t_{32}, respectively (both tasks are running on $CPU2$). C_{41f} and C_{42f} are mapped to t_{41} running on $CPU1$, and C_{43f} is mapped to t_{51} running on $CPU2$. Note that both many-to-one and one-to-many mapping between functional components and architectural tasks are allowed for generality and flexibility.

Timing contracts C'_{3T} and C'_{4T} are defined and should be consistent with C_T, through constraints defined in the vertical timing contract C_{TV}. For instance, in systems that are designed following the synchronous assumption [96], [108], the end-to-end latency deadline from the beginning of C_{31f} to the end of C_{32f} (denoted by L_1) should be within the activation period P_1 of C_{3f}, to ensure that each activation of C_{3f} can be completed before its next activation. Furthermore, the sum of the end-to-end latency deadlines of C'_{3F} and C'_{4F}, denoted as L_1 and L_2, respectively, should be within the entire control path deadline L at level N. There are also timing constraints across architectural views at different abstraction levels in C_{TV}, and constraints between functional components and architectural tasks in C'_{3T} and C'_{4T} (e.g., setting $T_{31f.(i)} = T_{t31.\mathrm{begin}(i)}$ to synchronize the execution of C_{31f} and t_{31}). For simplicity, they are not shown in Fig. 5.

The goal in hierarchical refinement with timing contracts is to answer: How to assign timing "budget" as contracts for each lower level component, which has significant impact on the design of each subsystem and the overall system quality? For instance, assuming L is set to 200 ms, we will need to address questions such as " if we set L_1 to 100 ms and L_2 to 100 ms, can we find feasible implementations/mappings for C_{3f} and C_{4f}?"; "What if we set L_1 to 80 ms and L_2 to 120 ms, will it provide better extensibility for the system?"; and so on. This is challenging to address since often the timing budgets (constraints) have to be decided before the corresponding lower level components are designed (their design choices depend on the timing budgets themselves and are often carried out by different teams). Furthermore, in practical systems, there are often multiple timing constrains for each lower level component, and components that do not share the same functional path may also impact each other if they share resources on the architectural platform.

There are two important aspects in using timing contracts to address these challenges.

- Vertical timing contracts formulation: The formulation of vertical contracts may leverage the similar mathematical formalisms as discussed above for horizontal contracts. Furthermore, the vertical contracts should be able to capture timing behavior and constraints across the hierarchical structure of systems. For instance, in [96], we presented a formulation called firing and execution timing automata (FETA), which can capture the periodic timing behavior of runnables at functional layer and of software tasks at embedded platform layer. The hierarchical composition of FETAs further corresponds to the mapping of multiple runnables to a task. Having such unified FETA formalism enables cross-layer timing analysis during synthesis, and could be leveraged in formulating vertical timing contracts.
- Hierarchical timing budgets exploration: Once the vertical timing contracts are formulated, synthesis algorithms are needed for exploring timing budgets during design refinement. One direction is to develop methodologies for a first estimation of the timing complexity of components, which measures how much impact a component may have on certain timing-related design metric (e.g., schedulability, extensibility, fault tolerance). Different timing complexity measurements may be required for different metrics. As an example, for schedulability, the concepts of local utilization and alpha ratio based on FETA in [96] are shown to be effective in estimating the impact of individual runnables on system schedulability.

The estimations of timing complexity for components can then be used to drive the timing budgets assignment and ultimately the design of components, such as the software task generation and mapping for them. For example, in Fig. 5, L_2 needs to be set to drive the task generation and mapping for C_{41f}, C_{42f}, and C_{43f}. To achieve effective exploration, an iterative approach between the timing budgets assignment and the task generation and mapping is needed.

E. Other Works

There are a number of other papers that address multiple system aspects and objectives in the synthesis of CPSs. In [105], we addressed both security and timing safety requirements in mapping software tasks onto CAN-based automotive platforms. We used message authentication codes (MACs) to protect against masquerade and replay attacks on CAN networks, and developed a mixed-integer linear programming (MILP) formulation and a greedy heuristic algorithm for exploring task allocation, signal packing, MAC sharing, and priority assignment while meeting security and timing constraints.

The work in [105] improves security for CAN-based systems by addressing it together with other design concerns during the synthesis process. However, with limited bandwidth and message size, it is still very challenging to apply authentication mechanisms such as MACs on CAN networks. In [106], we further addressed security issues for next-generation automotive buses that use time-division multiple-access (TDMA) communication, such as time-triggered Ethernet [109], FlexRay [110], or time-sensitive networking [111]. We used an authentication mechanism with time-delayed release of keys, and developed an algorithm to jointly address security and timing requirements by exploring task allocation, priority assignment, network scheduling, and key-release interval length. Experiments based on time-triggered Ethernet demonstrate that both security and timing requirements can be met through the joint formulation and synthesis—and may not be met if the authentication mechanism is applied after task synthesis, even with the much larger bandwidth and message size than CAN. Following the work in [105] and [106], we proposed a general methodology for addressing security and other system objectives together during synthesis, and apply it to a vehicle-to-vehicle (V2V) application [112].

In [96], we developed a model-based synthesis flow for automotive software systems that follow the AUTOSAR standard [113]. The synthesis flow optimizes the generation of AUTOSAR runnables from synchronous functional models, the mapping of runnables onto software tasks, and the allocation of tasks onto ECU cores. It introduces the formalism of FETA to capture the worst case execution time (WCET) of functional blocks, runnables, and tasks at each activation, and then leverages the unified FETA formulation to model system timing behavior and address timing constraints throughout the entire synthesis process. Furthermore, the synthesis flow considers a variety of software engineering objectives (runnable modularity, reusability, code size, memory cost) with timing behavior in a holistic fashion. In particular, the flow focuses on trading off modularity with schedulability during runnable synthesis, and on minimizing memory cost under schedulability constraints during task synthesis. The results demonstrate the importance of using a codesign methodology in synthesis and addressing timing across the layers of functional model, runnable, and software tasks. In [108], a similar codesign formulation was developed for direct generation of tasks from synchronous models, with respect to modularity, reusability, code size, and latency.

For control applications, there are various efforts on conducting controller design with the consideration of platform impact (e.g., timing delay, packet dropping, and scheduling policy) [75], [77]–[80], [114]–[131]. In [132], Roy *et al.* discussed the issues in traditional isolated process of controller design and implementation platform design, in particular the challenges in preserving model-level semantics and safety properties during the transformation of high-level controller models into implementations. They then provided a comprehensive review of recent efforts in control-platform cosynthesis, in which the control algorithms and platform parameters are designed together.

IV. VERIFICATION AND VALIDATION

Verification and validation tools are essential in codesigning CPSs. They ensure that system specification satisfies user and mission requirements, and system implementation meets the specification. Similarly as for synthesis, verification and validation face significant challenges from increasing functional complexity, distributed and networked architectural platform, heterogeneous system components, and stringent requirements on various system metrics. They not only have to guarantee functional correctness, but also need to ensure that requirements on nonfunctional properties (e.g., performance, security, reliability) are met. Moreover, properties that are often regarded as nonfunctional in traditional computing systems, such as timing behavior, may have significant impact on functional correctness in CPSs. The close interaction between discrete cyber components and continuous physical domain, as well as the uncertainties from dynamic environment and human activities, presents further challenges in CPS verification and validation.

Next, we will first present our approach to tackle CPS verification challenges, which combines platform-aware functional verification with constrained platform synthesis in a common framework. We will then introduce the application of this methodology in a cross-layer codesign and verification framework for connected vehicles.

A. Collaborative Functional Verification and Platform Synthesis

In current practice, verification of system's functionality (abstracted through a functional model) is often conducted without much consideration of the underlying architectural platform. On the other hand, synthesis methods that explore platform design choices are often oblivious of the high-level functional requirements. Such disconnected

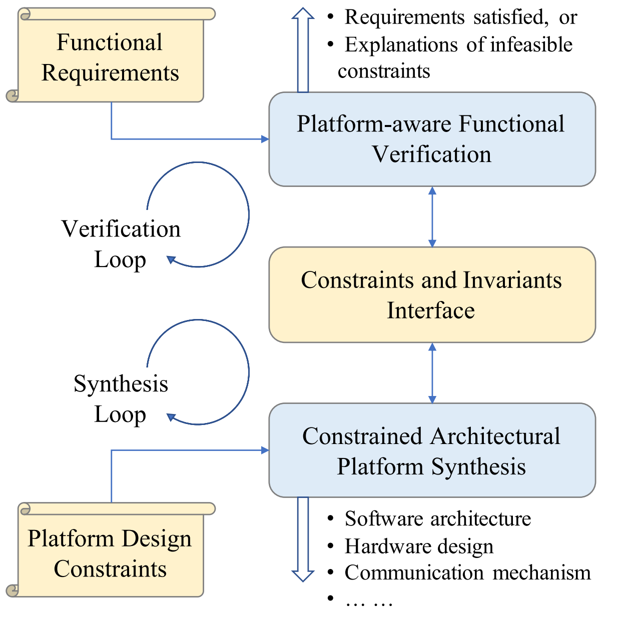
Functional Requirements
Requirements satisfied, or
Explanations of infeasible constraints
Platform-aware Functional Verification
Verification Loop
Constraints and Invariants Interface
Synthesis Loop
Constrained Architectural Platform Synthesis
Platform Design Constraints
Software architecture
Hardware design
Communication mechanism
… …

Fig. 6. ***Collaborative functional verification and platform synthesis framework for CPSs.***

approach may be feasible for traditional computing systems in which functional and nonfunctional properties can be clearly separated. However, it is unsuitable for many CPSs where nonfunctional quantities such as timing and reliability have direct and complex impact on system correctness, and using it could easily lead to infeasible designs (i.e., either cannot be verified with respect to system properties or cannot be implemented successfully) or inferior designs. In [133], we proposed a collaborative functional verification and platform synthesis framework for integrating the two currently separated steps in the design cycle, as shown in Fig. 6.

The idea in our approach is to divide the problem of verifying CPSs into two collaborative subproblems: 1) functional verification under constraints and invariants guaranteed by synthesis (e.g., verifying safety property when assuming sensor-to-actuator delay is within certain bound $[D_{\mathrm{MIN}}, D_{\mathrm{MAX}}]$); and 2) software/hardware platform synthesis under constraints and invariants specified by verification (e.g., synthesizing software design while meeting the same bound $[D_{\mathrm{MIN}}, D_{\mathrm{MAX}}]$ on sensor-to-actuator-delay).

The constraints and invariants interface can be viewed as a contract between functional verification and platform synthesis. For instance, the above example of "sensor-to-actuator delay is within bound $[D_{\mathrm{MIN}}, D_{\mathrm{MAX}}]$" is in fact an assume/guarantee contract, where the verification process assumes the delay bound will be guaranteed in the synthesis result. Thus, our framework integrates two essential aspects in CPS design and solve them systematically. By formalizing and managing the exchange of constraints and invariants through the verification-synthesis interface in coupled iterations, this approach could significantly improve the efficiency of both verification and synthesis. Next, we will introduce how we apply this methodology in codesigning and verifying connected vehicle applications, by analyzing the impact of communication delays and message losses on functional properties.

B. Cross-Layer Design and Verification of Connected Vehicles

Next-generation autonomous and semi-autonomous vehicles will not only percept the environment with their own sensors, but also communicate with surrounding vehicles and infrastructures to improve vehicle safety and transportation efficiency. The design, verification, and validation of various V2X [i.e., vehicle-to-vehicle (V2V) and vehicle-to-infrastructure (V2I)] systems involve multiple layers, from application functionality to vehicular communication networks and to the software and hardware of individual vehicles [134]. They are concerned with stringent requirements on timing, safety, security, dependability, cost, and resources across these layers.

The underlying sensing, computation, and communication platform, within vehicles and between them, fundamentally influences the correctness of functional properties at the V2X application layer. For instance, the time it takes a vehicle to broadcast its position, velocity, and acceleration to nearby vehicles has a significant impact on the size of safety zones in which the vehicles can collaboratively perform collision avoidance [133]. This timing is in turn influenced by many platform decisions and factors, such as the choice of sensors and their accuracies, the availability and capability of computation resources, the in-vehicle communication latencies over buses, the design of V2X communication protocol and the environment disturbance on such communication, and the overhead incurred by added security measurements for V2X and in-vehicle communications. Thus, the correctness of a functional property at the application layer, such as "vehicles in a platoon should always maintain a safe distance from one another," inherently depends on the design decisions and execution behavior of the underlying platform.

Based on the above observation, we have been developing CONVINCE, a cross-layer modeling, exploration, and validation framework for connected vehicles (Fig. 7). One of the ideas of CONVINCE is to integrate the functional verification of V2X and self-driving applications with platform synthesis of inter-vehicle communication and intra-vehicle (software and hardware) architecture, following the general methodology introduced earlier in this section. The CONVINCE framework includes mathematical models, synthesis, verification and validation algorithms, and a heterogeneous simulator in a holistic environment. As shown in Fig. 7, it explores a variety of design options with respect to constraints and objectives across system layers, and it takes into consideration of environment disturbance and possible security attacks.

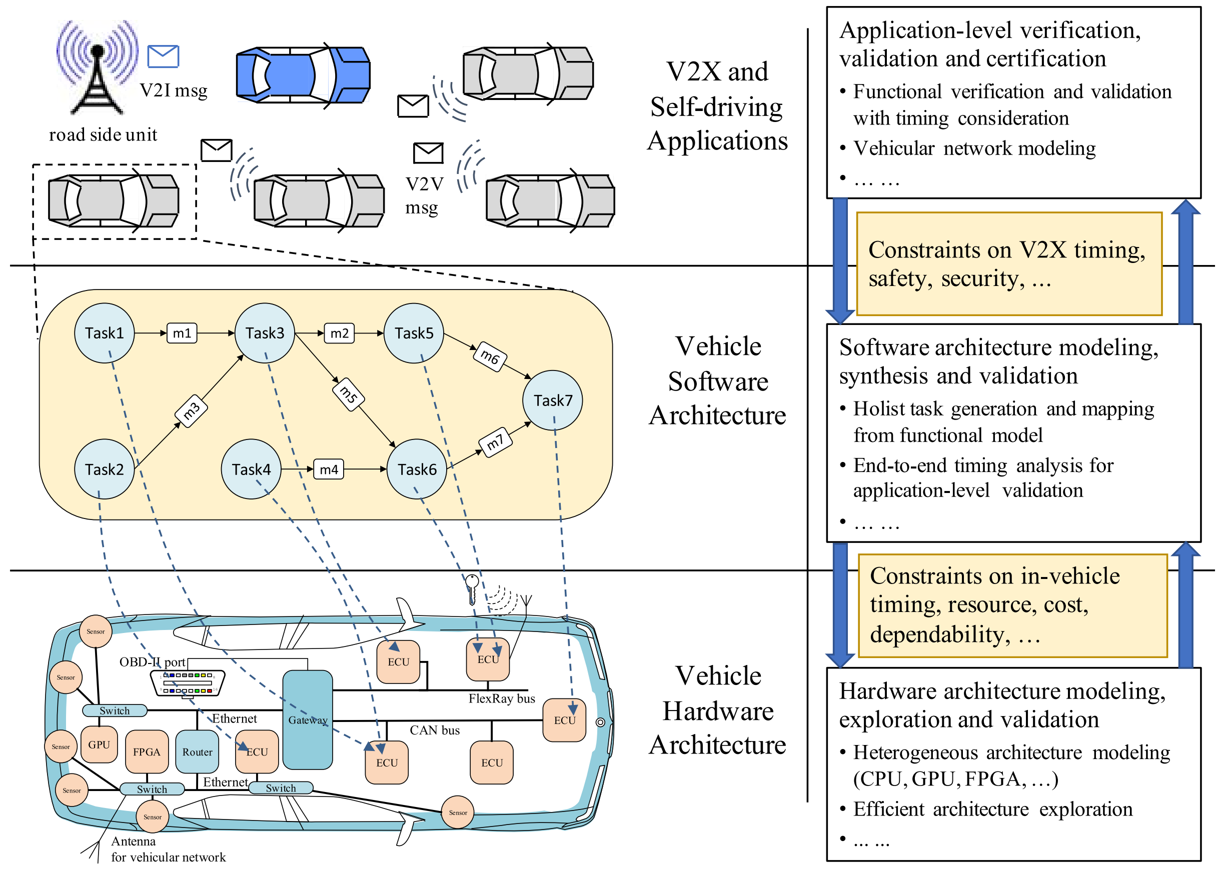
V2I msg
road side unit
V2V msg
V2X and Self-driving Applications
Application-level verification, validation and certification
• Functional verification and validation with timing consideration
• Vehicular network modeling
• … …
Constraints on V2X timing, safety, security, …
Task1
Task2
Task3
Task4
Task5
Task6
Task7
m1
m2
m3
m4
m5
m6
m7
Vehicle Software Architecture
Software architecture modeling, synthesis and validation
• Holist task generation and mapping from functional model
• End-to-end timing analysis for application-level validation
• … …
Constraints on in-vehicle timing, resource, cost, dependability, …
Sensor
OBD-II port
Switch
Ethernet
Gateway
ECU
FlexRay bus
CAN bus
GPU
FPGA
Router
Antenna for vehicular network
Vehicle Hardware Architecture
Hardware architecture modeling, exploration and validation
• Heterogeneous architecture modeling (CPU, GPU, FPGA, …)
• Efficient architecture exploration
• … …

Fig. 7. *CONVINCE: Cross-layer modeling, exploration, and validation framework for next-generation connected vehicles.*

In [134], we presented the preliminary design of CONVINCE and a case study of the collaborative adaptive cruise control (CACC) application, where every vehicle communicates with its preceding vehicle and adaptively maintains a safe distance. Through mathematical analysis and simulations, the case study demonstrate the impact of V2V communication delays on the performance of CACC.

In [135], we applied CONVINCE to the design of centralized autonomous intersection management, a complex V2X application that is significantly affected by the underlying platform. In a centralized autonomous intersection, an intersection manager accepts requests from approaching vehicles via V2I messages and schedules the order for those vehicles to cross the intersection. Previous papers in the literature assume perfect communication between vehicles and infrastructures, and do not explicitly consider communication delays [136]–[140]. However, significant message delays (up to several hundred milliseconds in the worst case) and losses could happen in vehicular network under dense traffic [141]–[143], and the situation could be even more severe when the communication channels are under malicious jamming or flooding attacks [134], [144]. In those cases, the previous approaches that lack consideration of messages delays and losses may lead to system deadlock or unsafe situations.

To address the above issue, we presented a delay-tolerant intersection management protocol in [135], and applied CONVINCE for the modeling, simulation, and verification of the protocol. The framework is able to verify that the protocol's safety property is guaranteed under any circumstance, and that its liveness and deadlock-free properties are guaranteed if the maximum communication delay is bounded and known. This bound should then be used as a constraint for the synthesis of the underlying communication and computation platform, i.e., as a constraint in the verification-synthesis interface in Fig. 6. Simulation results also demonstrate that 1) our protocol may significantly improve the intersection efficiency in normal situations (i.e., communication delay is within hundreds of milliseconds); and 2) the protocol performance worsens when communication delay increases, and thus it is important to quantitatively analyze such impact and be able to answer questions such as "for autonomous intersection to outperform traffic lights, what bound should the communication delay satisfy and how to ensure such bound in platform synthesis."

V. CONCLUSION AND FUTURE DIRECTIONS

We discussed the importance and challenges of holistically addressing modeling, synthesis, and verification of CPSs. We presented emerging design methodologies, algorithms, and tools for addressing CPS codesign, and introduced their applications in domains such as automotive systems, vehicular networks, and energy-efficient buildings.

There are still many open challenges remaining in CPS codesign. Below, we discuss some promising future directions for addressing them.

- Automated model generation and update: While a number of model-based frameworks have been proposed for capturing and analyzing CPSs (some of which are introduced in Section II), developing and maintaining those formal or semiformal models remains quite challenging in practice. There is typically a steep learning curve for designers to get familiar with the syntax and semantics of the frameworks, and to effectively apply them in modeling complex systems. This is especially the case in CPS codesign, as designers often need to model intrinsically heterogeneous components with different semantics and/or languages. The model development process is usually time-consuming and error-prone, and maintaining and updating the models throughout their lifetime may take even more effort. Thus, developing an automated or semiautomated process for model generation and update is of great interest. We envision an environment where designers only need to provide high-level informal descriptions of the system (e.g., in English) and models are automatically generated/updated based on those descriptions. To realize this, advanced techniques such as natural language processing (NLP) could be leveraged, as well as intuitive graphical interfaces and comprehensive design libraries. In addition, an interactive human-tool interface, in which designers could incrementally check, query, and modify the models, should facilitate the model development/update process (an interactive interface should also facilitate synthesis and verification as discussed below). Automated abstraction/rewriting techniques such as "lifting" are also promising directions [145].
- Agile model abstraction and integration: CPS codesign requires integration of heterogeneous cyber and physical components that are captured at various levels of abstraction. Moreover, based on the specific codesign problems, different abstraction levels may be chosen for the same component. For instance, in our approach to the codesign of an HVAC controller and sensing platform for buildings [82], a simplified resistor–capacitor (RC) network model from [146] is used to capture the room thermal dynamics, and is shown to be effective for facilitating the choices on different controllers and sensors. This model, however, may not be sufficiently accurate for designing the controllers. Detailed thermal dynamics models (such as the ones built in EnergyPlus [147]) could provide the needed accuracy but are often too complex for control design. Thus, models that are between these two abstraction levels need to be explored, through techniques such as model order reduction [148], [149] and data-driven modeling [150]–[155]. From the perspective of codesign tools, it is important to facilitate agile exploration of different model abstractions, such as the exploration of different thermal dynamic models in building design and operation. This will require well-defined component interfaces and system execution semantics that can support "plug-and-play" of models at different abstraction levels.
- Comprehensive cross-layer cosynthesis: The design of sensing, control, computation, and communication algorithms at the functional layer is closely intertwined with the embedded software and hardware design at the platform layers. The codesign/cosynthesis approaches presented in Section III analyze and leverage such cross-layer interdependencies to improve the overall system metrics such as performance, safety, and security. While showing promising results, these approaches have only explored the surface of cross-layer cosynthesis in CPSs. There is great potential to further investigate the interactions between CPS components across different system layers, discover and quantify the dependencies in their design choices, and develop holistic formulations and algorithms to cosynthesize them. For instance, HVAC control algorithms may be codesigned with the sensing platforms from scratch, beyond just being selected from existing controllers as in [82]. Vision-based sensing algorithms could be codesigned with the computation and communication platforms to enable efficient real-time video processing, as we started exploring in [156].
- Efficient algorithms for exploring heterogeneous design space: Compared with traditional embedded systems, codesign problems in CPSs often involve a more heterogeneous and complex design space. The problem formulations could include a large number of discrete and continuous design variables, and many nonlinear or even nonconvex constraints. Thus, when developing algorithms to explore such design space, it is usually infeasible to directly apply mathematical programming techniques such as linear programming and geometric programming, and ineffective (too slow or too far from the optimal solutions) to directly use randomized methods such as simulated annealing and genetic algorithms. New approaches need to be developed for efficient exploration of the heterogeneous codesign space in CPSs. Techniques such as approximation algorithms, greedy heuristics, parallel

randomized search, and learning-based methods are promising directions for tackling complexity. Furthermore, methods that can quickly estimate the bounds of design metrics for partial solutions (i.e., when only part of the design variables are decided) should facilitate pruning the design space and accelerate the exploration process.

- Interactive synthesis and verification interface: CPS design is often an iterative process, during which the system specifications and constraints are continuously refined and the tradeoffs among different metrics are constantly carried out. It is therefore important to develop an interactive interface between designers and design tools (e.g., synthesis and verification tools), to enable flexible additions and updates of specifications/constraints, and to support designer queries such as "is it possible to further improve metric A?" and "what if constraint X is removed or relaxed by quantity Y?" This interface will facilitate a nimble design process, better leverage designers' expertise, and ultimately improve design quality and productivity. To realize such interface, new synthesis and verification tools are needed to assess system feasibility (with respect to both functional and nonfunctional requirements) under an incomplete set of constraints, estimate the bounds of design metrics for all feasible implementations (if there are any), identify design bottlenecks when there is no feasible solution or certain metrics are not good enough, and leverage previous synthesis/verification results (rather than restarting from scratch) when new constraints are added or existing ones are modified.
- Runtime coadaptation: While this paper mostly focuses on tools and methods for design-time modeling, synthesis, and verification of CPSs, it is equally important to investigate and leverage the interdependencies between components for runtime adaptation of CPSs, especially for those systems that operate in uncertain environment and with changing missions. For example, when a robot faces adversarial environment, it could holistically adapt its operation across system layers by adopting more robust sensing and control algorithms, applying stronger security mechanisms in software and hardware, and possibly reducing nonessential tasks to meet resource constraints. When an intelligent building detects emergency situations (e.g., fire or breakout), it could adapt to a different operation mode, with changes across HVAC and lighting control algorithms, computation and communication infrastructures, and sensing platforms. Such level of coadaptation will require new synthesis and verification methods that are efficient and reliable enough for runtime usage. For instance, fast online algorithms could be developed with the help from offline synthesis/verification that consider different operating scenarios.

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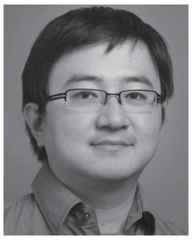

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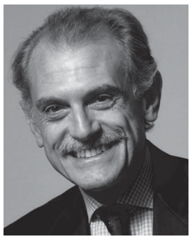

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