AC Computing Methodology for RF-Powered IoT Devices

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***Abstract*—An AC computing methodology is proposed for integration into wirelessly powered devices such as RF tags and sensor nodes. Contrary to traditional platforms that integrate DC-powered computational logic along with the rectification and regulation stages, in the proposed approach, the harvested RF signal is directly used to power the data processing circuitry by leveraging charge-recycling and adiabatic circuit theory. A near-field based wireless power harvesting system with an 8-bit arithmetic logic unit (ALU) is developed to evaluate the proposed framework. Simulation results in 45 nm technology demonstrate that the overall power consumption can be reduced by up to 16 times as compared to the conventional approach that relies on AC-to-DC conversion and static CMOS logic. This reduction in power enables significant computation capability for RF-powered devices. Several important characteristics such as the impact of circuit size on overhead and processing power, impact of voltage scaling on circuit operation and power consumption are investigated. Some important design issues and related tradeoffs are also discussed.**

***Index Terms*—AC computing, Adiabatic, Charge-recycling, Energy harvesting, RF tags, IoT, Sensor nodes, Wireless power.**

I. Introduction

POWER delivery is one of the fundamental limitations for future Internet of things (IoT). The advances in conventional electrochemical battery technologies have been relatively limited as compared to unprecedented progress in computing capabilities. The wide and growing gap between these two trends is a serious concern to the predicted scalability of IoT devices.

Power harvesting methods have long been considered for traditional wireless sensor nodes and emerging IoT devices. Some examples include photovoltaic, electrostatic or piezoelectric, thermoelectric, and RF or inductive energy converters [1], [2]. Computing techniques in the presence of unpredictable power sources have also received attention [3].

Wireless power transmission has become more common during the past decade due to popular applications such as RFIDs, wireless charging, and RF-powered bio-implantable devices [4]–[7]. Harvesting wireless RF power has the potential to provide a relatively more stable energy, considering the presence of dedicated energy sources (RF exciter or RFID reader) or the abundance of ambient communication and broadcast signals (such as TV/radio broadcast, mobile and Wi-Fi transmitters) [8], [9].

In a conventional wireless energy harvester, the propagating electromagnetic wave is received with an antenna or coupling coil. The harvested alternating signal is then converted into a DC signal through rectification, voltage multiplication, and regulation [10]. The power efficiency of these processes is typically low, particularly when the harvested input power is very small as in typical energy harvesting systems [11]–[13].

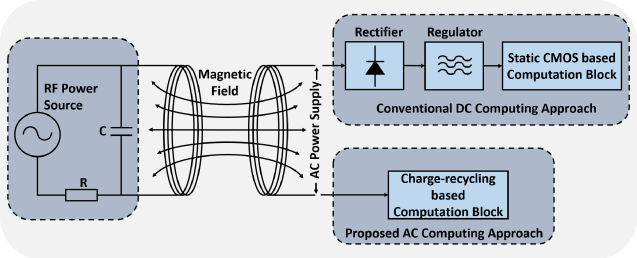

Fig. 1: AC computing methodology vs. conventional approach for RF-powered devices.

Recently, an AC computing methodology has been developed for wirelessly powered devices [14]–[16], as conceptually illustrated in Fig. 1. In this method, the harvested AC signal is used to power the digital logic while eliminating the lossy rectification and regulation stages. The AC signal is used as both the power and clock signals by leveraging adiabatic and charge recycling circuits. Significant power is saved by (1) eliminating AC-to-DC conversion and (2) recycling charge during the operation of digital circuits. Charge-recycling logic is re-engineered for the implementation of the processing circuitry that is powered by the AC signal. These existing works, however, did not include a comprehensive evaluation framework consisting of a realistic wireless link and practical logic circuit. Furthermore, some of the critical implementation details for high energy efficiency were not described. This paper mitigates these limitations of prior work while introducing the following contributions for a more comprehensive understanding of AC computing:

- Three different implementations of the methodology are proposed and evaluated with a comprehensive case study for brain implantable devices with near-field based wireless power transfer.
- The effect of circuit size on both overhead and processing power is investigated for the proposed methods and the conventional approach.
- The behavior of the proposed methods under scaled voltages is investigated and compared with the conventional approach.
- The advantages and limitations of the proposed methods are qualitatively discussed, thereby identifying related tradeoffs and providing useful design guidelines.

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The rest of the paper is organized as follows. In section II, previous work related to AC computing is summarized. Background on charge-recycling operation is provided in Section III. The proposed AC computing approach for wirelessly powered devices is described in Section IV. Simulation results are presented in Section V, demonstrating more than an order of magnitude reduction in overall power consumption. Important design considerations and related tradeoffs are discussed in Section VI. The paper is concluded in Section VII.

II. Summary of Previous Works

In earlier research on AC computing, a very low frequency (60 Hz - 300 Hz) AC power supply was proposed for wirelessly powered devices [17]. Since the power supply frequency is several orders of magnitude lower than the typical digital data rates, the AC signal behaves as if the voltage level is approximately constant. The processing circuit undergoes three phases of operation: turn-on (once the power supply exceeds the threshold voltage), perform computation, and turn-off [18]. An accurate power-on-reset is required to guarantee correct operation. Furthermore, a dynamic memory cell is needed to retain states between on and off cycles. As a significant limitation, this approach can only be applicable to wireless power harvesting systems with very low frequency.

In 2004, an AC-only RFID tag was proposed for barcode replacement [19]. The logic adopted in the circuitry is a combination of quasi static energy recovery logic [20] and a group of transmission gates that switch on and off during each half cycle of the AC power supply signal. The RFID tag chip was fabricated in 0.13 μm CMOS process and consumes 0.002 mm^2, approximately three times smaller than a conventional RFID-tag. The proposed approach, however, increases the overall power consumption.

In 2007, a quasi-static adiabatic logic consisting of diodes [21] was used for a low frequency (LF) ID tag [22]. The circuit consists of a pair of cross-coupled nMOS transistors, a pair of complementary NP functional blocks, and two diodes in series with P logic. The proposed approach alleviates the issue of dynamic power in conventional adiabatic circuits, but suffers from relatively large energy dissipated by the diodes.

In 2016, an RFID tag with RF powered digital logic (without rectification) was proposed [23]. The proposed RF-Only logic is similar to the quasi-static energy recovery logic in terms of topology [20]. The top and bottom power supply transistors behave as a switch controlled by the AC signal rather than acting as diodes. The proposed logic is similar to static CMOS, but suffers from degraded robustness caused by the floating output node during part of the operation. Furthermore, only a small portion of the charge stored at the load capacitance is recycled. According to simulation results, the tag area was reduced by approximately 80%. The overall power consumption, however, increased by an order of magnitude.

Contrary to these existing studies that primarily focus on device footprint (and therefore cost), the primary emphasis of the proposed approach in this paper is on achieving an order of magnitude reduction in power consumption. Such significant reduction has the potential to expand the application domain of wirelessly powered devices such as RFIDs due to stronger data processing capability under the same power budget.

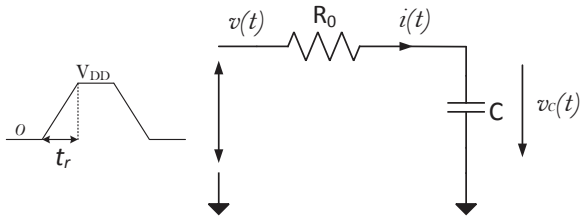

Fig. 2: Equivalent RC circuit to determine the energy loss in adiabatic logic.

III. Background

Wireless power harvesting can be considered as a niche application for charge-recycling adiabatic circuits since the harvested signal is in the form of AC signal [16]. These circuits permit gradual current flow through a transistor when the voltage difference is sufficiently small and recover a portion of the charge back to the supply voltage [24]. Historically, generation of the time varying trapezoidal signal from a DC supply voltage has been a primary barrier due to low efficiency in the range of 10% to 30% [25], [26]. This limitation does not exist in this case due to the sinusoidal harvested signal.

The principle of adiabatic switching operation is illustrated in Fig. 2. Consider the equivalent circuit for an adiabatic logic gate, where C is the load capacitance and R is the on-resistance of transistors along the charging path [27]. Contrary to the conventional charging that is achieved by a constant DC voltage, a time-varying voltage source is used as the power supply. If the transition time t_r is sufficiently long, capacitance voltage $v_C(t)$ approximately follows the input signal $v(t)$ [*i.e.*, $v_C(t) \approx v(t)$)]. Therefore, the charging current is

$$i(t) = C\frac{dv(t)}{dt} = \frac{CV_{DD}}{t_r}. \tag{1}$$

The energy dissipated during a charging event is calculated by integrating the instantaneous power $p(t)$ during the transition time t_r,

$$E = \int_0^{t_r} [v_R(t) + v_C(t)] \cdot i(t)dt = \frac{RC}{t_r}CV_{DD}^2. \tag{2}$$

A complete cycle consists of charging and recovery. Since the recovery process consumes the same amount of energy, the overall dissipation in one adiabatic logic during a cycle is expressed by

$$E_{AL} = 2\frac{RC}{t_r}CV_{DD}^2. \tag{3}$$

As indicated by (3), in adiabatic operation, energy is inversely proportional with the transition time. This characteristic is unlike static CMOS operation where energy to charge a capacitance does not depend upon the transition time. As such, it is important to note that the transition time should be larger than $4RC/\alpha$ for the adiabatic operation to outperform static CMOS, where α represents switching activity factor. Thus, the significant advantage of adiabatic logic in energy consumption is diminished as the frequency increases since $v_C(t)$ cannot follow the input signal $v(t)$. Unlike self-powered

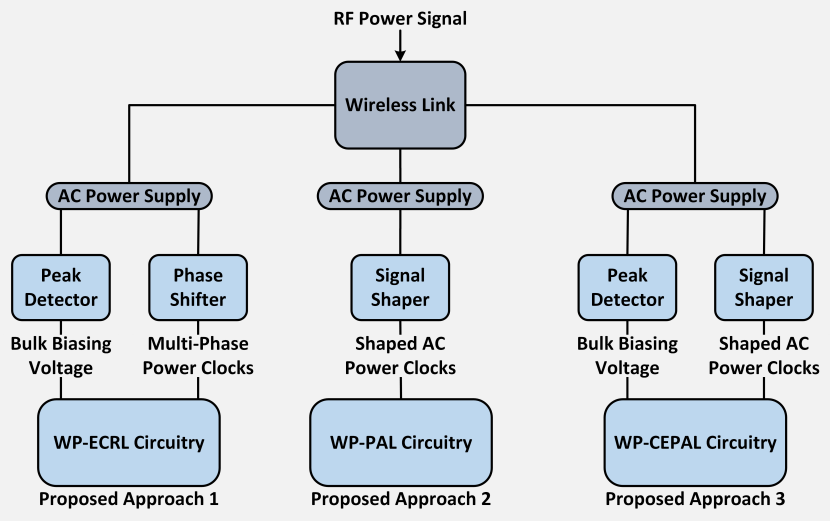

Fig. 3: Summary of the three proposed AC computing methodologies for wireless power harvesting and required auxiliary circuitry for each approach.

IoT applications, this behavior can be a disadvantage for conventional applications that demand high performance. It is also important to note that the parameter RC is highly technology dependent. In modern technologies, this parameter is in the range of picoseconds. Thus, reasonable power savings can be achieved by adiabatic operation at sufficiently high frequencies in nanoscale technologies.

A typical adiabatic circuit consists of two primary parts, a digital core consisting of charge-recycling gates and a circuitry for the generation of the AC power supply signal [28]. The AC signal behaves as both the power supply and clock signal and commonly referred to as the power-clock signal. Adiabatic circuits typically require multiple power-clock signals with certain phase difference. One cycle of a power-clock signal is divided into multiple intervals. As such, adiabatic circuits are typically inherently pipelined [29].

IV. Proposed Approach

In the proposed approach, the wirelessly harvested AC signal is used to power the digital logic that relies on charge-recycling/adiabatic circuits. The rectification and regulation steps of the conventional methods are eliminated. As depicted in Fig. 3, three approaches are proposed, each exhibiting different requirements and tradeoffs, as explored in this paper.

A wirelessly powered implantable computational logic is developed as the application to demonstrate the proposed methodology. In implantable applications, wireless powering and communication are essential since any wiring through the skin poses a significant health risk. RF energy is transmitted through inductive coupling due to high attenuation of the electrical field within the body [30]. Transmitted RF power is limited by the heating of the body tissue and these limits are determined by specific absorption rates for different tissues [31]. This limitation significantly constrains the amount of power that can be delivered to the implant. Thus, achieving high energy efficiency and small form factor are among the primary challenges in the design of implantable devices.

Implantable devices record biological signals, such as neural activity [32], [33], and/or stimulate different parts of the neural system [34]. In many applications, like in the case of deep-brain implants, the optimal stimulation timing and pattern are obtained by processing the recorded data, calling for the design of a closed-loop system. The existing designs of such systems [35], [36] have data processing implementation moved to a different location within the body where more energy is available due to the extended physical space for a battery. As demonstrated in this paper, the proposed AC computing methodology significantly reduces the energy cost of data processing and can therefore lead to implementation of a closed-loop system on a single substrate.

The clock frequency for the application is 13.56 MHz. An 8-bit arithmetic logic unit (ALU) is designed as the data processing unit using both the proposed methodology and the conventional method. Inductive coupling based wireless link and AC powered 8-bit ALU implemented with the proposed approach are described in the following subsections.

A. Wireless Link

The power supply signal for the operation of AC powered digital logic is obtained through RF energy harvesting. RF energy can be harvested in a near-field, by relying mostly on the inductive coupling at short distances from a transmitting coil [37], [38], and in far-field, by receiving radiated electromagnetic waves using antenna at much longer distances from an RF energy source [39]–[41]. In this case study, the focus is on near-field energy harvesting.

The wireless power harvesting system includes an external coil placed adjacent to the skin (for transmission of the RF signal) and an implanted receiving coil. An RF power amplifier drives the external coil and a dedicated RF electromagnetic wave is transmitted. A portion of this RF energy is captured by the implantable coil. The lump model of the link is illustrated in Fig. 4 [30], which presents a reasonable approximation up to 100 MHz of the transmitting frequency. L_1 and L_2 represent the inductances of the two separate coils and M

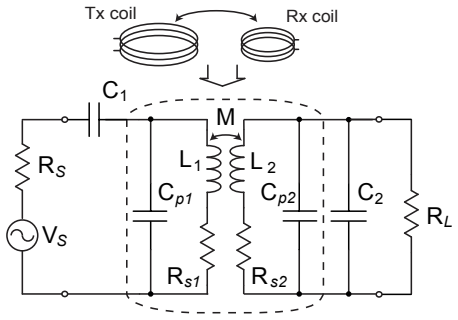

Fig. 4: Lumped model of an inductively coupled wireless power harvesting system.

is the mutual inductance. R_{s1} and R_{s2} represent parasitic resistive loss, while C_{p1} and C_{p2} are the parasitic capacitances in the coils. C_1 and C_2 are the tuning capacitance in order to achieve resonance in both the external and implantable circuits. R_S and R_L are the source and load resistances. The design of the coils in the wireless link is driven primarily by the application, that sets the physical constraints in the design of both coils and the distance between the coils. The form factor of the implant determines the size of the receiving coil. The power transmission frequency is determined based on two opposing trends: (1) the attenuation along the medium is lower at frequencies below 100 MHz as compared to gigahertz range, (2) for a fixed size of the implanted coil, a lower frequency leads to smaller electrical size, thereby lowering the received power. Thus, an optimal frequency exists, which depends on the application scenario. For example, if the external coil is sized on the order of a few centimeters, the optimal frequency is on the order of 40 MHz [42]. In the case of smaller external coil, the optimal frequency shifts to the order of 1 GHz [43].

To illustrate the design process of a wireless link, a deep brain implantable device is assumed. Transmitting coil is designed with a diameter of 5 cm and two designs of the receiving coil with diameters of 1.5 mm and 3 mm are explored. A full-wave electromagnetic field solver based on finite element method, HFSS (high frequency structural simulator), is utilized to analyze and extract the network characteristics of the wireless link. The power efficiency and the parameters for the equivalent narrow band model of the link (see Fig. 4) are determined from S parameters extracted from HFSS and Keysight Advanced design system (ADS) simulations. The simulation setup is depicted in Fig. 5 and the human head model is shown in Fig. 6. The physical and electrical characteristics of the coils are summarized in Table I. The transmitted power is set to 24 dBm. The power efficiency reaches -37.4 dB at a distance of 6.5 cm, assuming optimum matching networks are available for transformation of load impedance for maximum transfer efficiency. Note that in this analysis, the transmitting and receiving coils are assumed to be perfectly aligned. In a practical scenario, the power transfer efficiency of the link is reduced by lateral and/or angular misalignment [44]–[46].

The maximum available power for the implantable device as a function of the distance between the coils is shown in Fig. 7. This figure demonstrates that by lowering the power consumption of the implantable coil (as targeted in this research), a greater implantation depth is achieved.

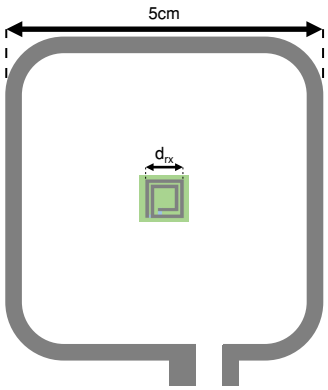

Fig. 5: Wireless link simulation setup: transmitting and receiving coils at D_{imp} distance.

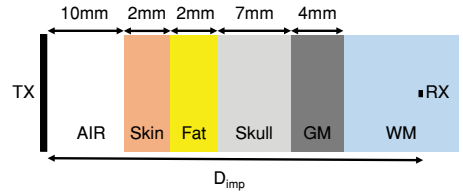

Fig. 6: Model of the human head for deep brain implantable devices. GM and WM refer, respectively, to gray matter and white matter.

B. AC Powered 8-Bit ALU

The RF energy harvested from the near-field wireless link described above is used to power an 8-bit ALU. The ALU consists of two types of computational blocks: boolean logic (INV, OR, XOR, and AND) and arithmetic logic (adder, subtracter, and multiplier), as shown in Fig. 8. To demonstrate the proposed methodology, the ALU is implemented with each of the three proposed approaches (see Fig. 3) as well as the conventional method where the wirelessly harvested AC signal is rectified, regulated, and used with conventional static CMOS. 45 nm technology with a nominal voltage of 1 V is used for each approach.

In the first proposed approach [see Fig. 9(a)] where wirelessly powered efficient charge recovery logic (WP-ECRL) [14], [28] is utilized, four power-clock signals are required, each exhibiting 90° phase difference. Furthermore, an appropriate voltage level is needed to properly bias the bulk terminals of the pMOS transistors. Thus, the proposed

TABLE I: Parameters of T_x and R_x coils.

Parameter	T_x	R_{x1}	R_{x2}
Diameter (mm)	50	1.5	3
Material	Cu	Cu	Cu
Number of turns	1	2	2
Trace width (mm)	3	0.2	0.3
Trace Thickness (μm)	38	38	38
Space between turns (mm)	N/A	0.1	0.1
Effective L @ 13.56 MHz (nH)	126.3	4.6	17.4
Resistance ($m\Omega$)	64.7	21.2	49.9
Resonance capacitor (nF)	1.09	29.9	7.9

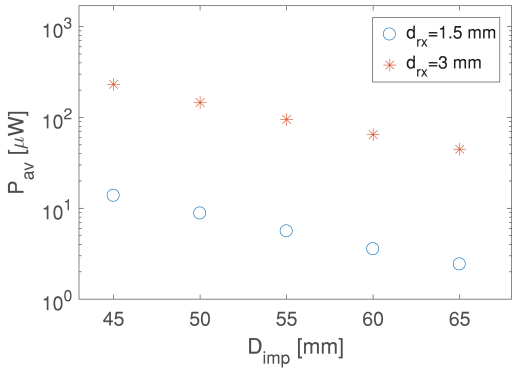

Fig. 7: Available power for the operation of the implant with two different sizes of the receiving coil as a function of distance between transmitting and receiving coils.

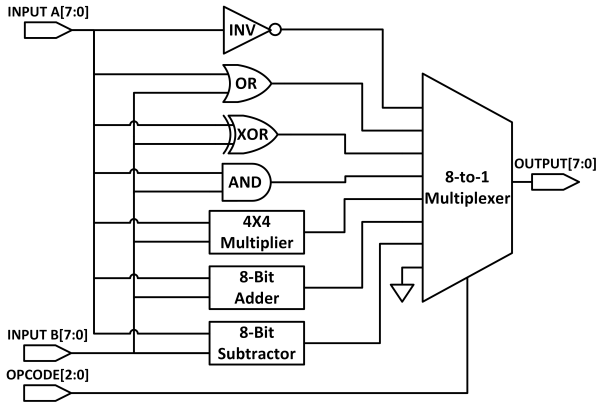

Fig. 8: Block-level diagram of the 8-bit arithmetic logic unit.

WP-ECRL approach requires two blocks for correct operation under wirelessly harvested AC signal. These blocks are a *peak detector* (for bulk biasing) and *phase shifter* (to generate multi-phase power-clock signals). Note that two phase shifters are required to generate 90° phase difference from two harvested AC signals that are out-of-phase, producing four power-clock signals in total, as depicted in Fig. 9(a).

In the second proposed approach [see Fig. 9(b)], where wirelessly powered pass transistor adiabatic logic (WP-PAL) [15], [47] is utilized, two out-of-phase power-clock signals are required. These power-clock signals are directly harvested through two receiving coils configured to produce 180° phase difference, as shown in Fig. 9(b). Thus, a phase shifter is not required by WP-PAL. However, since the PAL based gates cannot correctly operate with the harvested sine wave that has negative voltage components, a low complexity *signal shaper* is developed. Note that two signal shapers are required since there are two out-of-phase power-clock signals.

Finally, in the third proposed approach [see Fig. 9(c)], where wirelessly powered complementary pass transistor adiabatic logic (WP-CEPAL) [16], [25] is utilized, two out-of-phase power-clock signals are required, similar to WP-PAL. Unlike PAL, each gate of CEPAL requires both power-clock signals at the same time. As such, CEPAL is not inherently pipelined. WP-CEPAL requires a peak detector to properly bias the bulk nodes of the pMOS transistors (similar to WP-ECRL) and two signal shapers (similar to WP-PAL) to eliminate the negative

TABLE II: Characteristics of the 8-bit ALU for each of the proposed and conventional approaches.

	Transistor Number	Latency	Operation
WP-ECRL	4158	2.5 clock cycles	4-phase
WP-PAL	4158	5 clock cycles	2-phase
WP-CEPAL	9394	4 clock cycles	quasi-static
Static CMOS	6990	4 clock cycles	static

voltage components of the harvested $PCLK$ and $\overline{PCLK}$ signals, as depicted in Fig. 9(c).

These supporting circuitries (phase shifter, peak detector, and signal shaper) required for the proposed approaches are referred to as *auxiliary circuits*. Note that in conventional static CMOS based approach where the harvested AC signal is converted into a DC voltage, these circuits include a rectifier and regulator. The details of these auxiliary circuits are described in the following section.

It is important to note that WP-ECRL and WP-PAL are inherently pipelined with a logic depth of 10 clock phases. Since ECRL operates with 4-phase power-clock signal whereas PAL operates with 2-phase power-clock, the latency for ECRL and PAL are, respectively, $10/4 = 2.5$ and $10/2 = 5$ clock cycles. Alternatively, WP-CEPAL and static CMOS based approaches require sequential circuits (flip-flops) for synchronization, resulting in 4 pipelining stages. As such, the overall number of transistors in WP-CEPAL and static CMOS is higher than WP-ECRL and WP-PAL. WP-CEPAL requires the highest number of transistors since each gate in CEPAL requires four transistors in addition to the conventional pull-down and pull-up networks [see Fig. 9(c)]. WP-ECRL and WP-PAL require the least number of transistors since there are no flip-flops and the pull-up network in each gate only consists of two pMOS transistors [see Figs. 9(a) and (b)]. Also note that dual-rail encoding in adiabatic logic generates complementary output signals. As such, some arithmetic operations such as subtraction that requires the 2's complement can be built without introducing additional inverters. Some of these characteristics are summarized in Table II for each approach.

In WP-ECRL and WP-PAL that do not have any flip-flops due to inherent pipelining, additional buffers are used to synchronize data paths with different logic depths. Specifically, buffers are inserted to those data paths with shorter logic depths to ensure that the outputs are synchronized with the same power-clock signal. This requirement adds significant overhead to WP-ECRL and WP-PAL as compared to WP-CEPAL and static CMOS logic. To partially mitigate this issue, multiple gates can be merged into a single complex gate, thereby reducing the logic depth of a data path, as depicted in Fig. 10 for a 1-bit full adder. In this example, output S (sum) takes two phases of the AC power-clock signal whereas output C_{out} (carry) takes three phases. Thus, an additional buffer would be required at the output of S to synchronize these two signals. Instead, these two functions can be merged into a single ECRL (or PAL) complex gate, as shown in Fig. 10.

C. Auxiliary Circuits for Each Method

1) Peak Detector: Elimination of the rectification stage makes it difficult to bias the nWELL of the cross-coupled

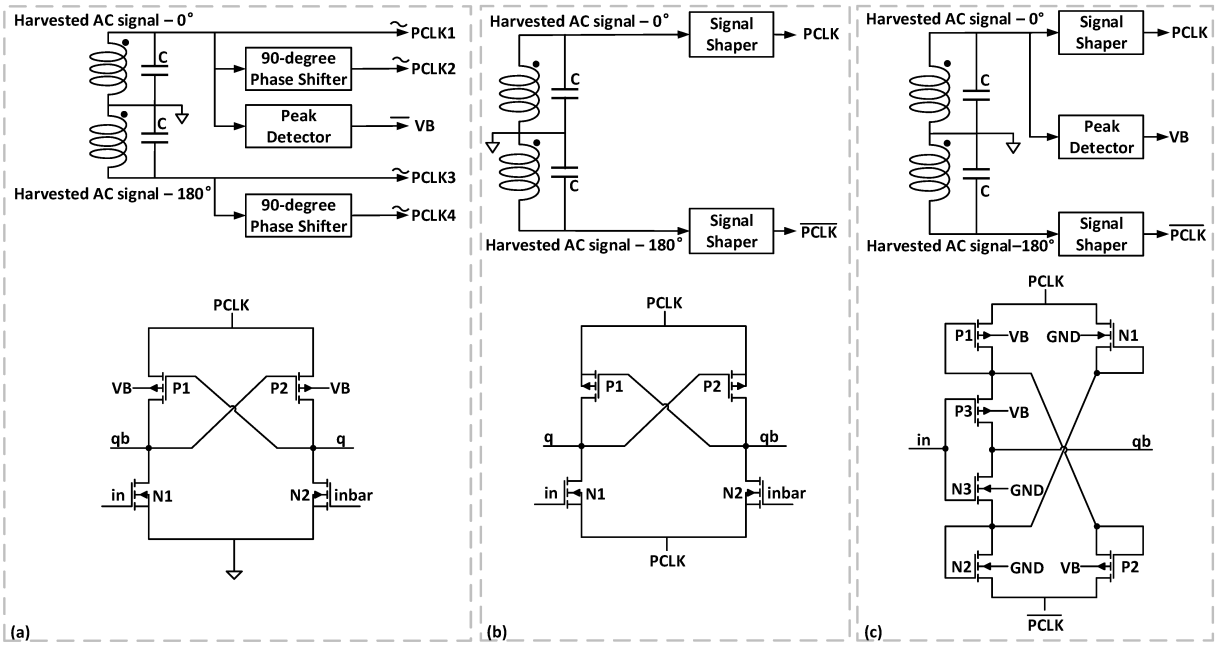

Fig. 9: Illustration of the required auxiliary circuitry as well as the schematic of an inverter gate for each of the proposed methods: (a) WP-ECRL, (b) WP-PAL, and (c) WP-CEPAL.

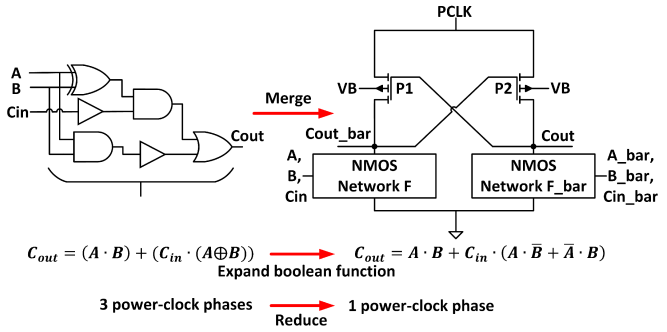

Fig. 10: Merging multiple gates into a single complex adiabatic gate to mitigate the overhead of additional buffers required for synchronization.

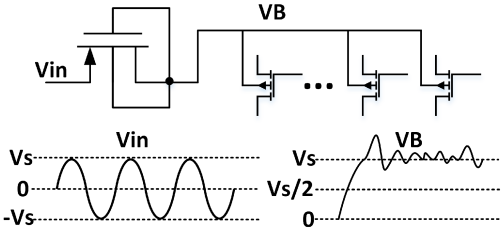

Fig. 11: Diode-connected MOS transistor used as peak detector to properly bias the bulk terminals of the pMOS transistors.

pMOS transistors in both WP-ECRL and WP-CEPAL. If these bulk nodes are connected to the AC power-clock signal (with negative voltage components), the bulk-to-drain junction diodes are turned on when the junction voltage exceeds the forward-on threshold, dissipating unnecessary power due to significant forward bias diode current. To prevent this issue, a peak detector is used, as depicted in Fig. 11.

Thus, an unregulated DC voltage (equal to the peak value of the input AC signal) is produced for the bulk nodes. Forward biased junction diodes are prevented. Output of the peak detector is shown in Fig. 12(a) where the input is the harvested AC signal. The relatively large ripple voltage at the output does not affect proper operation since this voltage does not drive any circuit. Note that unlike a conventional rectifier used for generation of DC supply voltage that transmits significant current to the output load, the current across the proposed peak detector is negligible. Thus, the energy loss is sufficiently low.

2) Phase Shifter: The two inductors within the receiving coupling circuit are configured such that the two harvested AC signals have 180° phase difference, thereby providing a pair of complementary power-clock signals (0° and 180°). These out-of-phase signals are sufficient for the operation of WP-PAL and WP-CEPAL. However, for WP-ECRL, a phase shifter is required to generate the remaining two power-clock signals (90° and 270°). The proposed phase shifter can be represented as a low pass network, as shown in Fig. 13. This choice of the phase shifter implementation is limited to the operating frequencies below 20 MHz, where use of transmission lines leads to long and lossy lines. The 90° phase shift is achieved with the resonance of L_o and C_o, while the gain is set by the ratio of resistance R_o and impedance of the inductor at resonance. Minimization of the power loss on R_o requires higher values of the inductor. The adiabatic logic, driven by the phase shifter, is modeled as a series of a resistor R_L and a capacitor C_L. These load characteristics are determined from power analysis [48],

$$R_L = \frac{P}{I_L^2}, \tag{4}$$

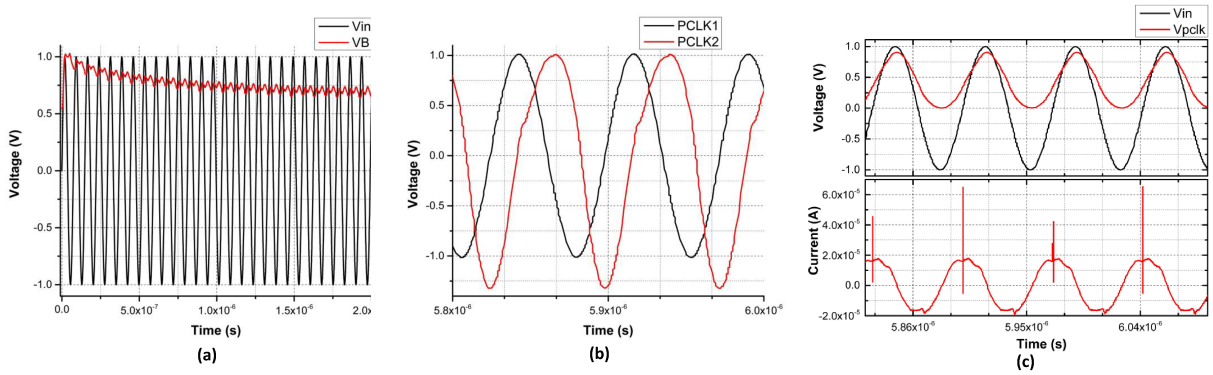

Fig. 12: Simulated output waveforms of the auxiliary circuits: (a) input and output signals of the peak detector, (b) power-clock signals with 90° phase difference, (c) input and output signals of the signal shaper along with the output current.

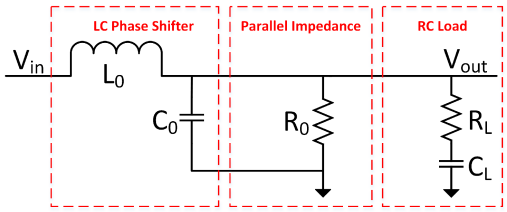

Fig. 13: An RLC model of LC phase shifter with load.

TABLE III: The variation of load characteristics R_L and R_C during different phases for WP-ECRL.

Power-Clock	R_L(kΩ)	$C_L(fF)$	$I_L(\mu A)$	$P_L(\mu W)$
Phase 1	4.15	168.15	10.13	0.43
Phase 2	5.87	155.20	9.35	0.51
Phase 3	1.84	206.16	12.42	0.28
Phase 4	4.74	127.38	7.67	0.28

$$C_L = \frac{\sqrt{2} I_L}{\pi V_{DD} f_c}, \tag{5}$$

where P is the simulated average power consumption for a specific phase, I_L is the RMS current drawn by the load during the same phase, and f_c is the frequency of the AC power-clock signal. Note that the load seen by the phase shifter output is relatively the same regardless of the switching direction since either of the two complementary branches conducts in each cycle of the power-clock signal. However, the load characteristics slightly vary for each phase of the power-clock signal, as listed in Table III. A smaller parallel resistance R_0 in Fig. 13 can be used to mitigate the effect of phase on R_L and C_L. A sufficiently small R_0, however, should be avoided to prevent significant power loss. The parameters of the two phase shifters required for WP-ECRL are listed in Table IV. The gain of the phase shifter for the selected values of the circuit elements is 0.7. The value of the inductor L_o in μH range leads to an increased form factor of the phase shifter implementation. This limitation could prohibit the use of WP-ECRL logic with the proposed phase shifter in certain applications. For typical values of the Q factor of the inductor on the order of 30 [49], [50], the effect of the Q factor on the gain and the phase mismatch is negligible. At higher frequencies, however, the value of the inductor is considerably

TABLE IV: Specifications of the phase shifter.

Parameter	L_0	C_0	R_0
LCPS1	810μH	55fF	100$k\Omega$
LCPS2	925μH	80fF	100$k\Omega$

reduced. For applications that are highly footprint-constrained, WP-PAL can be a better choice since phase shifter is not required. The output of the phase shifter is illustrated in Fig. 12(b), demonstrating 90° phase difference. The small amplitude mismatch at the negative peak voltage between the input and output of the phase shifter does not affect the operation since WP-ECRL inherently eliminates the negative voltage component of the power supply at the output.

3) Signal Shaper: In WP-PAL, the negative voltage components of the harvested AC signal should be eliminated to ensure proper operation. A signal shaper is developed for this objective, as shown in Fig. 14. It consists of a pMOS transistor with the bulk, gate, and one of the junctions shorted. The input voltage of the signal shaper is an RF harvested bipolar sinusoidal waveform centered around ground potential, while the output is a unipolar sinusoidal-like signal that does not fall below zero, as depicted in Fig. 12(c). The signal shaper has two distinct phases of operation. In the first phase, for a small fraction of the sine wave period, the transistor operates in the subthreshold region and the source-bulk diode is forward biased. In the second phase, the transistor and the parasitic diodes are turned off. Referring to Fig. 14, if the transistor capacitors C_{GS} and C_{SB} are comparable in size to the load capacitance seen by the power-clock signal, the capacitive coupling current flowing through the capacitors C_{GS} and C_{SB} is much larger than the leakage current and the output voltage is a scaled version of the input voltage. The ratio of capacitors C_{GS}, C_{SB} and load capacitance (which depend upon the size of the signal shaper and the number of driven transistors) determines the ratio of the input and output voltage in this region of operation. In the mean time, the size of the signal shaper also sets the overall DC level of the output voltage. The optimal size of the transistor leads to a sine wave-like signal at the output that is always greater than zero volt.

To better understand the operation and the high power efficiency of the proposed signal shaper, the time domain waveforms of the currents of all four transistor terminals are

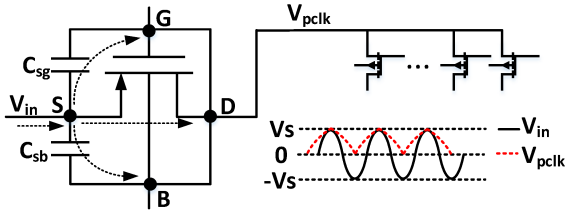

Fig. 14: Schematic of a diode-connected MOS signal shaper to eliminate the negative voltage components of the harvested AC signal.Parasitic capacitances are also illustrated.

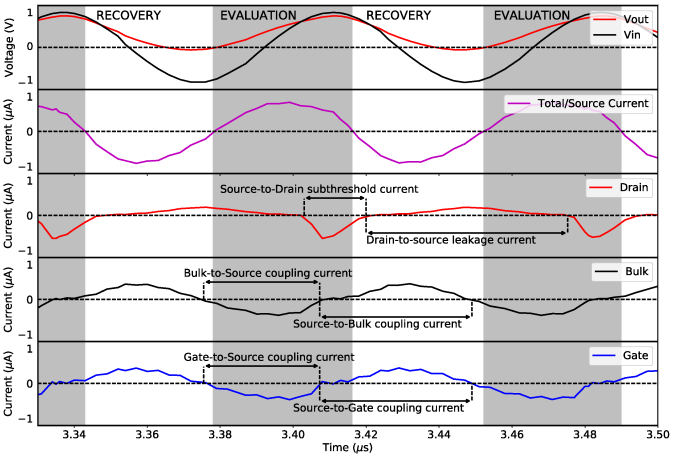

Fig. 15: Waveforms of the signal shaper to better understand the high efficiency operation. From top to bottom: input and output voltages, overall current (at source node), drain current, bulk current, and gate current.

illustrated in Fig. 15, along with the depiction of the evaluation and recovery phases. The duty cycle and the DC level of the signal shaper output voltage are determined by the ratio of the subthreshold current component and the leakage current component of the overall drain current during two phases of the transistor operation. The gate and bulk current components correspond to the capacitive coupling current through the transistor capacitors and dominate the overall current. Thus, the power efficiency of the signal shaper is maximized. Furthermore, since the coupling current is the primary conduction mechanism, bi-directional current flow across the signal shaper is enabled. This characteristic is critical to successfully recycle charge during the recovery phase (note the negative current during this phase).

Another approach to overcome the issue of harvested AC signal with a negative voltage component would be to produce a negative DC voltage through a peak detector (similar to the one proposed for WP-ECRL) and connect the bulk terminals of the nMOS devices to this negative voltage to ensure proper operation. In this way, harvested AC signal with negative voltage could be directly used without a signal shaper. According to simulation results, however, this approach significantly increases the leakage current from channel to drain due to band-to-band tunneling (BTBT) [51]. BTBT is exacerbated in this case due to gate-induced drain leakage (GIDL) since the gate-to-source node has negative voltage [52].

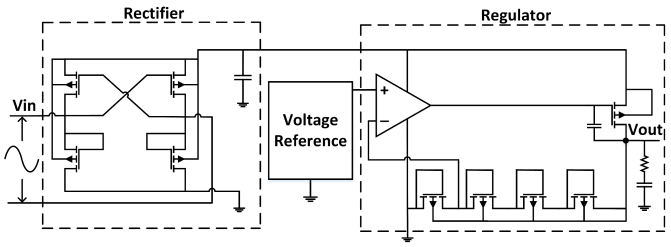

Fig. 16: Circuit diagram of a low complexity RF-DC converter and regulator required for traditional approaches.

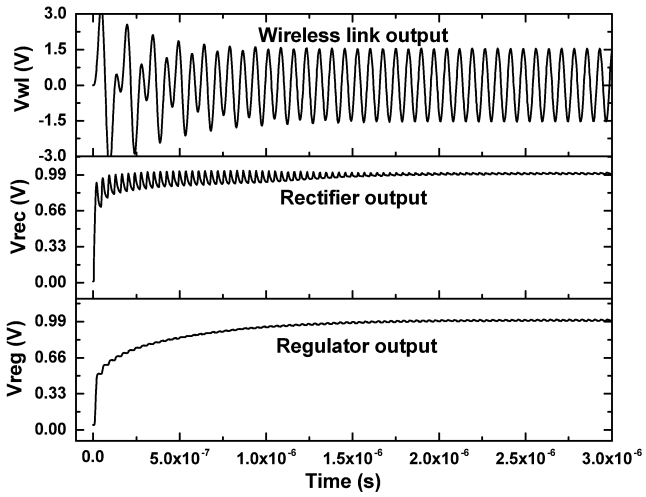

Fig. 17: Simulated output waveforms of the wireless link, rectifier, and regulator for the conventional topology.

4) RF-DC Converter/Regulator: RF-DC converter/regulator is considered as an auxiliary circuitry for the conventional approach, as illustrated in Fig. 16. Typical maximum power conversion efficiencies at low input power levels are in the range of 30 to 40% due to voltage drop across the diodes [11], [53]–[55]. To ensure a fair comparison between conventional and proposed approaches, the RF-DC converter/regulator is designed to achieve a power efficiency of 32.9% (39.7% for rectification stage and 95.2% for regulation stage). The harvested wireless signal as well as rectified and regulated signals are illustrated in Fig. 17. The regulated 1 V is used to power 8-bit ALU designed with conventional static CMOS method with the same clock frequency of 13.56 MHz.

V. Simulation Results

The output waveform of one of the bits is provided for each approach in Fig. 18. Note that the WP-CEPAL output is similar to the output signal obtained from conventional static CMOS approach. There is, however, reduction in rail-to-rail voltage due to the diode-connected transistors.

The average power consumed by the proposed approaches is compared with the conventional approach in Table V. The P_R in the table refers to the received power at the implanted coil when the transmitted power through the wireless link is such that the amplitude of the harvested power-clock signal

Fig. 18: Example output waveforms of the ALU for each of the proposed method as well as the conventional approach.

TABLE V: Comparison of received power at the wireless link (summation of overhead and logic power consumption) for each of the proposed methods and conventional approach.

	$P_R/\mu W$	$P_{overhead}/\mu W$	$P_{logic}/\mu W$
WP-ECRL	17.49	14.28	3.10
WP-PAL	2.94	2.542	0.40
WP-CEPAL	5.70	2.15	3.55
WP-Static CMOS	47.64	31.99	15.65

for adiabatic logic (or DC supply for static CMOS) is 1 V. $P_{Overhead}$ and P_{Logic} refer, respectively, to the power consumed by the auxiliary circuits in each approach and the logic power consumption (8-bit ALU described in Section IV-B). As such, the power conversion/conditioning efficiency for each implementation is determined by the ratio of P_{logic} and P_R and can be obtained from Table V.

As listed in this table, up to 16.2× reduction in overall power consumption is achieved by the proposed methodology (WP-PAL) as compared to conventional static CMOS that has a rectifier and regulator. The overhead power is the highest for the conventional case (approximately twice the logic power) due to relatively inefficient AC-to-DC conversion process where the input power levels are in the microwatt range. The overhead power in WP-ECRL is also relatively high compared to WP-PAL and WP-CEPAL due to the power consumed by two phase shifters. Alternatively, the signal shaper and peak detector are highly efficient, minimizing the overhead power for WP-PAL and WP-CEPAL. The logic power consumption in WP-PAL is only 0.4 μW (approximately 40× less than static CMOS) due to the ability to fully recycle charge.

To investigate the dependence of both overhead and processing power on circuit size, the power consumed by 4-, 8-, and 16-bit adder is plotted for each approach in Fig. 19 (overhead power) and Fig. 20 (processing power). The overhead power in static CMOS based approach increases with circuit size since the rectification and regulation stages consume more power when the load circuit is larger. Alternatively, in the proposed approaches, overhead power consumption is relatively independent of the circuit size. For processing power, WP-PAL exhibits the slowest increase with respect to circuit size since charge is fully recycled. Alternatively, the traditional approach exhibits the fastest increase.

TABLE VI: Effect of voltage scaling on power consumption and performance under nominal operating conditions.

V_A (V)	P_{ECRL} (μW)	P_{PAL} (μW)	P_{CEPAL} (μW)	P_{Static} (μW)
1.2	2.46	1.17	7.85	35.32
1.1	1.83	0.77	6.31	23.16
1.0	1.51	0.59	4.92	16.55
0.9	1.27	0.46	Fail	12.18
0.8	1.07	0.40	Fail	8.86
0.5	0.63	Fail	Fail	3.09

TABLE VII: Effect of voltage scaling on power consumption and performance under slow process corners and nominal temperature of 27°C.

V_A (V)	P_{ECRL} (μW)	P_{PAL} (μW)	P_{CEPAL} (μW)	P_{Static} (μW)
1.2	2.19	0.87	6.91	27.28
1.1	1.66	0.64	5.48	19.05
1.0	1.42	0.52	Fail	14.2
0.9	1.23	0.45	Fail	10.74
0.8	1.07	0.41	Fail	8.01
0.5	0.67	Fail	Fail	2.93

Finally, the behavior of the proposed method is investigated at lower operating voltages. This investigation is important for unreliable (such as ambient) wireless power sources where the harvested voltage can vary. The overall power consumption at various voltages is listed in Table VI for each approach under nominal operating conditions. According to this table, WP-ECRL and conventional approach can operate at the lowest supply voltage of 0.5 V where WP-PAL and WP-CEPAL fail. The minimum operating voltage for WP-PAL and WP-CEPAL is higher due to the reduction in the voltage headroom, as illustrated by the waveforms in Fig. 18.

The effect of scaled voltages is investigated at slow process corner to consider process variations, as listed in Table VII. WP-ECRL continues to operate correctly and WP-PAL fails at 0.5 V whereas WP-CEPAL fails at 1 V (contrary to nominal operating points where the failure occurs at 0.9 V). Finally, in Table VIII, the slow process corners are combined with a high operating temperature of 127°C. In this case, WP-PAL fails at all operating voltages, primarily due to degraded logic-low values. These simulations demonstrate the robustness of WP-ECRL approach as compared to WP-PAL and WP-CEPAL.

TABLE VIII: Effect of voltage scaling on power consumption and performance under slow process corners and high temperature of 127°C.

V_A (V)	P_{ECRL} (μW)	P_{PAL} (μW)	P_{CEPAL} (μW)	P_{Static} (μW)
1.2	3.03	Fail	9.87	36.82
1.1	2.43	Fail	8.02	25.99
1.0	2.03	Fail	Fail	19.4
0.9	1.72	Fail	Fail	14.64
0.8	1.46	Fail	Fail	11.01
0.5	0.86	Fail	Fail	4.07

TABLE IX: Qualitative comparison of the proposed methods and conventional approach, listing advantages and limitations. Nominal operation conditions are assumed.

	WP-ECRL	WP-PAL	WP-CEPAL	Conventional
Power supply	4-phase AC power-clocks	2-phase AC power-clocks	2-phase AC power-clocks	DC power
Complementary input	Yes	Yes	No	No
Output swing	Full swing	$V_{OH} = V_{DD}, V_{OL} = 1/4\|V_{tp}\|$	Half swing	Full swing
Output floating	One side floating during recovery	One side floating	Partial floating	No
Phase shifter	Required	Not required	Not required	Not required
Signal shaper	Not required	Required	Required	Not required
Peak detector	Required	Not required	Required	Not required
Rectifier and regulator	Not required	Not required	Not required	Required
Lowest supply voltage	<0.5V	0.8V	0.95V	0.5V
Pipelining	Inherently pipelined	Inherently pipelined	Flip-flops are required	Flip-flops are required

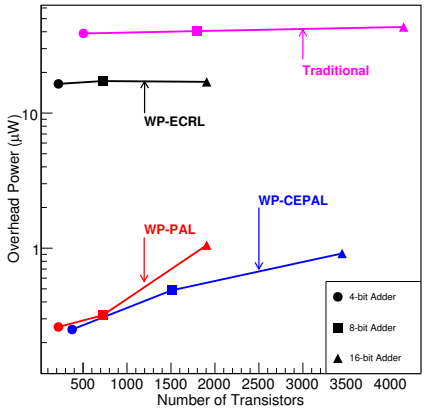

Fig. 19: Overhead power versus number of transistors to investigate the dependence of overhead power on circuit size for each of the methods.

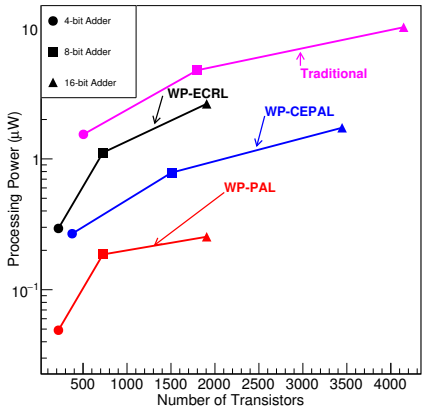

Fig. 20: Processing power versus number of transistors to investigate the dependence of processing power on circuit size for each of the methods.

VI. Discussion

Leveraging charge-recycling operation for wirelessly powered devices can achieve significant reduction in digital/processing power, as demonstrated in the previous section. The tradeoffs related with the three proposed implementations are discussed in this section, as summarized in Table IX.

WP-ECRL approach can operate at lower voltages compared to WP-PAL and WP-CEPAL. The operation is also relatively more robust due to full swing output signals. WP-ECRL, however, requires two phase shifters due to 4-phase AC power supply. The phase shifter consumes more power than the auxiliary circuitry required for WP-PAL and WP-CEPAL. However, if the data processing block is sufficiently large, this overhead power can be a small portion of the overall power consumption. Also note that the phase shifter potentially consists of off-chip passive devices, depending upon the required inductor and capacitor. At relatively low frequencies, the size of the required inductor can be prohibitive for certain applications where form factor is an important design objective. Alternatively, relatively reliable and robust operation at low voltages makes WP-ECRL an appropriate candidate for applications that rely on ambient wireless energy.

WP-PAL exhibits the least overall power consumption with a slight degradation at the output voltage swing. Furthermore, this approach relies on 2-phase AC power supply where the phase shifter is not required. Due to 2-phase operation, however, adjacent logic gates recover and evaluate at the same time, making synchronization more sensitive to phase deviations between the AC power supplies. As an important limitation, WP-PAL cannot reliably operate at voltages less than 0.8 V. Thus, this approach is relatively more appropriate for applications with dedicated wireless power source such as RFIDs and inductively coupled implantable devices.

WP-CEPAL is similar to static CMOS in terms of design and operation and therefore is an appropriate approach for larger-scale IoT devices where cell-based design and automation is critical. This approach, however, suffers the most from reduced voltage swing due to diode-connected transistors and is not inherently pipelined, unlike WP-ECRL and WP-PAL. Thus, this method consumes the highest number of transistors due to requirement for sequential cells, complete pull-up networks, and diode-connected transistors.

Finally, it is important to note that most of the IoT devices and wireless sensor nodes also consist of analog/RF blocks for sensing, digitization, and communication. Since these blocks require a DC voltage for reliable operation, the overall harvested energy may need to be split to obtain a DC voltage, only for the analog/RF blocks. More efficient AC computing can be used for local processing. The efficient on-site processing can be helpful in extracting meaningful information, thereby reducing the amount of data (and power) that should be transmitted.

VII. Conclusion

A novel AC computing methodology has been proposed for wirelessly powered IoT devices that typically suffer from the low computational resources. The proposed method leverages the existing charge-recycling and adiabatic principles while introducing several circuit structures to ensure efficient operation with wireless power harvesting. An inductive coupling based, near-field wireless link and an 8-bit arithmetic logic unit have been developed for evaluation. The energy efficiency of the auxiliary circuitry introduced for each method is characterized by quantifying the overhead power. Simulation results demonstrate significant reduction (up to 16.2x) in overall power consumption as compared to the conventional method that relies on AC-to-DC conversion and static CMOS based computation. Furthermore, compared to the conventional adiabatic systems, the inefficient multi-phase power-clock generation from a DC supply voltage is eliminated. Finally, some important design considerations and related tradeoffs are discussed.

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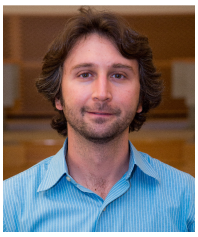

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