Signal Shaping at Interface of Wireless Power Harvesting and AC Computational Logic

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***Abstract*—The wirelessly powered adiabatic logic has introduced significant power savings in the design of the computational logic. We explore energy-efficient interfacing of one of the most efficient adiabatic logic families, pass-transistor adiabatic logic (PAL), with RF harvested signal. The interface circuit, signal shaper, transforms the bipolar sinusoidal input voltage to non-negative unipolar sinusoidal output that serves as the power clock signal for PAL. A theoretical analysis of the operation of the signal shaper is presented and verified using simulations in 65 nm CMOS technology. The designed shaper, when interfaced with 8-bit multiplier implemented using PAL, demonstrates the settling time of a few clock periods and high power conversion efficiency as high as 90%.**

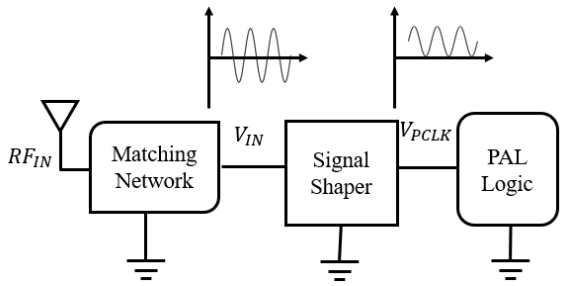

Fig. 1. Block diagram of the PAL-based wireless computing system.

I. Introduction

With a growing number of cyber-enabled devices engaged in a wide range of Internet of Things (IoT) applications, one of the most important obstacles for massive deployment presents the limited power budget [1]. This becomes more pronounced in the applications with an increasing need for more complex signal processing and/or security algorithms.

As the use of batteries becomes prohibitive in many applications, different forms of energy harvesting, like photovoltaic, piezoelectric, thermoelectric, have been commonly used in order to enable operation of the IoT devices [2], [3]. EM energy harvesting, either in far or near field, has also been employed. While inductive coupling has been limited mostly to the implantable devices [4], RF energy harvesting found application in a wide range of different sensory platforms like computational Radio Frequency Identification (RFID) tags [5], [6]. RF wireless power harvesting can typically provide more stable energy compared to other harvesting modalities, considering the presence of dedicated energy sources (RF exciter or RFID reader) or the abundance of ambient communication and broadcast signals (such as TV/radio broadcast, mobile and Wi-Fi transmitters) [7], [8].

The adiabatic switching mechanism that provides energy recovery has been proposed and explored due to a significant reduction in power consumption [9]. The adiabatic logic circuits operate with AC voltage supply. However, the generation of an AC power signal from a DC supply in the initial implementations suffered from limited efficiency, large LC tank and considerable complexity of the circuit [10]–[12]. With RF energy harvesting the AC power signal becomes obtained directly at the terminals of a coil or an antenna [13], [14]. Moreover, as the AC power supply acts as power clock for the digital system, there is no need for additional clock generation circuitry. However, RF harvested AC signal cannot be directly connected to the adiabatic logic. We investigate the adiabatic logic, pass-transistor adiabatic logic (PAL), that demonstrates the lower power consumption compared to other adiabatic logic families [15], [16] and signal shaper that is inserted after the antenna circuit to enable wirelessly powered PAL logic, as illustrated in Fig. 1.

The paper is organized as follows. Section II briefly reviews the wirelessly powered PAL logic. Section III describes the design and theoretical analysis of the proposed signal shaper with the simulation results presented in Section IV. Conclusions are outlined in Section V.

II. Wirelessly Powered PAL logic

Pass-transistor adiabatic logic (PAL) is one of the most efficient adiabatic switching mechanisms. Compared with the conventional efficient charge recovery logic (ECRL) where the NMOS transistors are directly connected to the ground, the PAL connects the NMOS transistors to the power clock. It allows a cut-off of the path to the ground and thus achieves higher power savings [17]. A PAL inverter circuit, shown in Fig. 2, is taken as an example to summarize the operation of general PAL gate. At the start, input IN is at logic high. It forms a current path from output power clock $PCLK$ to $\overline{OUT}$ and thus the $\overline{OUT}$ follows the $PCLK$. Meanwhile, output OUT is floating and close to zero due to the load capacitance of the following stages. As the $PCLK$ ramps up, the $\overline{OUT}$ achieves the peak of the power clock.

The inverter, as well as the more complex digital logic, can be modeled as a series of a resistor R_L and a capacitor C_L.

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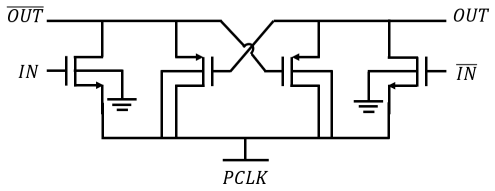

Fig. 2. A classic PAL inverter circuit.

The load values are determined from power analysis [18],

$$R_L = \frac{P}{I_L^2} \quad (1)$$

$$C_L = \frac{\sqrt{2}I_L}{\pi V_{DD} f_c} \quad (2)$$

where P is the simulated average power consumption for a specific phase, I_L is the RMS current drawn by the load during the same phase, and f_c is the frequency of the AC power clock signal. Note that PAL is a two-phase logic where the AC supply of each consecutive gate is 180^o out-of-phase. Thus, when one of the gates is at the evaluation phase, the preceding gate is at the hold phase, maintaining the input signals stable for the evaluating gate.

AC power clock signal is required for the operation of PAL logic. If RF harvested AC signal is used as the power clock signal, the power clock would be negative for one half of the period. When the power clock signal is negative, the gate-to-source voltage becomes negative leading to increased leakage current due to gate-induced drain leakage (GIDL) and it is even further enhanced by the band-to-band tunneling (BTBT) [19]. A signal shaper that transforms the bipolar sinusoidal voltage to non-negative sinusoidal voltage, has been proposed to interface the PAL logic and the RF harvested energy circuit [15]. The shaper consists of a PMOS transistor in a configuration similar to the classical rectifier, with the input, a matched antenna output, connected to one of the source/drain terminals and the output, power clock of PAL logic, connected to the gate, bulk and the other source/drain terminal. As the capacitance of the transistor has to be comparable to the equivalent capacitance of PAL logic, the size of the transistor becomes large leading to the low efficiency of the shaper.

III. Signal Shaper

This section illustrates the operation of the proposed signal shaper along with the implementation details. The proposed signal shaper, shown in Fig. 3, comprises the PMOS transistor in the same configuration as in the previously reported shaper [15], along with an external capacitance connected between the input and the output of the shaper.

The shaper has two distinct regions of operation, one when the voltage across the transistor is positive, that is $V_{in} > V_{out}$, and one when the voltage across the transistor is negative, that is $V_{in} < V_{out}$. In a steady state the time period $[t_1, t_2]$ in which transistor operates with positive voltage across transistor has a

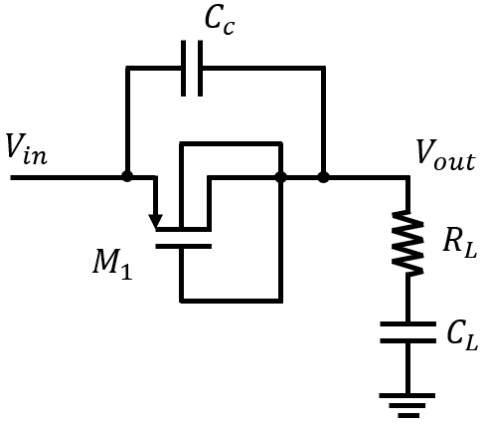

Fig. 3. Schematic of the proposed signal shaper.

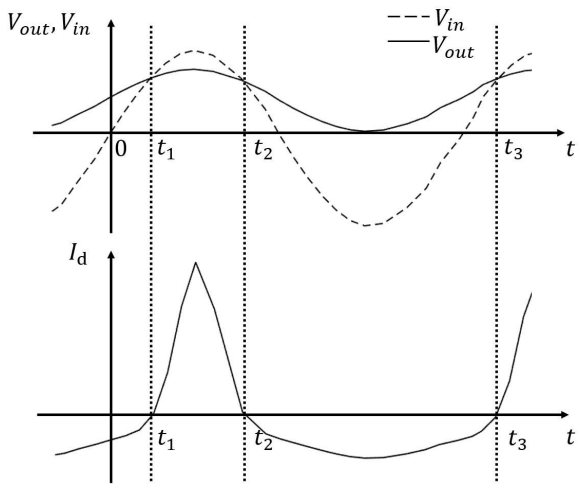

Fig. 4. Waveforms of the input voltage, output voltage, and transistor current in steady-state.

very low duty cycle. Duty cycle is low due to large difference between the current of the transistor in the two regions of operation, as illustrated in Figure 4.

$$I_{in} = I_{so}\frac{W}{L}(e^{\frac{V_{in}-V_{out}}{V_T}} - 1). \quad (3)$$

When the input voltage amplitude is lower than approximately 1.2 V, the difference between V_{in} and V_{out} in this region is small and the transistor operates in subthreshold region of operation. The subthreshold current of PMOS is:

$$I_{ds} = I_{so}\frac{W}{L}e^{-\frac{V_{gb}}{nV_T}}(e^{\frac{V_{sb}}{V_T}} - e^{\frac{V_{db}}{V_T}}), \quad (4)$$

$$I_{so} = \mu_p\sqrt{\frac{q\epsilon_{Si}N_{ch}}{2\varphi_s}}V_T^2 e^{\frac{-V_{tn}-V_{off}}{nV_T}}, \quad (5)$$

where n is the subthreshold slope coefficient, W and L are the width and length of the transistor, V_T is the thermal voltage, V_{off} is the subthreshold offset voltage, N_{ch} is the doping concentration in the channel and φ_s is the surface potential.

By inserting the values for the terminal voltages in this case the current of the transistor becomes

In the second region of the operation, when the voltage across the transistor is negative, the reverse current is relatively small and has the same expression as the transistor current in the first region (3). If we assume the transistor is turned off in this time period $[t_2, t_3]$, the signal shaper works merely as a capacitive voltage divider. The ratio of the amplitude of V_{out} and V_{in} is expressed as:

$$\frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{\frac{1}{j\omega C_L} + R_L}{\frac{1}{j\omega C_c} + \frac{1}{j\omega C_L} + R_L}, \tag{6}$$

and the average of V_{OUT}, $\overline{V_{OUT}}$, is zero. As the output voltage by design has to be kept higher than zero, the two capacitors have similar values. Without the external capacitor C_c, as in the previously proposed design [15], the total parasitic capacitance of the transistor C_{gs}, C_{ds} and C_{bs} has then to be large to match the capacitor C_L. This leads to large area of the transistors and low power efficiency of the shaper [15].

For sinusoidal input V_{in}, due to a low duty cycle of transistor's directly conductive region, we approximate the output voltage V_{out} as sinusoidal time waveform as well:

$$V_{in}(t) = V_{in}^{amp} \sin \omega t, \tag{7}$$

$$V_{out}(t) = V_{out}^{mid} + V_{out}^{amp} \sin \omega t, \tag{8}$$

where V_{in}^{amp}, V_{out}^{amp}, and V_{out}^{mid} are the input voltage amplitude, output voltage amplitude and the average level of output voltage, respectively. Additionally, the ratio of the amplitudes of the input and output voltage can be approximated as the ratio of the amplitudes in the region when the voltage across transistor is negative as in (6)

$$V_{out}^{amp} = V_{in}^{amp} \frac{C_c + C_{gs}}{C_c + C_{gs} + C_L} \times \sqrt{\frac{1 + \omega^2 C_L^2 R_L^2}{1 + \omega^2 \left(\frac{(C_c + C_{gs})C_L}{(C_c + C_{gs}) + C_L}\right)^2 R_L^2}}, \tag{9}$$

where C_c is the compensation capacitor and C_{gs} is the source-gate parasitic capacitance of the transistor. Note that other parasitic capacitances of the transistor are neglected since they are considerably smaller compared to the gate-source capacitance.

In the steady-state, the total charge that flows through the transistor in one period of the input signal is zero [20]. Thus, we have:

$$\begin{aligned} Q &= \int_0^T I_{in}(t)dt \\ &= \int_0^T I_{so} \frac{W}{L} (e^{\frac{V_{in}(t) - V_{out}(t)}{V_T}} - 1) = 0 \end{aligned} \tag{10}$$

where T is the period of the input voltage.

By inserting (7), (8) and (9) into (10), the average level of the output voltage, V_{out}^{min}, can be obtained as:

$$V_{out}^{min} = V_T \ln \left[I_0 \left(\frac{V_{in}^{amp} - V_{out}^{amp}}{V_T} \right) \right] \tag{11}$$

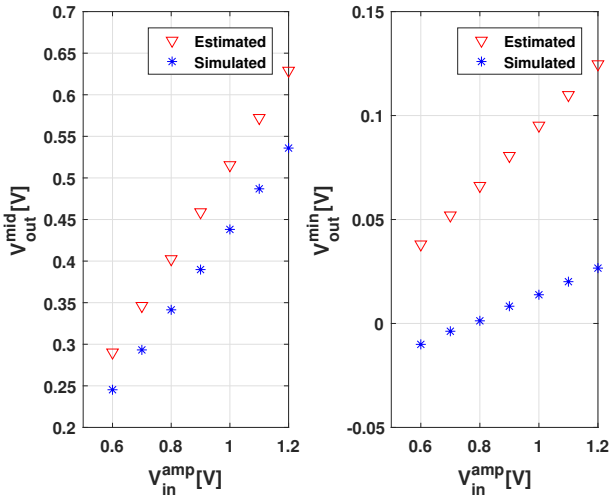

Fig. 5. Estimated and simulated (a) mid-level and (b) minimum output voltage with different input amplitudes.

where I_0 is the zero-th order modified Bessel function of the first kind. For $(V_{in}^{mid} - V_{out}^{mid}) \gg V_T$, the average level of output voltage can be approximately expressed as:

$$V_{out}^{mid} = V_{in}^{amp} - V_{out}^{amp} - \frac{1}{2} V_T \ln \left[\frac{2\pi (V_{in}^{amp} - V_{out}^{amp})}{V_T} \right] \tag{12}$$

Note that due to the Miller capacitance effect, the effective compensation capacitor is slightly bigger:

$$C_c' = C_c(1 + A_v), \tag{13}$$

where A_v is the amplification factor of transistor M_1. The final expression is:

$$V_{out}^{mid} = K V_{in}^{mid} - \frac{1}{2} V_T \ln \left(\frac{2\pi K V_{in}^{mid}}{V_T} \right), \tag{14}$$

where

$$K = \frac{C_L}{C_c(1 + A_v) + C_{gs} + C_L} \times \sqrt{\frac{1 + \omega^2 C_L^2 R_L^2}{1 + \omega^2 \left\{ \frac{[C_c(1 + A_v) + C_{gs}]C_L}{[C_c(1 + A_v) + C_{gs}] + C_L} \right\}^2 R_L^2}}. \tag{15}$$

As the amplification, A_v, is small, the size of transistor M_1 does not have a significant influence on the average level of the output voltage, V_{out}^{mid}. From (13) and (14), the compensation capacitor C_c has a dominant influence on V_{out}^{mid}. However, the sizing of transistor M_1 affects the settling time and the optimal sizing is obtained as a trade-off between the power efficiency of the shaper and settling time.

IV. Simulation Results

The proposed signal shaper along with the PAL logic is designed in 65 nm CMOS process. In the performed simulations, the input AC signal that mimics the harvested RF signal is set as a bipolar sinusoidal voltage at 13.56 MHz with

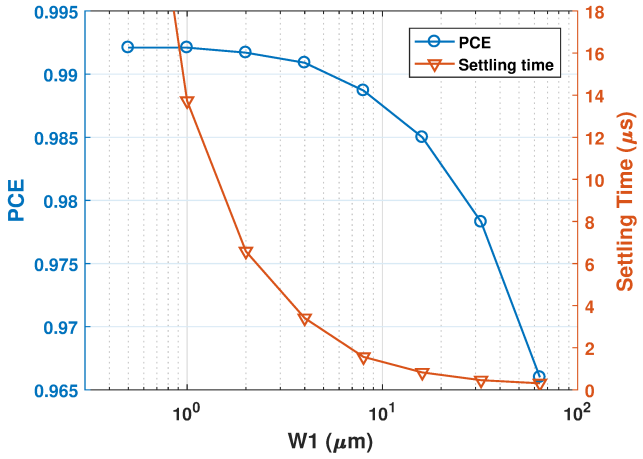

Fig. 6. PCE and settling time of the signal shaper for different widths of M_1.

1.2 V input amplitude. The frequency is selected as standard frequency for silicon-based item-level RF identification [21] and the commonly used carrier frequency in the inductive link for implantable devices [4], [22].

In the first set of simulations, to verify the presented analysis in Section III and illustrate the trade-off between the power conversion efficiency (PCE) and the settling time, as PAL logic, an 8-bit arithmetic logic unit (ALU) is implemented and used as the load of the signal shaper. The equivalent R_L and C_L of the ALU are 6.64 kΩ and a 437.5 fF, respectively. The parameters for (4) and (5) are obtained by the curve fitting based on simulated transistor characteristic $I_{ds} - V_{gs}$. Fig. 5 compares the values of mid-level output voltage and the minimum output voltage at steady state obtained from estimation model presented in Section III and simulations, with input amplitudes ranging from 0.5 V to 1.2 V. As shown in the figure, the obtained estimated values from the proposed model are close to the values obtained through simulations. As the amplitude of the input voltage increases, the discrepancy between the voltage levels obtained by the model and simulations increases, as the transistor in a certain time period moves from the subthreshold region of operation into moderate and strong inversion when the voltage across the transistor is positive.

Figure 6 shows PCE and the settling time of the signal shaper as a function of the width of the PMOS transistor, M_1. To reduce the settling time the transistor has to be sufficiently large. Therefore, to drive the ALU the signal shaper uses a 40 μm/60 nm PMOS transistor and a 295 fF capacitance C_c to achieve a reasonable settling time (i.e., less than 10 frequency periods) with PCE of 97.5%.

The signal shaper has been designed to interface 8-bit multiplier implemented using PAL logic. The layout of the shaper and the PAL logic is shown in Figure 7. The simulations have been performed on the extracted layout. The two signal shapers that provide two-phase power-clock signal occupy an

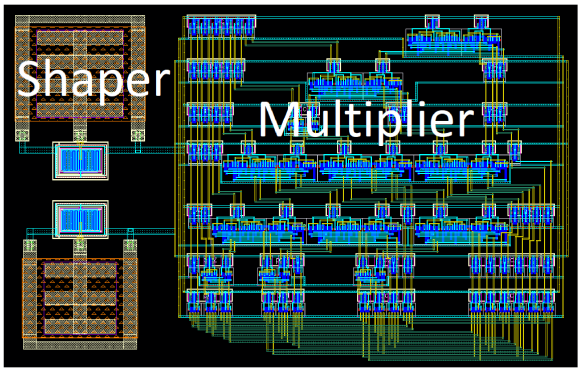

Fig. 7. Layout of the signal shaper and 8-bit multiplier implemented in PAL logic.

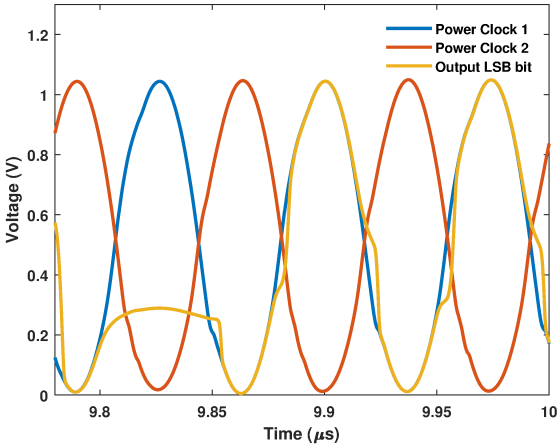

Fig. 8. Time waveform of the two power-clock signals and the LSB output bit of the 8-bit multiplier.

area of 14.5 μm x 37 μm and 8-bit multiplier occupies an area of 44 μm x 39 μm. The time waveform of the power clock signals and output LSB bit are shown in Figure 8. For the first power-clock signal shaper, the input power is 637.2 nW, output power is 575.8 nW and PCE of 90.36%. For the 180^o out of phase power clock signal shaper, the input power is 316.7 nW, output power is 275.4 nW and PCE is 86.96%.

V. Conclusion

The proposed signal shaper significantly reduces the overhead power consumption at the interface of RF power harvesting and PAL adiabatic logic family. At the same time, the shaper achieves fast settling time, which can be important when the RF signal is intermittent. Our future work will be focused on enhancing the robustness of the PAL logic and enabling the operation of logic at a lower supply voltage.

Acknowledgment

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