ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

Scalable 3D Ta:SiO_x Memristive Devices

Hao Jiang, Can Li, Peng Lin, Shuang Pi, Jianhua Joshua Yang, and Qiangfei Xia**

A highly reliable memristive device based on tantalum-doped silicon oxide is reported, which exhibits high uniformity, robust endurance (≈1×10^9 cycles), fast switching speed, long retention, and analog conductance modulation. Devices with junction areas ranging from microscale to as small as 60×15 nm^2 are fabricated and electrically characterized. ON-/OFF- conductance and reset current show weak area dependence when the device is relatively large, and they become proportional to the device area when further scaled down. Two-layer devices with repeatable switching behavior are achieved. The current study shows the potentials of Ta:SiO_2-based 3D vertical devices for memory and computing applications. It also suggests that doping of the switching layer is an efficient approach to engineer the performance of memristive devices.

1. Introduction

Memristive device, or resistance switch,[1–7] stands out as one of the leading candidates for emerging memory and computing technologies to address challenges in data-centric applications.[8–13] Although the memristive switching phenomenon has been observed in various materials, silicon oxide is a promising choice because it is well studied and fully compatible with the complementary metal–oxide–semiconductor technology.[14,15] However, functional devices based on pure SiO_x switching layers suffered from high switching voltages and limited endurance.[14–17] On the other hand, it has been demonstrated that introducing metallic dopants, such as Ni,[18] Zr,[19] and Pt,[20,21] into the SiO_2 layer improves the performances, although the highest reported endurance was around 3×10^7 cycles.[21]

Building memristor crossbars into 3D is an effective approach to provide high packing density and flexibility/efficiency for computing because of their massive and complex connectivity.[22,23] Conventional "wood-pile structure" is to repeatably stack planar crossbar layers, while shared vertical electrodes (VEs) are adopted in another 3D scheme.[24–28] Compared with the traditional 3D cross-point structure, the 3D vertical structure requires only one critical lithography step and hence is more bit cost-efficient.[25] However, 3D vertical structure with SiO_x switching layer has not been achieved yet.

Herein, we report a Ta:SiO_2 device with reliable bipolar memristive switching. After introducing Ta cations, our devices showed high uniformity, superior endurance (>10^9 cycles), fast switching speed, reliable retention, and analog modulation of device conductance. In addition, we studied the scaling ability of the Ta:SiO_2-based 3D vertical devices with sizes ranging from micro- to nanoscale (as small as 60×15 nm^2). The switching behavior shows weak dependence on area size when the device is relatively large; after that, state conductance and the operation current decrease when the device is further scaled down. We built 3D devices and achieved similar memristive behavior from both the top and bottom cells in a two-layer vertical device. Our work confirms that doping SiO_x is an efficient way to tailor properties of memristive devices, which has great scalability and stackability.

2. Results and Discussion

2.1. Ta:SiO_2 Thin Films Prepared by Co-Sputtering

The Ta:SiO_2 thins film were prepared by co-sputtering from Ta and SiO_2 targets. **Figure 1** schematically shows the principle of the co-sputtering process, in which two targets are sputtered simultaneously in the chamber. The SiO_2 target was sputtered at a constant radiofrequency (RF) power of 270 W, while the Ta target was sputtered with varied direct current (DC) powers ranging from 0 to 20 W. The atomic ratios for Ta dopants sputtered at 10 and 20 W were determined to be 14.1% and 22.5%, respectively. More importantly, the Ta in the thin films is in different valence states, as revealed by X-ray photoemission spectroscopic (XPS) characterization (**Figure 2**). The Ta 4f XPS spectra from films after 4 min Ar^+ sputtering inside the chamber were deconvolved into three chemical states of Ta: fully oxidic (Ta^{5+}), suboxidic, and metallic states.[29] The atomic ratios of the three states were calculated to be 57.65%/25.97%/16.39% (Figure 2a) and 34.91%/29.81%/35.28% (Figure 2b), respectively, for the two films prepared with different DC powers on Ta. The concentration of the Ta metallic state increased evidently in the film with a higher Ta sputtering power.

From electrical measurements (see Figure S1 in the Supporting Information), the device without Ta doping was hard breakdown, while the device based on $Ta_{22.5\%}$:SiO_2 was directly shorted. On the contrary, reliable memristive switching

Dr. H. Jiang,[+] Dr. C. Li, Dr. P. Lin, Dr. S. Pi, Prof. J. J. Yang, Prof. Q. Xia
Department of Electrical and Computer Engineering
University of Massachusetts
Amherst, MA 01003, USA
E-mail: hao.jiang@yale.edu; qxia@umass.edu

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/aelm.201800958.

[+]Present address: Department of Electrical Engineering, Yale University, New Haven, CT 06520, USA

DOI: 10.1002/aelm.201800958

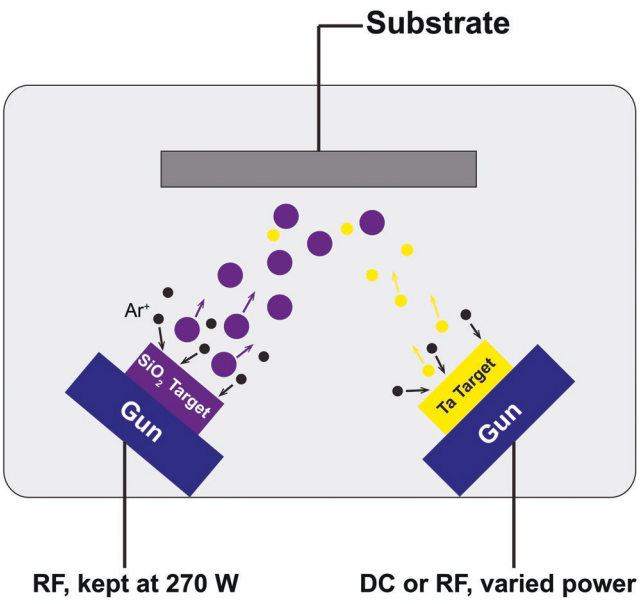

Figure 1. Schematic representation of the cosputtering process from Ta and SiO_2 targets. The SiO_2 target was sputtered with a RF power of 270 W and the Ta target was sputtered using a varied RF or DC power ranging from 0 to 20 W, which leads to thin films with different Ta doping concentrations.

behavior was obtained from the $Ta_{14.1\%}$:SiO_2 device. In later studies, we kept DC power at 10 W for Ta and RF power of 270 W for SiO_2 during the co-sputtering process.

2.2. Ta:SiO_2-Based Memristive Devices with Disk-Shaped Top Electrodes

Figure 3a schematically shows the structure of disk-shaped devices. It consists of a 40 nm Ta blanket layer as the bottom electrode (BE), 20 nm thick disk-shaped Pt with 20–200 µm diameters as the top electrode (TE), and a ≈5 nm Ta-doped SiO_2 switching layer sandwiched in between (see the Experimental Section for more fabrication details). During electrical measurements, the Pt TEs were biased, while the Ta BEs were grounded.

The device exhibited reliable bipolar memristive switching behavior after an electroforming or so-called "soft-breakdown" step.[30] Typical current–voltage (I–V) switching curves by DC sweeps for a 50 µm device are shown in Figure 3b. The device can be set to the low resistance state (LRS) with a negative voltage sweep (0 to −0.8 V) and reset back to the high resistance state (HRS) with a 0 to 1.5 V sweep. The device can be repeatedly switched for over 1×10^8 cycles without any feedback or power-limiting circuits (Figure 3c), two times higher than the endurance of the previously reported Pt: SiO_2[21] and Ti/SiO_2/C devices.[31] For the endurance measurement, we used 1 µs pulses (V_{set} = −0.9 V, V_{reset} = 1.5 V). The devices were programmed to LRS or HRS states and the resistance was read at 0.1 V DC voltage after every 2^n switching cycles (n = 1, 2, 3...).

2.3. Ta:SiO_2-Based Memristive Devices with the 3D Vertical Structure

The fabrication process of single-layer 3D vertical Ta:SiO_2 devices is shown step-by-step in Figure S2 in the Supporting Information. Pt horizontal electrodes (HEs) (varied thicknesses from 5 to 20 nm) and the 30 nm SiO_2 isolation layer were sequentially deposited. After patterned by standard photolithography, square holes (50 µm × 50 µm) were opened by dry etching. A ≈5 nm thick Ta: SiO_2 was then deposited as the switching material by co-sputtering. 150 nm thick Ta, serving as VEs, was DC sputtered to refill the holes. Finally, a 20 nm thick Pd capping layer was deposited on the top of Ta also by DC sputtering to reduce the contact resistance between electrodes and probe tips, and to prevent further oxidation of Ta under ambient environment. During electrical measurements, Ta VEs were always biased with Pt HEs grounded. **Figure 4**a shows the schematic representation of the fabricated device.

Typical I–V switching curves from Ta:SiO_2-based vertical devices with 15 nm Pt as HE are shown in Figure 4b. The vertical device switches in a bipolar mode although the polarity

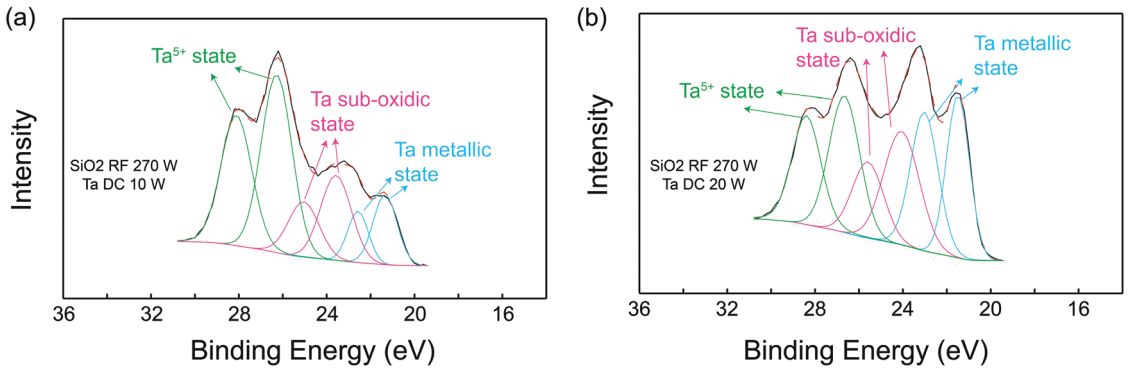

Figure 2. X-ray photoemission spectroscopy (XPS) spectra of the Ta:SiO_2 thin films prepared with a) 10 W and b) 20 W DC power on Ta. The Ta 4f XPS spectra were deconvolved into three chemical states of Ta: fully oxidic (Ta^{5+}), suboxidic, and metallic states. The atomic ratios of the three states were calculated to be a) 57.65%/25.97%/16.39% and b) 34.91%/29.81%/35.28%, respectively for the two films prepared with different DC powers on Ta. The concentration of the Ta metallic state increased evidently in the film prepared with a higher Ta sputtering power, suggesting an increase in film conductivity.

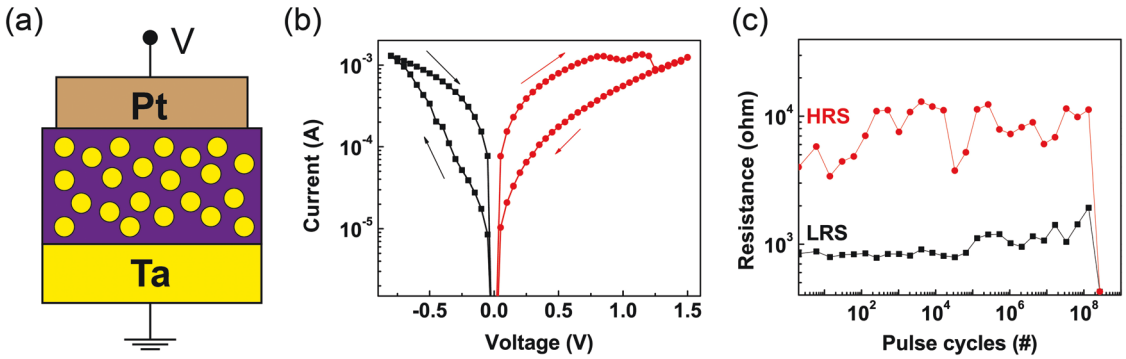

Figure 3. a) Schematic representation of the structure of traditional disk-shaped devices, with a Ta:SiO_2 switching layer sandwiched between Ta and Pt electrodes. During electrical measurements, the Pt electrode is biased and the Ta electrode is grounded. b) Typical bipolar memristive switching *I*–*V* curves. The arrows indicate the switching polarity. c) Endurance test results from traditional disk-shaped devices with a diameter of 50 µm. >1×10^8 switching cycles have been achieved with 1 µs programming pulses (set: −0.9 V; reset: 1.5 V). The device resistance was read with a 0.1 V DC voltage between switching events.

is reversed since the biasing scheme is opposite. A positive voltage sweep turned the device from HRS to LRS, while a subsequent negative voltage sweep switched the device back to the HRS. The small dimension of Pt HE concentrates the electrical field,[32] leading to the more abrupt switching, compared with that from the traditional devices (Figure 3b and Figure 4b) that have larger electrodes. Distributions of LRS/HRS resistances and V_{set}/V_{reset} from 100 consecutive cycles are shown in Figure 4c,d. The coefficients of variations (standard deviation/mean value) are 3.2% for LRS resistances and 23.2% for HRS resistances. The V_{set} has a mean of 0.6 V with a variation of 5.6%, while the mean and variation of the V_{reset} are −0.9 V and 3.0% respectively. Reducing the thickness of the Pt HE leads to lower operation current and higher programming voltages (see Figure S3 in the Supporting Information), consistent with previous studies.[33] The differences in device operation could be attributed to the much higher electrode resistance from the thinner Pt electrode.[33]

The endurance, switching speed, and retention were measured for Ta:SiO_2-based vertical devices with 15 nm Pt as HE

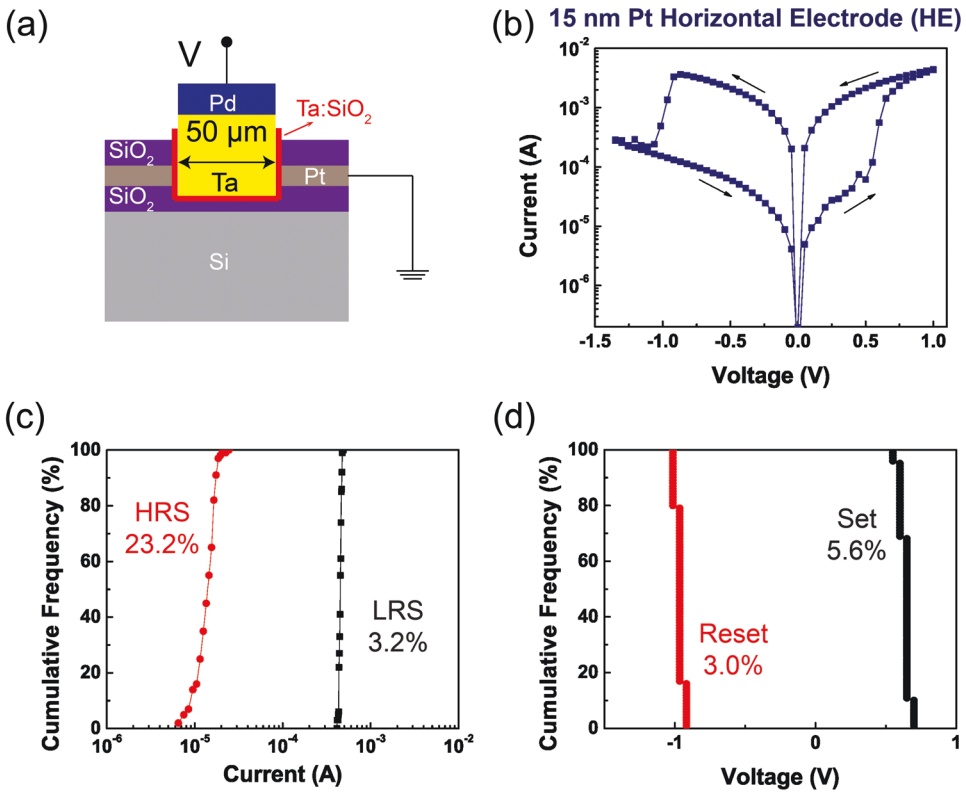

Figure 4. a) The schematic view of device cross section. b) Typical *I*–*V* curve from the vertical device with 15 nm Pt as the HE. The black arrows indicate the switching polarity. Cycle-to-cycle distributions of c) LRS/HRS resistances and d) set/reset voltages. The variations are 3.2% and 23.2% for LRS and HRS resistances, respectively, while 5.6% and 3.0% for set and reset voltages.

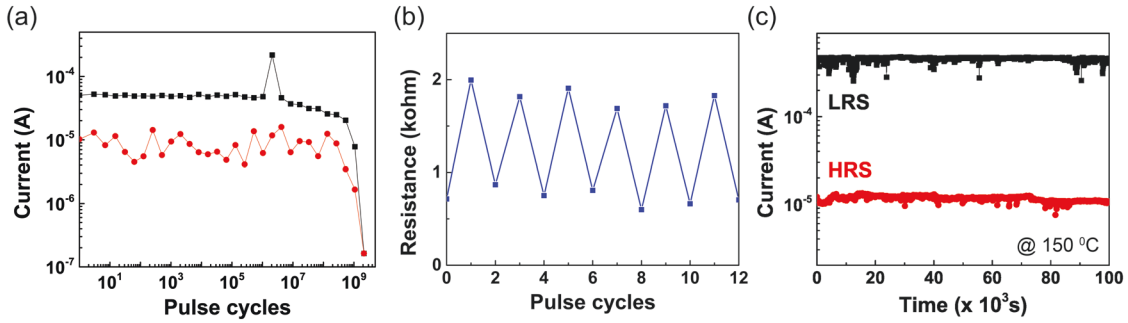

Figure 5. a) ≈1 × 10^9 switching cycles can be achieved from the Ta:SiO_2-based vertical devices with 15 nm Pt HE (pulse conditions: 1 V @ 1 µs for set and −1.3 V @ 1 µs for reset). b) Switching cycles between LRS and HRS with 5 ns electrical pulses (set: 2.2 V, reset: −3 V). A faster speed is expected if a shorter pulse is available and can be delivered to the switching location. c) Retention tests at both LRS and HRS show no evident changes after over 10^5 s when baked at 150 °C. For the endurance and switching speed tests, 0.1 V DC voltage was used to read the device resistance between switching events, while during the retention test, the device resistance was monitored every 60 s with 0.1 V pulses (≈20 ms).

(**Figure 5**). >10^9 open-loop switching cycles were achieved during the endurance test with 1 µs voltage pulses (V_{set}: 1 V, V_{reset}: −1.3 V). The device can be reliably switched between LRS and HRS using 5 ns electrical pulses (V_{set}: 2.2 V, V_{reset}: −3 V). A faster speed is expected if a shorter pulse is available and can be delivered to the switching junction through specially designed structures.[34,35] Furthermore, the Ta:SiO_2-based vertical device can retain both LRS and HRS without any degradation after over 10^5 s at 150 °C. It should be noted that the device was switched to LRS by a quasi-static DC sweep for the retention test (Figure 5c). The lower LRS resistance compared with that achieved by a voltage pulse (Figure 5a), could be attributed to a longer programming time under the same voltage amplitude.[36,37]

In response to 25 positive pulses (0.8 V, 1 µs) and then 25 negative pulses (–0.9 V, 1 µs), the Ta:SiO_2 memristive devices show analog switching behavior with their conductance gradually tuned with a train of electrical pulses, similar to the potentiation and depression behavior of biological synapses[38–40] (**Figure 6**a,b). Additionally, we tested the cycling performance of such analog conductance modulation behavior and over 600 potentiation/depression epochs (each epoch has 50 pulses) were achieved in the Ta:SiO_2 vertical device without any evident degradation (Figure 6c). Further material engineering can be used to increase the conductance window. For example, Kim et al. reported that a small amount of Si dopants into TaO_x can enlarge the oxygen vacancy (V_o) hopping distance and increase its drift speed, leading to a much larger dynamic range.[41]

2.4. Scaling of the Ta:SiO_2 Devices

To study the scaling capability of our Ta:SiO_2 devices, new structure is proposed and adopted (**Figure 7**). We used metal wires of various width instead of a blanket metal layer as HEs to achieve devices with different active areas. More schematics about the proposed new structure are shown in Figure S4 in the Supporting Information. The metal wires were fabricated by e-beam lithography, metallization, and lift-off. The switching layer, isolation layer, and VEs were fabricated in a fashion similar to regular devices. The width of Pt HEs was varied from 60 nm to 10 µm with their thickness kept at 15 nm. An optical image of the fabricated devices is shown in Figure 7a, with a typical scanning electron microscope (SEM) image of a 100 nm Pt HE shown in Figure 7b.

The typical *I*–*V* curves from devices with different sizes are shown in **Figure 8**a–d. The set/reset voltages exhibited negligible changes with the device size. The LRS/HRS resistances and the reset current are weakly dependent on the device size

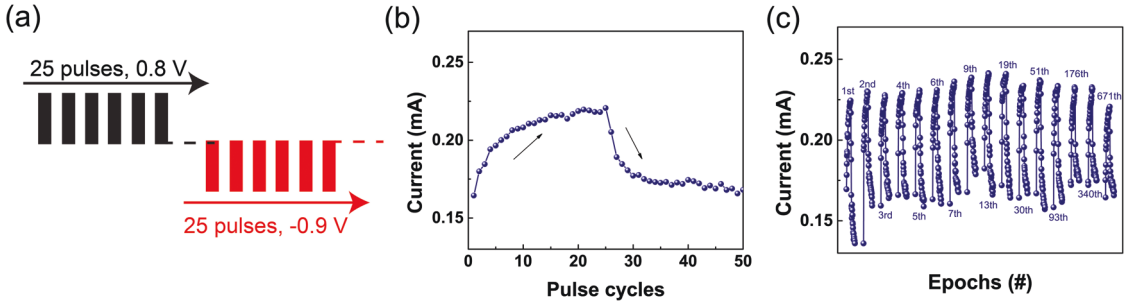

Figure 6. a) Pulse trains used in the analog tuning of the resistance state. 25 positive pulses (0.8 V, 1 µs) were used to potentiate the device, while another 25 negative pulses (–0.9 V, 1 µs) were used for depression. b) A typical analog switching epoch from the Ta:SiO_2 vertical device. The device conductance can be incrementally increased (potentiation) or decreased (depression) by consecutive positive or negative pulses. The conductance was measured at 0.1 V after each pulse. c) Over 600 potentiation/depression epochs (each epoch consists of 50 pulses) were achieved, suggesting that the device is promising as electronic synapse for unconventional computing.

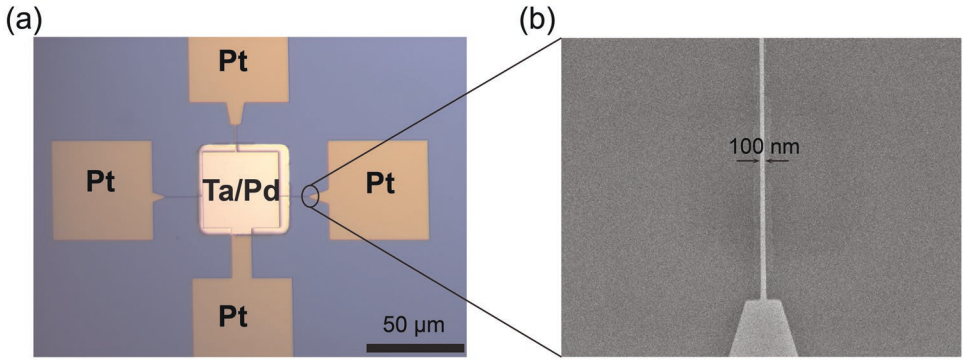

Figure 7. a) An optical image of devices with Pt nanowires of different widths as the horizontal electrodes. The active area of the device is determined by Pt thickness (t) × Pt wire width (L). In the study, the width of Pt wires is varied from 60 nm to 10 μm, while the thickness is kept at 15 nm. b) An SEM image of the 100 nm Pt wire.

either if the device is relatively large (for example $>1 \times 10^4$ nm^2 in this study). However, all of them are inversely proportional to the junction area when the device becomes smaller (Figure 8e,f). The LRS resistance can be understood as follows: I) If the device area is relatively large, both numbers and sizes of conduction channels can be statistically constant and irrespective of the device area change, in which case the dependence is weak. II) If the device area is much smaller (comparable to conduction channels), numbers/sizes of conduction channels start decreasing and hence the LRS resistance increases with the area size shrinking. In addition, a conduction channel with a lower concentration of defects can also lead to a higher LRS resistance, which is a non-negligible possibility. The HRS resistance is attributed to either the low conductivity of conduction channels[42] or possible formation of tunneling gap.[2] In the second-case scenario, the HRS resistance is determined by the leakage current through the gap with the ruptured conduction channels serving as virtual electrodes. Hence for both scenarios, the HRS resistance is strongly dependent on numbers/sizes/compositions of conduction channels and shows the same scaling behavior as the LRS resistance. Moreover, the reset current has a similar scaling trend as state resistances, which is reasonable since numbers/sizes/compositions of conduction channels decide the required power for Reset.

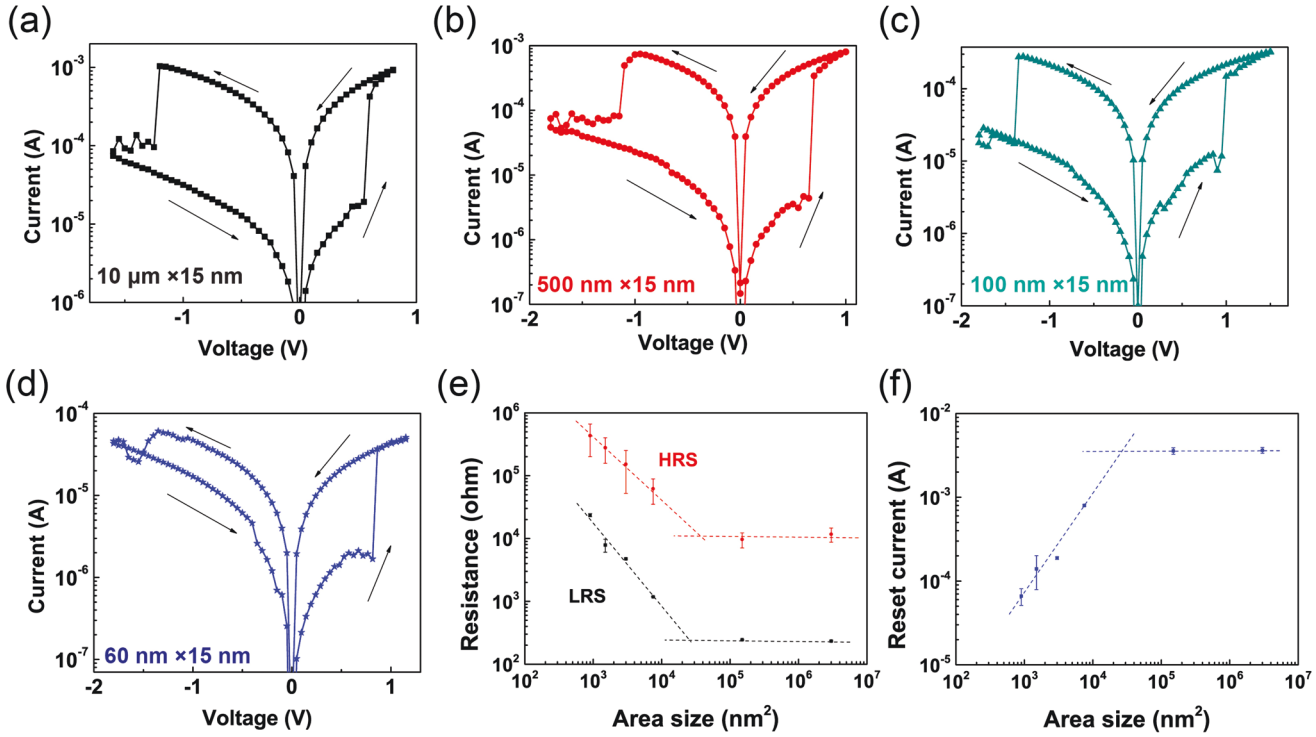

Figure 8. Typical bipolar I–V curves from vertical devices with a junction area of a) 10 μm × 15 nm, b) 500 nm × 15 nm, c) 100 nm × 15 nm, and d) 60 nm × 15 nm. The back arrows indicate the switching polarities. Dependences of e) LRS/HRS resistances and f) reset current on device sizes. The dash lines are for eye guidance. The device with a smaller area size shows smaller reset current and larger LRS/HRS resistances.

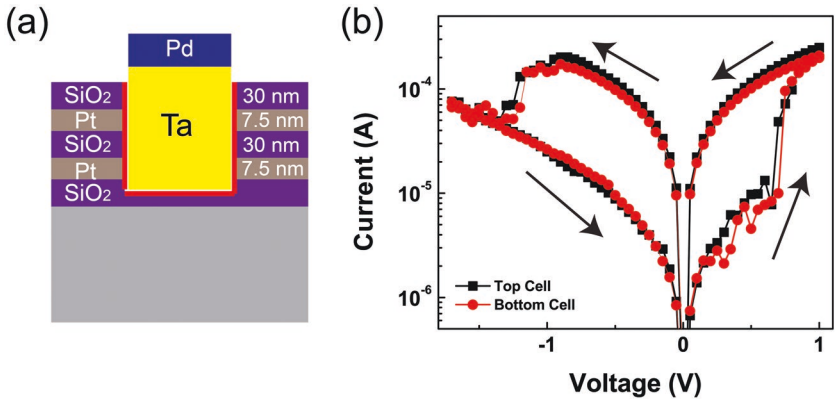

Figure 9. a) The schematic structure of two-layer Ta:SiO_2-based vertical devices. The Pt horizontal electrodes have a thickness of 7.5 nm. b) Typical bipolar switching curves from the top and bottom cell in the two-layer structure showing good repeatability in the switching. The black arrows indicate the switching polarity.

It should be noted that the increased electrode resistance may also contribute to the decrease of LRS/HRS conductance and reset current when the device size is scaled down. For example, the electrode with larger resistance can work as a current limiter and modulate the numbers/sizes/compositions of conduction channels during memristive switching.

The device starts to show rectifying behavior at HRS when scaled down to a size of 500 nm × 15 nm, which can be resulted from the lower defect concentration within conduction channel(s) near the Pt electrode after reset and hence a transition from Ohmic to rectifying contact at the oxide/Pt interface. Similar size-dependent phenomena can be observed from the TaO_x memristive system when scaled down from microscale to as small as $(30\ nm)^2$.[3]

2.5. 3D Stacking of the Ta:SiO_2 Devices

To demonstrate the 3D stacking capability, two-layer Ta:SiO_2 vertical devices were fabricated and electrically characterized. **Figure 9**a shows the schematic representation of the fabricated two-layer devices with 7.5 nm Pt as HEs. Typical bipolar memristive switching *I*–*V* curves from both the top and bottom cells are shown in Figure 9b. Their similar switching characteristics indicate the great potential of stacking multilayer Ta:SiO_2-based memristive devices with such cost-effective 3D vertical structure.

2.6. Proposed Switching Mechanism of the Ta:SiO_2 Devices

Finally, we believe that resistance switching in the Ta:SiO_2 devices is attributed to the formation and rupture of conduction channels through ionic motions (e.g., oxygen ions[21] and Ta cations[43–45]). The concurrent achievements in the ultrahigh switching speed and long state retention from our Ta:SiO_2 devices, consistent with previous work on Pt:SiO_2 by Choi et al.,[21] suggest the device is based on the ionic motion rather than electron movement. Nevertheless, further work including physical characterization of the composition of conduction channels and dynamics of ionic motion is needed to clarify the underlying physics of the switching.

3. Conclusion

We incorporated proper amount of Ta into SiO_2 thin films by co-sputtering and made memristive devices with high uniformity, robust endurance, fast switching speed, long retention, and analog conductance modulation. We made devices with different junction areas and studied the area-dependent switching behavior such as the resistance states and programming current. We further stacked the devices into 3D and achieved repeatable switching behavior for devices in different layers. Our work suggests that doping the switching layer is an efficient way in memristive device engineering.

4. Experimental Section

Device Fabrication: Si wafers with 100 nm thermal oxide on top were cleaned in a Piranha solution (H_2SO_4: H_2O_2 = 3: 1) for 15 min, followed by dipping in a diluted HF solution (1: 50) for 30 s. For the disk-shaped devices, a 40 nm thick Ta blanket layer was first deposited as BEs by DC sputtering. A ≈5 nm Ta-doped SiO_2 thin film was prepared by co-sputtering from Ta and SiO_2 targets (Ta: DC 10 W; SiO_2: RF 270 W). 20 nm thick Pt was then evaporated through a metal shadow mask as TEs, with a diameter ranging from 20 to 200 µm. For the 3D vertical devices, Pt and SiO_2 blanket layers were sequentially deposited by e-beam evaporation and plasma enhanced chemical vapor deposition. The thickness of Pt HEs was varied from 5 to 20 nm and the SiO_2 isolation layer was 30 nm. 50 µm × 50 µm square holes were made by using standard photolithography (365 nm wavelength) and dry etching. A ≈5 nm Ta-doped SiO_2 was co-sputtered as the switching material (Ta: DC 10 W and SiO_2: RF 270 W), followed by the sputtering of 150 nm thick Ta VEs into the holes. Finally, a 20 nm thick Pd capping layer was deposited on the top of the Ta to provide better electrical contact to the probe and to prevent oxidations of Ta under ambient environment. For the studies on scaling effects, Pt wires with 10 µm to 60 nm linewidth were prepared by using electron-beam lithography as the horizontal electrodes. During fabrication, a small part of Pt HEs or Pt pads as contacts were protected by glass covers or photoresists to avoid further depositions of other materials.

Electrical Characterization: An Agilent 4156b or Keithley 4200 semiconductor parameter analyzer in a voltage-sweep mode was used for the *I*–*V* measurements. The switching speed was measured with an Agilent 81160a pulse generator, while the other pulse measurements including cycling endurance and analog switching were conducted with a pulse-generator-unit in the Agilent 4156b. The retention tests at 150 °C were performed on a probe station equipped with a thermal chuck. The device resistances were periodically monitored with a low read voltage (0.1 V) to avoid disturbance of the device states. During the electrical measurements, for the disk-shaped devices, the Ta bottom electrodes were grounded, and the Pt top electrodes were biased; while for the 3D vertical devices, Ta vertical electrodes were biased with Pt horizontal electrodes grounded. Before electrical measurements, the contact was checked by landing two probe tips onto the same Pt HE.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported in part by the US National Science Foundation (NSF) (CCF-1740248) and the Semiconductor Research Corporation (SRC) (2018-NC-2766-B). The authors would like to thank John Nicholson from Center for Hierarchical Manufacturing (CHM) at the University of Massachusetts Amherst for technical help.

Conflict of Interest

The authors declare no conflict of interest.

Keywords

3D, doping, memristive device, silicon oxide, tantalum

Received: December 20, 2018
Revised: January 17, 2019
Published online:

[1] D. B. Strukov, G. S. Snider, D. R. Stewart, R. S. Williams, *Nature* **2008**, *453*, 80.
[2] J. J. Yang, M. D. Pickett, X. Li, D. A. Ohlberg, D. R. Stewart, R. S. Williams, *Nat. Nanotechnol.* **2008**, *3*, 429.
[3] M. J. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, Y. B. Kim, C. J. Kim, D. H. Seo, S. Seo, U. I. Chung, *Nat. Mater.* **2011**, *10*, 625.
[4] R. Waser, R. Dittmann, G. Staikov, K. Szot, *Adv. Mater.* **2009**, *21*, 2632.
[5] H. S. P. Wong, H. Y. Lee, S. Yu, Y. S. Chen, Y. Wu, P. S. Chen, B. Lee, F. T. Chen, M. J. Tsai, *Proc. IEEE* **2012**, *100*, 1951.
[6] Y. Li, S. Long, Q. Liu, H. B. Lv, S. Liu, M. Liu, *Chin. Sci. Bull.* **2011**, *56*, 3072.
[7] M. A. Zidan, J. P. Strachan, W. D. Lu, *Nat. Electron.* **2018**, *1*, 22.
[8] J. Gantz, D. Reinsel, The Digital Universe In 2020: Big Data, Bigger Digital Shadows, and Biggest Growth in the Far East, http://www.emc.com/collateral/analyst-reports/idc-the-digital-universe-in-2020.pdf (accessed: November 2018).
[9] C. S. Hwang, *Adv. Electron. Mater.* **2015**, *1*, 1400056.
[10] J. J. Yang, D. B. Strukov, D. R. Stewart, *Nat. Nanotechnol.* **2013**, *8*, 13.
[11] C. Li, M. Hu, Y. Li, H. Jiang, N. Ge, E. Montgomery, J. Zhang, W. Song, N. Davila, C. E. Graves, Z. Li, J. P. Strachan, P. Lin, Z. Wang, M. Barnell, Q. Wu, R. S. Williams, J. J. Yang, Q. Xia, *Nat. Electron.* **2018**, *1*, 52.
[12] Z. Wang, S. Joshi, S. E. Savel'ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li, Q. Wu, M. Barnell, G. L. Li, H. L. Xin, R. S. Williams, Q. Xia, J. J. Yang, *Nat. Mater.* **2017**, *16*, 101.
[13] S. Pi, C. Li, H. Jiang, W. Xia, H. L. Xin, J. J. Yang, Q. Xia, *Nat. Nanotechnol.* **2019**, *14*, 35.
[14] J. Yao, Z. Sun, L. Zhong, D. Natelson, J. M. Tour, *Nano Lett.* **2010**, *10*, 4105.
[15] A. Mehonic, A. L. Shluger, D. Gao, I. Valov, E. Miranda, D. Ielmini, A. Bricalli, E. Ambrosi, C. Li, J. J. Yang, Q. Xia, A. J. Kenyon, *Adv. Mater.* **2018**, *30*, 1801187.
[16] Y. Chang, P. Chen, B. Fowler, Y. Chen, F. Xue, Y. Wang, F. Zhou, J. C. Lee, *J. Appl. Phys.* **2012**, *112*, 123702.
[17] C. Li, L. Han, H. Jiang, M. H. Jang, P. Lin, Q. Wu, M. Barnell, J. J. Yang, H. L. Xin, Q. Xia, *Nat. Commun.* **2017**, *8*, 15666.
[18] T. Tsai, K. Chang, T. Chang, Y. Syu, S. Chuang, G. Chang, G. Liu, M. Chen, H. Huang, S. Liu, Y. Tai, D. Gan, Y. Yang, T. Young, B. Tseng, K. Chen, M. Tsai, C. Ye, H. Wang, S. M. Sze, *IEEE Electron Device Lett.* **2012**, *33*, 1696.
[19] K. Chang, T. Chang, T. Tsai, R. Zhang, Y. Hung, Y. Syu, Y. Chang, M. Chen, T. Chu, H. Chen, C. Pan, C. Shih, J. Zheng, S. M. Sze, *Nanoscale Res. Lett.* **2015**, *10*, 120.
[20] B. J. Choi, A. B. K. Chen, X. Yang, I. Chen, *Adv. Mater.* **2011**, *23*, 3847.
[21] B. J. Choi, A. C. Torrezan, K. J. Norris, F. Miao, J. P. Strachan, M. Zhang, D. A. A. Ohlberg, N. P. Kobayashi, J. J. Yang, R. S. Williams, *Nano Lett.* **2013**, *13*, 3213.
[22] M. M. Shulaker, G. Hills, R. S. Park, R. T. Howe, K. Saraswat, H. S. P. Wong, S. Mitra, *Nature* **2017**, *547*, 74.
[23] B. Chakrabarti, M. A. Lastras-Montaño, G. Adam, M. Prezioso, B. Hoskins, M. Payvand, A. Madhavan, A. Ghofrani, L. Theogarajan, K.-T. Cheng, D. B. Strukov, *Sci. Rep.* **2017**, *7*, 42429.
[24] I. G. Baek, C. J. Park, H. Ju, D. J. Seong, H. S. Ahn, J. H. Kim, M. K. Yang, S. H. Song, E. M. Kim, S. O. Park, C. H. Park, C. W. Song, G. T. Jeong, S. Choi, H. K. Kang, C. Chung, presented at *Int. Elect. Dev. Meet.*, Washington, DC, USA, December **2011**.
[25] S. Yu, H. Chen, B. Gao, J. Kang, H. P. Wong, *ACS Nano* **2013**, *7*, 2320.
[26] M. Yu, Y. Cai, Z. Wang, Y. Fang, Y. Liu, Z. Yu, Y. Pan, Z. Zhang, J. Tan, X. Yang, M. Li, R. Huang, *Sci. Rep.* **2016**, *6*, 21020.
[27] Y. Bai, H. Wu, K. Wang, R. Wu, L. Song, T. Li, J. Wang, Z. Yu, H. Qian, *Sci. Rep.* **2015**, *5*, 13785.
[28] Q. Luo, X. Xu, H. Liu, H. Lv, T. Gong, S. Long, Q. Liu, H. Sun, W. Banerjee, L. Li, J. Gao, N. Lu, S. S. Chung, J. Li, M. Liu, presented at *Int. Elect. Dev. Meet.*, Washington, DC, USA, December **2015**.
[29] S. Kim, S. Choi, J. Lee, W. D. Lu, *ACS Nano* **2014**, *8*, 10262.
[30] J. J. Yang, F. Miao, M. D. Pickett, D. A. A. Ohlberg, D. R. Stewart, C. N. Lau, R. S. Williams, *Nanotechnology* **2009**, *20*, 215201.
[31] A. Bricalli, E. Ambrosi, M. Laudato, M. Maestro, R. Rodriguez, D. Ielmini, presented at *Int. Elect. Dev. Meet.*, San Francisco, CA, USA, December **2016**.
[32] Z. P. Zhang, Y. Wu, H. S. P. Wong, S. S. Wong, *IEEE Electron Device Lett.* **2013**, *34*, 1005.
[33] H. Chen, S. Yu, B. Gao, R. Liu, Z. Jiang, Y. Deng, B. Chen, J. Kang, H. P. Wang, *Nanotechnology* **2013**, *24*, 465201.
[34] A. C. Torrezan, J. P. Strachan, G. Mediros-Ribeiro, R. S. Williams, *Nanotechnology* **2011**, *22*, 485203.
[35] B. J. Choi, A. C. Torrezan, J. P. Strachan, P. G. Kotula, A. J. Lohn, M. J. Marinella, Z. Li, R. S. Williams, J. J. Yang, *Adv. Funct. Mater.* **2016**, *26*, 5290.
[36] G. Wang, S. B. Long, Z. Yu, M. Y. Zhang, Y. Li, D. L. Xu, H. B. Lv, Q. Liu, X. B. Yan, M. Wang, X. X. Xu, H. T. Liu, B. Yang, M. Liu, *Nanoscale Res. Lett.* **2015**, *10*, 39.
[37] S. Yu, H. S. P. Wong, *IEEE Trans. Electron Devices* **2011**, *58*, 1352.
[38] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, W. Lu, *Nano Lett.* **2010**, *10*, 1297.
[39] P. Yao, H. Wu, B. Gao, S. B. Eryilmaz, X. Huang, W. Zhang, Q. Zhang, N. Deng, L. Shi, H. S. P. Wong, H. Qian, *Nat. Commun.* **2017**, *8*, 15199.

[40] M. Prezioso, F. Merrikh-Bayat, B. Hoskins, G. Adams, K. K. Likharev, D. B. Strukov, *Nature* **2015**, *521*, 61.
[41] S. Kim, S. H. Choi, J. Lee, W. D. Lu, *ACS Nano* **2014**, *8*, 10262.
[42] F. Miao, J. P. Strachan, J. J. Yang, M. X. Zhang, I. Goldfarb, A. C. Torrezan, P. Eschbach, R. D. Kelley, G. Medeiros-Ribeiro, R. S. Williams, *Adv. Mater.* **2011**, *23*, 5633.
[43] A. Wedig, M. Luebben, D. Y. Cho, M. Moors, K. Skaja, V. Rana, T. Hasegawa, K. K. Adepalli, B. Yildiz, R. Waser, I. Valov, *Nat. Nanotechnol.* **2016**, *11*, 67.
[44] H. Jiang, L. Han, P. Lin, Z. Wang, M. H. Jang, Q. Wu, M. Barnell, J. J. Yang, H. L. Xin, Q. Xia, *Sci. Rep.* **2016**, *6*, 28525.
[45] I. Valov, M. Luebben, A. Wedig, R. Waser, *ECS Trans.* **2016**, *75*, 27.

