Current collapse in high-Al Channel AlGaN HFETs

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We report the first study of current collapse in ultra-wide bandgap high-Al AlGaN channel heterostructure field-effect transistors (HFETs) using short-pulse biasing. Our results show that, under applied pulsed gate and drain voltages, the current collapse results from increased resistance of the source- gate and gate-drain regions but not from the channel under the gate. We also show that passivation of access regions of the high-Al channel HFET with SiNx results in significant reduction in current collapse.

Although significant progress has been made in the III-N based high-power/ high-frequency electronic devices, the gate- and drain- lag also referred to as current collapse is still a major challenge as it degrades the microwave output performance as well as increases the dynamic on-resistance of power switches.[1, 2, 3, 4, 5, 6]. The most common way of suppressing current collapse in AlGaN/GaN HFETs is surface passivation using Si_3N_4 [7,8,9,10,11]. Recently, several groups including ours, have reported HFETs with high-Al AlGaN channels[12,13,14,15,16,17,18,19,20]. These devices are promising for high-voltage and high-power applications due to increased critical fields in high-Al AlGaN material. However, to the best of our knowledge, to date there are no reports of studies on current collapse phenomena in high-Al AlGaN channel HFETs. In this work we for the first time report on the current collapse effects in

high Al AlGaN channel HFETs, identify the device regions responsible for the collapse and show that efficient suppression of current collapse can be achieved using Si_3N_4 passivation.

The device epilayer structure shown in Figure 1 was deposited on a 3 μm thick AlN /sapphire template using a pulsed metalorganic- chemical-vapor deposition (MOCVD) process. Details of the growth procedure are reported in[21]. The off axis (102) X-ray peak line width for the AlN buffers was measured to be about 330 arcsecs, which based on our past calibrations, translates to an overall defect-density ~ (1-3)×10^8 cm^{-2}. The thickness of undoped $Al_{0.40}Ga_{0.60}N$ channel and the Si-doped *n*-$Al_{0.65}Ga_{0.35}N$ barrier layers for our structures were 0.5 μm and 300 Å respectively. The barrier layer carrier concentration due to Si-doping was approximately 4-6×10^{18} cm^{-3}, as measured from the capacitance-voltage ($1/C^2$ vs V) plot. The sheet resistance (R_{sh}) value for our heterojunction was ~1900Ω /□ as measured by the Eddy current method. The 2DEG electron sheet density in our sample was Ns= 1.9×10^{13} cm^{-2} according to C-V data. The total polarization charge at the interface calculated as per[22] is 1.76×10^{13} cm^{-2}. The threshold-voltage V_T = -13.7 V was determined by C-V measurements and it was in good agreement with that from device current-voltage (I-V) characteristics. Using the measured electron sheet density and the barrier thickness of 300A, we obtain the estimated voltage to deplete the 2DEG, V_{2DEG} = $qNs/C_1 \approx 11$ V , where C_1 is the unit area barrier capacitance. The actual threshold voltage of 13.7 V is higher because the barrier layer in our structure is doped, and around 2 V is needed to deplete the barrier layer.

The device fabrication was started by mesa isolation step with Cl_2-based inductively coupled plasma reactive ion-etching (ICP-RIE) followed by source/drain ohmic metal deposition. The source-drain ohmic-contacts consisted of a Zr/Al/Mo/Au (150/1000/400/300 Å)[12] metal stack that was deposited using an e-beam process and it was annealed for 30 second at

950 °C under N_2 using rapid thermal annealing (RTA). We achieved linear source-drain ohmic-contacts with a contact resistance as low as 1.64 Ω-mm which gives an equivalent ohmic specific contact resistivity of $\sim 1.4\times10^{-5}$ Ω-cm^2. The gate-metal consisted of Ni/Au (1000Å/2000Å). Identical devices were passivated with a 300 nm thick Si_3N_4 film deposited by plasma enhanced chemical vapor deposition (PECVD).

The static and pulsed output I-V characteristics (I_{DS} vs V_{DS}) were measured using the DIVA D265 dynamic IV analyzer. Positive gate and negative drain pulses with the quiescent points $V_{GS,Q}$ = -15 V (below the threshold voltage) and $V_{DS,Q}$ = 20 V correspondingly. Pulse widths for our study varied from 500 ns to 1 ms with duty cycle of 100.

Fig 2 (a) shows the static and pulsed I-Vs of un-passivated $Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ HFET, with a 1.8μm long gate (L_G), in a 6 μm source-drain spacing. Clear saturation is observed, with peak currents ~0.4 A/mm at V_G=2V and V_D=20V. Under gate and drain pulsing with above mentioned quiescent bias points, the device shows significant reduction in the drain current (current collapse). These observations are similar to those on unpassivated AlGaN/GaN HFETs[3,4, 23,24,25,26,27]. Fig. 2 (b) includes the same data for devices that were surface passivated using Si_3N_4. The data show that the Si_3N_4 surface passivation layer effectively removes the current collapse in our high-Al AlGaN channel HFETs. Fig. 3 shows that, as pulse width increases from 100 ns to 1000 μs, the degree of collapse reduces due to sufficient time the device spends in the on- state for electron de-trapping. As seen from Fig. 3, the characteristic time for electron emission from traps range from approximately 1 μs to 1 ms. However, the most important contribution comes from traps with characteristic emission time of approximately 200 μs. The corresponding emission rate of 5×10^3 s^{-1} is considerably, by two-three orders of magnitude, lower than that observed in the work by O. Mitrofanov and M. Manfra[28] for

AlGaN/GaN HFETs. The difference is understandable considering larger bandgap of high-Al devices used in our study. Fig. 3 inset shows the drain current I-Vs for two different on-time pulse durations. At a pulse width of 1 ms, the degree of collapse is significantly lower and the dynamic drain current returns to ~90% of the static current value.

Next, we carried out additional experiments to establish which device regions are primarily responsible for the observed current collapse. For these, we used gated transmission line model (GTLM) measurements as described in.[29] The gate lengths in sequential sections of the GTLM varied from L_G=10 μm to L_G=100 μm, whereas the gate- source and the gate- drain openings were kept constant at L_{GS}=L_{GD}=10 μm. The width of all GTLM sections was W=200 μm. Two levels of drain bias have been used: below and above the knee voltage in order to study the device behavior in both linear and saturation regimes. The technique used is described below following the approach of [29].

In linear regime, the total resistance of the GTLM section measured at any time during the transient process is given by:

$$R_T(t) = 2R_C + R_{GS} + R_{CH}(V_G) + R_{GD} \qquad (1)$$

Where R_C, R_{GS} and R_{GD} are the contact resistance and the resistances of the gate-source and the gate-drain openings, respectively and R_{CH} is the gate voltage dependent resistance of the channel under the gate. We assume that all components of the total resistance R_T, except R_C, can be time-dependent due to trapping effects. At low drain bias the components of the total resistance can be expressed as

$$R_{GS} = R_{GD} = R_{SA} \times L_{GS}/W \qquad (2a)$$

$$R_{CH}(L_G) = R_{SG} \times L_G/W \qquad (2b)$$

where R_{SA} and R_{SG} are the sheet resistances of the channel in the access regions and under the gate correspondingly. The total resistance of the GTLM section can therefore be rewritten as

$$R_T(t) = 2R_C + 2R_{SA} \times \frac{L_{GS}}{W} + R_{SG} \times \frac{L_G}{W} \qquad (2c)$$

The total resistance of the GTLM sections $R_T(0)$ and $R_T(\tau)$ were measured in the beginning of the transient (instantaneous response) and at the end of the pulse (when the current is close to its steady state value), respectively. The corresponding dependencies of $R_T(0)$ and $R_T(\tau)$ are shown in Fig. 4 (a). The slope of the $R_T(L_G)$ line represents the channel resistance under the gate, while the intercept $R_T \; at \; L_G = 0$ provides the sum of the contact resistances $2R_C$ and the gate-source and gate-drain access region resistances $R_{GS} + R_{GD}$ in the beginning and at the end of the transient. Fig. 4 (a) also shows the change $\Delta R = R_T(\tau) - R_T(0)$ of the total device resistance as a function of gate length L_G. Fig. 4(a) shows, $R_T(\tau) \; and \; R_T(0)$ versus L_G to have near identical slopes but different intercepts. Therefore, the time dependence of the total resistance in the linear regime is caused by the dynamic modulation of the gate-source and gate-drain access region resistances, whereas the channel resistance under the gate remains unaffected.

Fig. 4 (b) shows the GTLM measurement results for a high drain bias case corresponding to the current saturation regime. Since the gate length in our GTLM exceeds 10 μm one can see that the velocity saturation effects can be ignored (see, e.g. the estimates for AlGaN/GaN HFETs in [29]. The velocity saturation effects in high-Al AlGaN HFETs are even weaker due to lower electron mobility). In this case the saturation current of the HFET, I_{DS} is given by [30]

$$I_{DS} = \frac{g_{CH}(V_G - V_T)}{2(1 + g_{CH}R_S)}, \qquad (3)$$

Where $g_{CH} = \frac{1}{R_{CH}(L_G)}$, is the channel conductance under the gate, $R_{CH}(L_G)$ is given by Eq. 2(b), V_G is the gate voltage, V_T is the threshold voltage and R_S is the HFET source-gate series resistance (including the contact resistance). Using a term "trans-resistance", $R_{TR} = (V_G - V_T)/(2I_{DS})$, the equation (3) can be rewritten as

$$R_{TR} = \frac{V_G - V_T}{2I_{DS}} = R_S + \frac{1}{g_{CH}} = R_S + R_{CH}(L_G) \qquad (4)$$

Equation (4) describes similar gate length dependence of R_{TR} for the saturation regime as the equation 2(c) for the linear regime. The experimental dependence of $R_{TR}(L_G)$ is plotted in Fig. 4(b). These results show that, in the saturation regime, the current transient process is also controlled by the variation of access region resistance rather than by the change of the resistance under the gate. Note that, the saturation current in HFETs is mainly affected by the source access resistance R_S, as seen from Eq. (3) and therefore, Fig. 4(b) shows the change of R_S during the transient. However, it is reasonable to expect that the drain resistance is also modulated and even to a larger degree because the voltage between drain and gate is higher than that between gate and source. The drain resistance modulation is evident from the dynamic I-Vs of Fig. 2a, where one can see significant knee voltage run away in spite of lower dynamic drain currents. This effect can be explained by additional voltage drop ΔV_D across additional dynamic drain resistance ΔR_D: $\Delta V_D = I_{DS} \times \Delta R_D$.

Our observations show that the manifestations of current collapse in high-Al AlGaN channel HFETs are qualitatively similar to those observed in AlGaN/GaN HFETs and other III-N devices (see, e.g.[31]); thus it can be mitigated by using similar passivation techniques and strategies. Therefore, we believe that the mechanism of current collapse in high-Al AlGaN channel HFETs includes one or both of: (i) carrier trapping in the access regions and (ii) strain modulation in the

access regions as first suggested in[29]and later also referred to as inverse piezoelectric effect.[32] We are conducting more detailed studies to determine the exact dominant mechanism of current collapse in these new devices and the results will be published when available.

In conclusion, analysis of transient processes and dynamic I-Vs in in high-Al AlGaN channel HFET showed that the access region resistances are mainly responsible for the current collapse. The channel resistance under the gate is practically not affected by electron trapping. The characteristic emission rates for trapped electrons is significantly lower than those observed in AlGaN/GaN HFETs due to larger bandgap of high-Al HFETs. The current collapse was successfully mitigated by using Si_3N_4 surface passivation.

Acknowledgment:

This research is partially supported by National Science Foundation (NSF), ECCS Award nos. 1711322 and 1810116 by program director Dr. Dimitris Pavlidis. The authors would like to acknowledge partial support of this work by DARPA DREAM contract (ONR N00014-18-1-2033), Program Manager Dr. Young-Kai Chen, monitored by ONR, Dr. Paul Maki and ARO contract W911NF-18-1-0029 monitored by Dr. M. Gerhold. The authors also acknowledge the support from the University of South Carolina through the ASPIRE program.

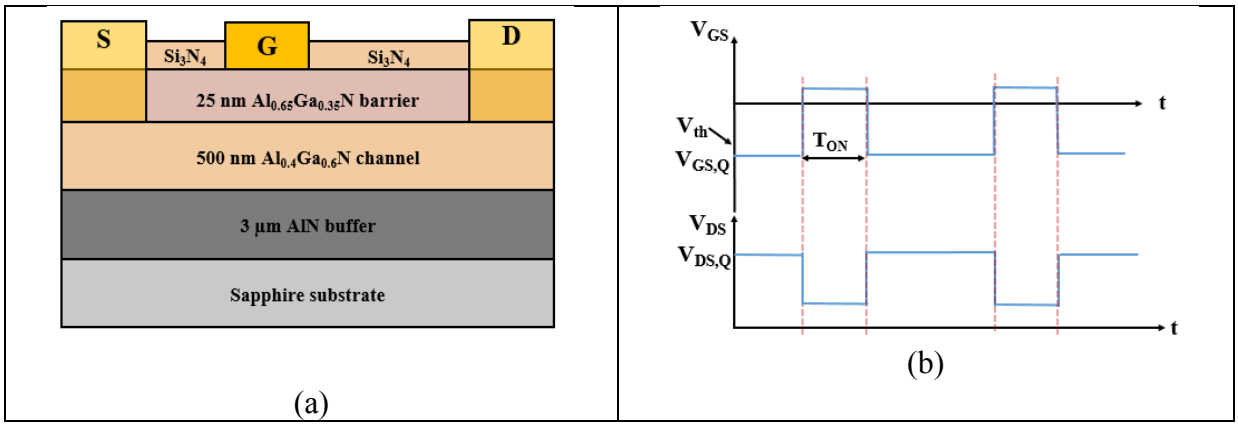

Fig. 1. (a) The Device structure of the HFET. (b) Time diagram of Gate and Drain pulses.

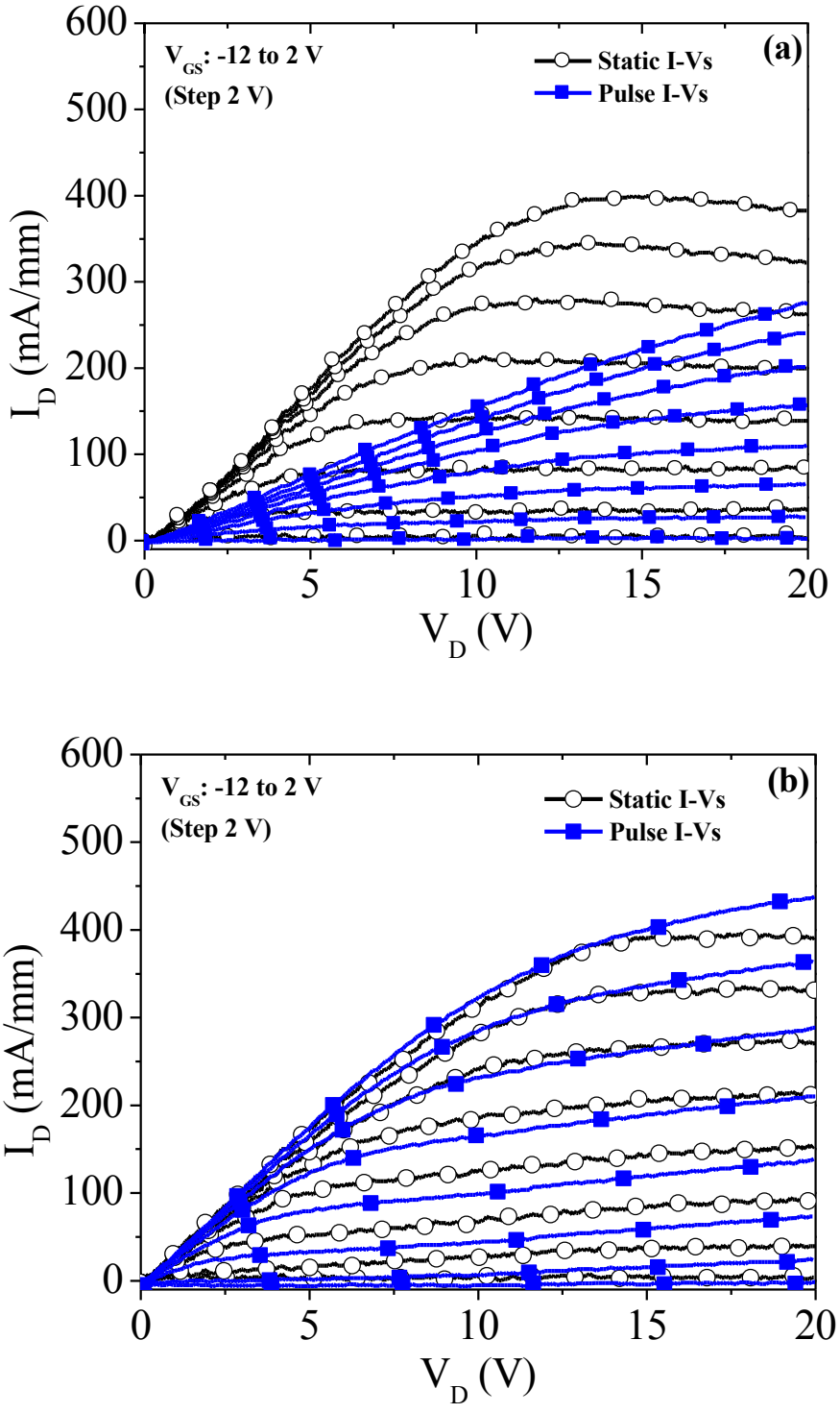

Fig. 2. Static and Pulse I-V characteristics of (a) HFET without passivation and (b) Si_3N_4 passivated HFET. Pulse duration T_{ON}= 500 ns, pulse period T= 500 µs.

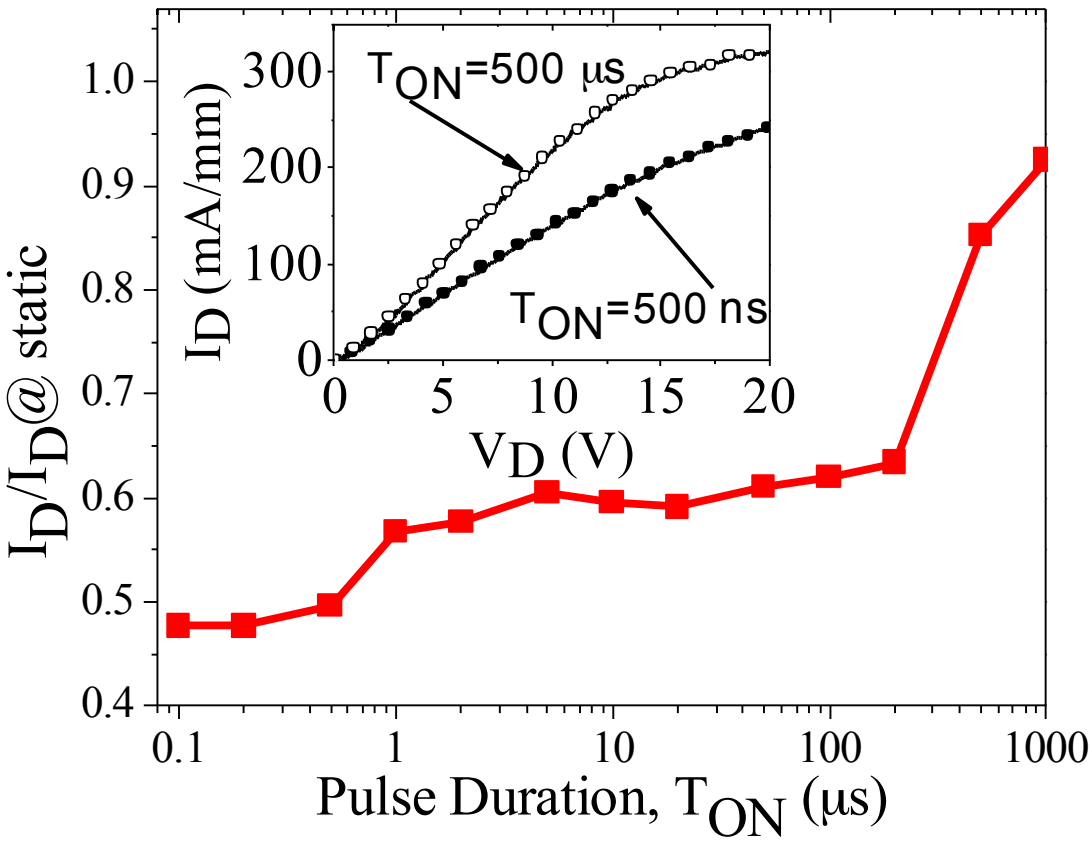

Fig. 3. ON time (T_{ON}) dependence of the non-passivated HFET drain current. The quiescent bias point is $V_{GS,Q}$ = -15V, $V_{DS,\,Q}$ = 20 V. Inset shows pulse I-V characteristics of un-passivated HFET with different pulse width.

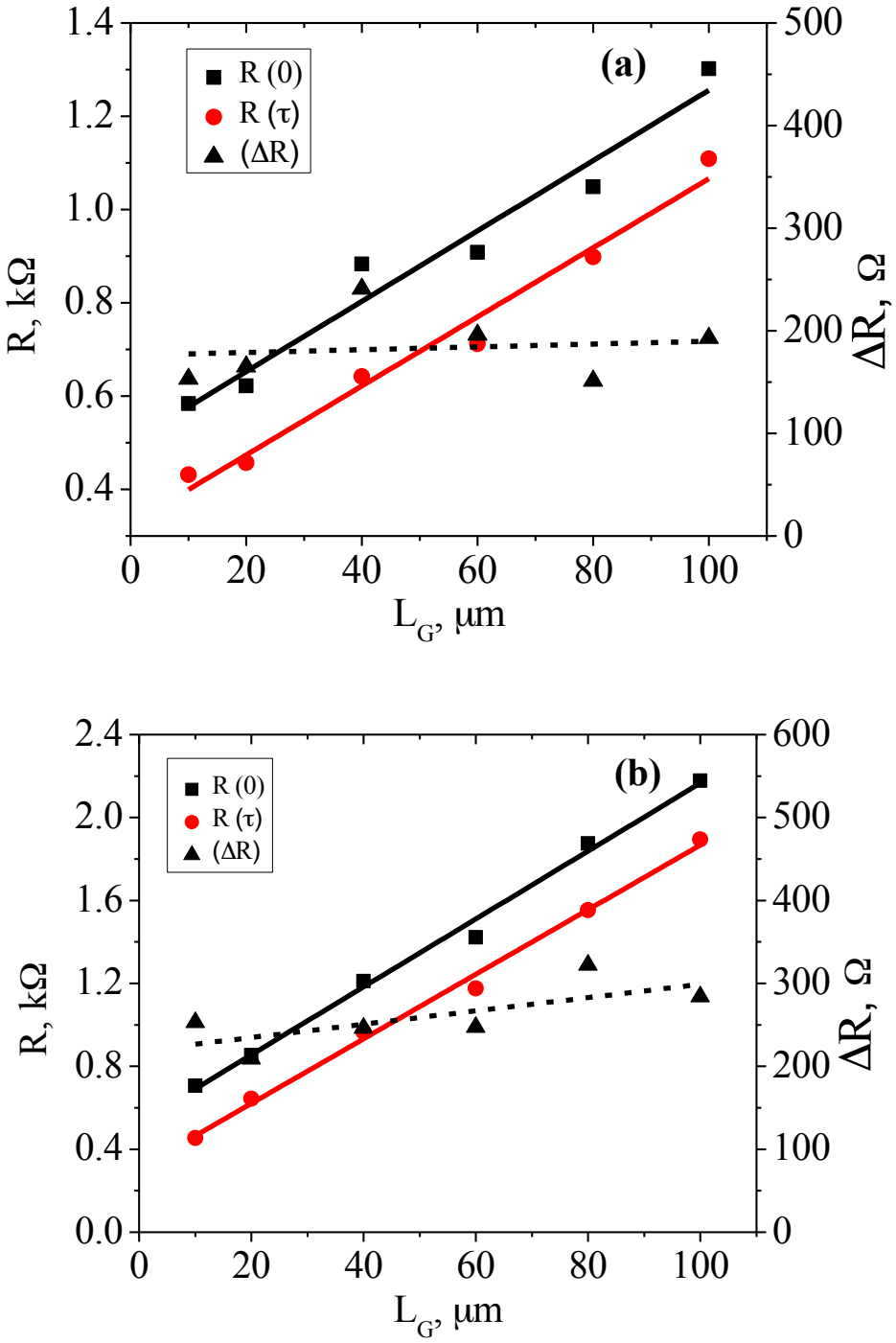

Fig. 4. Gate length dependencies of total resistance in the linear regime (a) and transfer resistance in the saturation regime (b). Rectangles and circles show the data measured in the beginning and at the end of the transient, respectively. Dashed lines with the triangles show the gate length dependencies of the change in device resistances ΔR.

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