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Spatially Precise Transfer of Patterned Monolayer WS_2 and MoS_2 with Features Larger than 10^4 μm^2 Directly from Multilayer Sources

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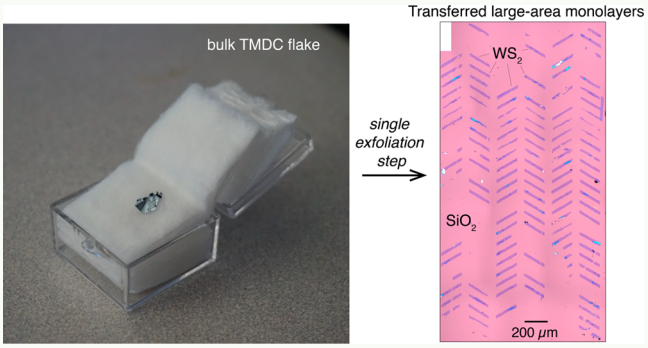
Supporting Information

ABSTRACT: A current challenge in the processing of 2D materials, or "van der Waals (vdW) solids", is the transfer of 2D layers from source crystals and growth substrates onto target substrates. Transfer—as opposed to direct growth and patterning on the target—enables low-temperature processing of the target as well as the use of diverse target materials. These two attributes will allow the assembly of vdW heterostructures to realize devices exploiting the unique properties of vdW materials. Until now, however, there has been no effective method for transferring regions of monolayer material of controlled shape from a multilayer source. We introduce such a method and demonstrate its use in the spatially controlled transfer of arrays of single-layer MoS_2 and WS_2 sheets from multilayer crystals onto SiO_2 substrates. These sheets have lateral sizes exceeding 100 μm and are electronically continuous. The method offers a scalable route to parallel manufacturing of complex circuits and devices from vdW materials.



KEYWORDS: *nanomanufacturing, transfer, scalable, two-dimensional materials, MoS_2, WS_2, exfoliation*

INTRODUCTION

van der Waals (vdW) solids are composed of single- to few-atom-thick "two-dimensional" layers loosely bound to each other by van der Waals forces. Their thinness results in extreme mechanical flexibility and exceptional properties, enabling many applications[1] including in electronics,[2,3] photonics,[4] and chemical sensing.[5] A growing appreciation of the properties of 2D materials has enabled increasingly sophisticated material heterostructures[6,7] and increasingly integrated circuits containing, to date, over 100 2D material-based devices.[8] Interfaces between semiconducting, conducting, and insulating 2D materials find applications in, for example, field-effect transistors (FETs),[9] memristive memories,[10] diodes,[11] including light-emitting diodes (LEDs),[12,13] photodetectors,[12] photovoltaics,[14] and catalysis.[14]

However, to fabricate multimaterial 2D structures through sequential vapor-phase deposition, lithography, and etching steps on a single substrate—as in conventional semiconductor manufacturing—is fraught with difficulties. First, although single-layer vapor-phase deposition techniques such as chemical vapor deposition are now maturing,[1,15] the development of processes to deposit one specific 2D material on top of another, while possible,[16,17] is time-consuming (e.g., 26 h required[15] for uniform monolayer MoS_2 or WS_2 on SiO_2). Moreover, continuous layers of uniform thickness may prove impractical to produce because of lattice mismatches or chemical incompatibilities. While some fabrication flows actually exploit selective deposition characteristics to form overlap junctions (<1 μm) at pattern edges,[18,19] many applications such as LED displays will demand larger ($\gtrsim$10 μm) planar junctions between sheets of material. Second, when a particular layer of a heterostructure needs to be patterned without destroying those underneath—e.g., to enable electrical contact—either extremely high etch selectivity or atomically precise control of etching depth is needed. These requirements are likely to be impractical to achieve because of difficulties in selecting appropriate etchants and inevitable etch-rate spatial nonuniformities.

Third, the high temperatures of typically 400−1000 °C required for vapor-phase deposition[1,16] impose challenging

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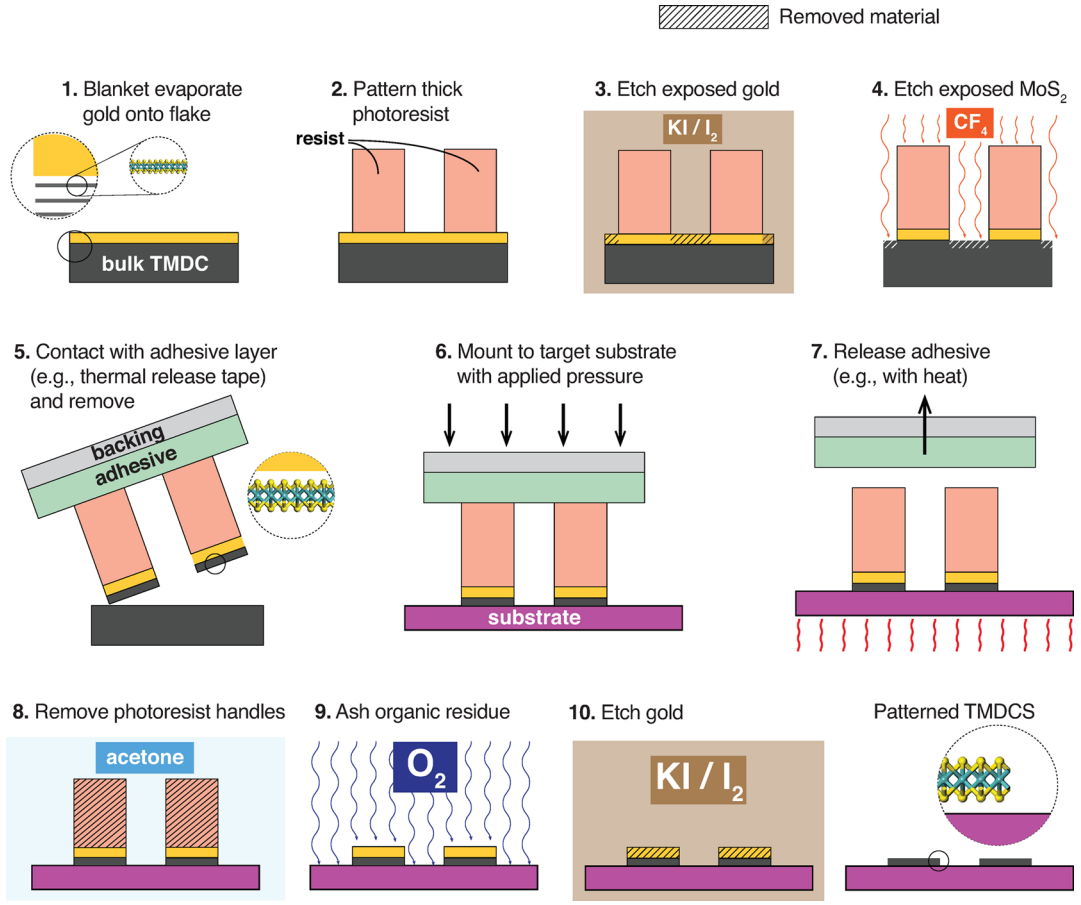

Figure 1. Process for producing patterned monolayers. The process for patterning and transferring van der Waals monolayers uses standard photolithography techniques. It relies on the use of a thick handle layer (here, photoresist, step 2) to pattern the gold and the underlying layered bulk material as well as to offset the adhesive transfer medium from the bulk, thus permitting transfer of only the patterned regions.

thermal budgets and preclude the use of polymeric substrates, which are highly desirable for flexible electronics and would truly take advantage of 2D materials' inherent flexibility.[9]

Attention has therefore turned to transfer-based assembly methods. Techniques using the surface tension of liquids to maneuver 2D monolayers into position offer limited spatial precision, are prone to wrinkling and folding,[20] and introduce residues at the monolayer−substrate interface.[1] Dry transfer (exfoliation) techniques have harnessed normally applied,[21] shearing,[22] and mixed-mode[23] mechanical stresses to separate material from naturally occurring and synthetic sources. Several of these methods provide some within-layer dimensional precision, but layer thickness selectivity when exfoliating from multilayer sources has often been limited (Supporting Information Figure S1). Yet atomic monolayers are generally essential, e.g., for achieving a direct bandgap in MoS_2.[24,25] What is needed is a technique with precision in all three dimensions, that can handle continuous sheets with lateral dimensions of many tens of micrometers or larger. Such large lateral sheet dimensions are needed for at least two possible purposes: (1) to provide material on which can be created integrated circuits with many submicrometer devices in a predefined spatial arrangement or (2) to define the boundaries of, e.g., powerful individual visible light emitters or sensitive detectors requiring dimensions in the tens of micrometers or larger. Moreover, a process that simultaneously achieves shape selectivity and monolayer selectivity is desirable for forming arrays of heterostructures by enabling the deposition of a patterned monolayer array at the final substrate (which may already have patterned monolayer arrays on its surface).

Recently, the prospects for monolayer exfoliation to be used as a manufacturing process have improved markedly with the discovery that a thin Au film can be used to mediate the single-step exfoliation of large-area monolayers (>10^4 μm^2) from multilayer sources.[26,27] What that work did not achieve was precise control of monolayer shape or position (Figure S1), meaning that one was still required to comb over a target substrate for usable material. Recent work leveraging the same principle has demonstrated the transfer of larger area sheets,[28] though subsequent patterning of material deposited on the substrate is necessary to form devices.

The principles underlying this monolayer selectivity have recently started to be understood.[29,30] Essentially, atomic-scale modeling[30] shows that when a metal is evaporated onto a 2D material crystal, the lattice mismatch between the metal and the 2D material induces a compressive strain in the top layer of the 2D material, weakening the bond between the top and second 2D layers so that a crack preferentially propagates between them when a load is applied (see also Supporting Information section S2). This crucial phenomenon removes the need for atomically precise etching of 2D materials prior to exfoliation of defined shapes of material. It therefore points toward the development of exfoliation-based transfer of patterned vdW monolayer materials.

The manufacturing process that we introduce (Figure 1) uses gold-mediated exfoliation in conjunction with a litho-

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graphically patterned handle layer to transfer arrays of monolayer regions with controlled shape, size, and separation. Our approach delivers a far higher areal density of usable, continuous monolayer material than unpatterned exfoliation[26,27,29] and does so in predictable relative locations so that arrays of devices can subsequently be created in a systematic way.

METHODS

Overview and Novelty. The process for creating patterned monolayers is shown in Figure 1. It makes use of the recently established gold-mediated monolayer-selective exfoliation phenomenon but adds a *pre-exfoliation* patterning stage in which photolithography followed by etching (wet etching of the gold, then plasma etching of the 2D material) defines the edges of regions to be exfoliated. What is particularly new and advantageous about this process is that the etching process *does not need to be atomically precise*: rather, the plasma etch creates crack initiation locations at the edges of the desired regions of material, while the deposition of the metal film ensures that those cracks propagate between the first and second layers of the 2D material. What is also demonstrated for the first time is spatial predetermination of where these regions of material are exfoliated. Making blanket contact between a transfer adhesive and a gold-coated 2D crystal—as in previous reports—does, every so often, produce some very large areas ($>10^4$ μm^2) of monolayer material, but they are ultimately very sparse on the substrate and their locations cannot be predicted. Etching material on the substrate *post-transfer* would not overcome this limitation. Patterning the crystal *before* exfoliation, as we do, initiates cracks that succeed in dictating where material will be exfoliated. Our new method thus generates arrays of monolayer regions with controlled shape and relative position.

Even moderate yield of successfully transferred monolayer regions within such an array is useful because the user of that material no longer needs laboriously to seek individual monolayer regions on which to create devices. Instead, it is simply necessary to image each location in the known array, determine which have yielded monolayer material, and systematically use those locations for devices. These steps can in principle readily be automated and are compatible, for example, with the use of lithography masks carrying large arrays of device electrodes to be superimposed on the transferred 2D material. In this work we show yields of monolayer features above 50% in some transferred arrays (see results, especially Table S3): while not yet nearing semiconductor industry production-level yields, such values are more than enough to accelerate device development greatly compared to the use of unstructured exfoliation.

Moreover, our process itself is rapid compared to state-of-the-art monolayer CVD processes, which require, e.g., 26 h growth[15] even before transfer and patterning. Our process, which results in fully patterned monolayers on a target substrate, requires <10 h before any automation. The most time-costly steps are the evaporation (~45 min is required for vacuum pump-down), the photolithographic patterning (~1 h), and the acetone rinse (4 h). Key aspects of the process design are described below, followed by full, step-by-step details of the process.

Mechanical Design of the Photoresist Handle. A further innovative aspect of the process is that the thickness of the photoresist handle is chosen based on contact mechanics modeling (Supporting Information section S3) so that when thermal-release tape is attached to the top surface of the handle pattern prior to exfoliation, the ~300 kPa pressure needed to trigger adhesion does not deform the tape enough to touch the source material between the features. In this way, exfoliation occurs only within the desired features. The required handle thickness depends on the elastic modulus of the thermal-release tape as well as the geometries of the features to be exfoliated and particularly on their spacing. In the results presented here, arrays of 320 μm × 40 μm features separated by 120 μm are found to need a handle thickness of at least 12 μm, which is readily obtained with spun-on commercial photoresists.

Transfer of Material. After exfoliation from the source, the material is transferred via the thermal release tape to the target substrate (SiO_2 in this work), heat and pressure are applied, the tape and photoresist are stripped away, and the remaining gold is etched. This process ensures that the interface between the exfoliated material and the target substrate remains dry and never touches any other materials. Moreover, the gold layer prevents direct contact between the transferred monolayer and any organic solids. These attributes are expected to minimize heterostructure contamination.

Detailed Process Steps. (1) The multilayer source material (in this work, MoS_2 or WS_2) is prepared. The flattest available sections of material are used. In the case of MoS_2, natural, mined crystals were obtained (eBay) and were manually cleaved to create a flake several millimeters in diameter and a fraction of a millimeter thick. This flake was mounted to a glass slide using double-sided Kapton tape for subsequent processing. Both WS_2 and additional MoS_2 samples were obtained as a multilayer sample fabricated by chemical vapor transport (CVT), ~0.2−0.3 mm thick (HQ Graphene), and used as received. The prepared source material is coated with a 100 nm thick layer of gold by thermal evaporation (Torr International, Inc.).

(2) The source material is coated with AZ 4620 photoresist (PR, MicroChemicals GmbH), which is then patterned (details in Supporting Information section S8).

(3) Without removing the photoresist layer, we etched the exposed gold for 1 min in KI/I_2 (Gold Etchant TFA, Transene Company, Inc.; used undiluted). This step exposes the MoS_2 or WS_2 that is not to be transferred, while the to-be-transferred material remains masked by gold and photoresist. The sample is rinsed in DI water.

(4) The patterned flake is then exposed to a 30 s etch in CF_4 plasma (20 sccm, 100 W, Plasma Equipment Technical Services, Inc.) to remove at least one atomic layer of the MoS_2 or WS_2 from unmasked regions. Initially, a 1 min etch time was used to ensure the removal of at least the top layer;[31] however, the longer etch time was correlated to large amounts of organic residue on the sample and was adjusted down. As an alternative to a plasma etch, an argon ion milling step may be used. Ion milling (Pi Scientific 6 in. system) was conducted using argon ions (5 sccm RF neutral, 15 sccm ion source), with 100 mA beam current, 500 V beam voltage, and 20° incidence angle. The duration of the mill was 7 min, and the pressure was 1.9×10^{-4} Torr. In some cases it was found that the photoresist was easier to remove in step 8 below when ion milling had been used than when the CF_4 etch had been used, possibly because of fluoropolymer deposition onto the photoresist during CF_4 processing. The results shown in this paper, however, were all obtained with CF_4 etching.[a]

(5) Thermal release tape (REVALPHA, Nitto) is brought into contact with the remaining photoresist pattern. Light manual pressure is applied by brushing rubber-tipped tweezers against the back side of the tape, and the tape, loaded now with the pattern, is peeled by hand from the bulk flake.[b]

(6) The silicon wafer target substrate with 260 nm silicon oxide is treated in O_2 plasma for 5 min (120 W, Diener Electronic Nano). It is then placed on a hot plate at 80 °C for at least 5 min, and an IR gun is used to verify it has reached 80 °C.[c] The tape, loaded with the patterned material, is placed onto the heated target substrate, and pressure is applied to the tape/substrate stack for 5 min using a 6.8 kg weight atop a rubber stopper (area: 11 cm^2; thickness: 2.54 cm (1 in.)). The purpose of the rubber is to distribute the load uniformly over the uneven microtopography of the patterned tape's surface. The applied pressure is ~60 kPa.

(7) The target substrate, carrying the loaded tape, is moved to a hot plate at 160 °C to trigger the release of the thermal tape.

(8) The transferred stack is now adhered to the silicon/silicon oxide substrate and is placed in acetone for at least 4 h to remove the photoresist.

(9) The substrate is ashed in O_2 plasma (3 min, 20 sccm, 300 W, Plasma Equipment Technical Services, Inc.) to remove any organic residue on the surface. During the ashing step, the remaining gold layer protects underlying MoS_2 or WS_2 monolayers from damage or removal.

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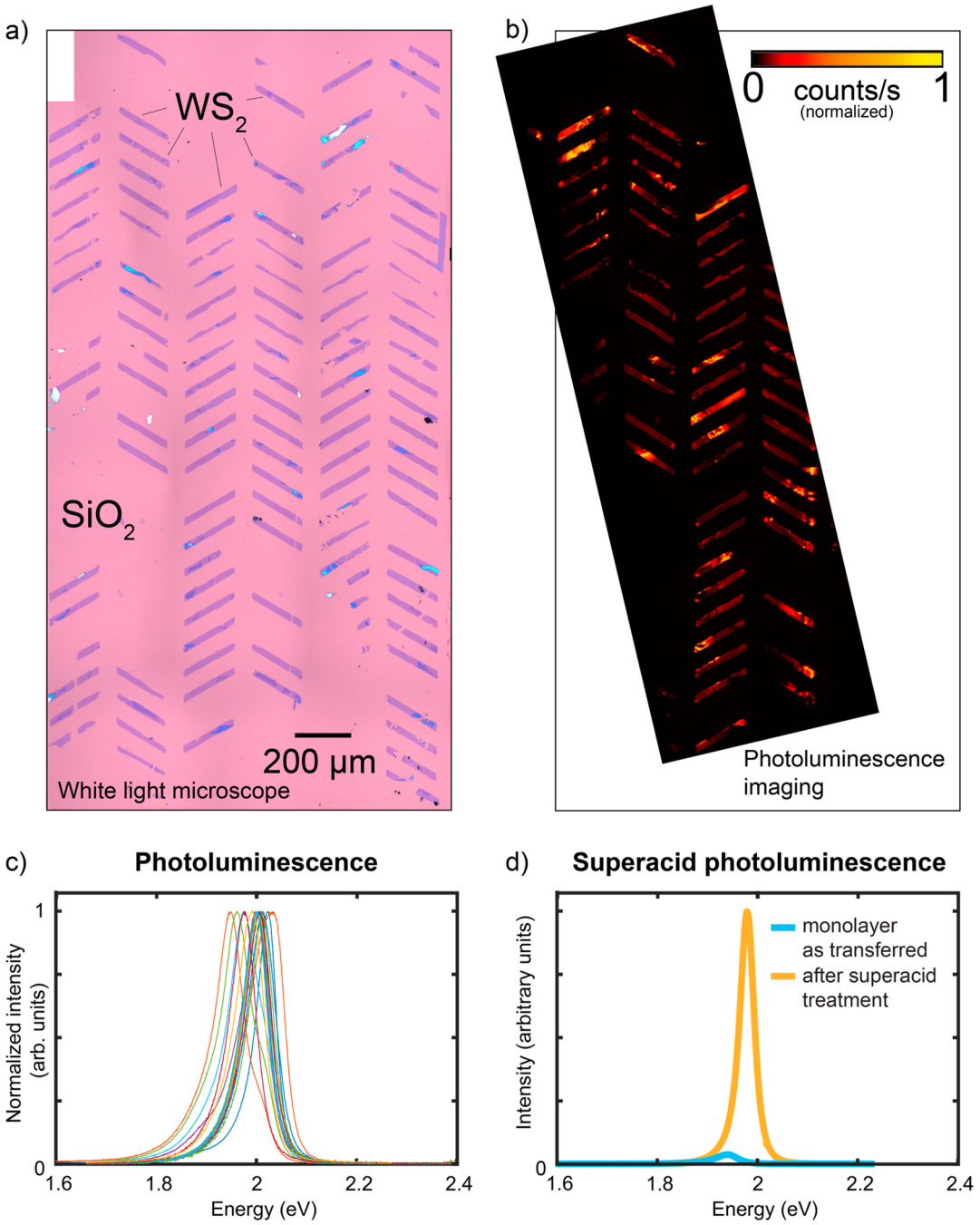

Figure 2. Optical and optoelectronic WS_2 monolayer characterization. (a) White-light reflectance image of a set of transferred WS_2 features on 260 nm thermal SiO_2 on Si. (b) Photoluminescence image of part of the same region as in (a): orientation is the same as (a), and the outline corresponds to that of the region imaged in (a). (c) Photoluminescence spectra from 13 regions of WS_2 on 260 nm thermal SiO_2 on Si, confirming that monolayer WS_2 has been transferred to the substrate. (d) Result of treating a WS_2 monolayer with a superacid, showing more than a 25-fold increase in quantum efficiency.

(10) Finally, the remaining gold is stripped in KI/I_2, and the sample is rinsed in DI water. The result is monolayer TMDC material on the silicon/silicon oxide substrate (Figure S13).

RESULTS AND DISCUSSION

The technique is demonstrated using chemical-vapor-transport-grown bulk WS_2 (Figure 2) as well as mined crystals of naturally occurring MoS_2 (Figure S4) as sources. Results of the transfer process have been examined with optical microscopy, photoluminescence (PL) imaging and spectroscopy, and characterization as a FET channel (all methods in the Supporting Information).

Optical Characterization of Transferred Material. Monolayer regions within an array of $\gtrsim$100 transferred WS_2 features are identified from white-light optical reflection micrographs using well-established optical contrast methods[33,34] (Figure 2a). These micrographs show that features printed using the method are predominantly composed of monolayer material and include substantial continuous monolayer areas. The monolayer nature of these regions is confirmed with PL imaging[24,25] (Figure 2b for WS_2 and Figure

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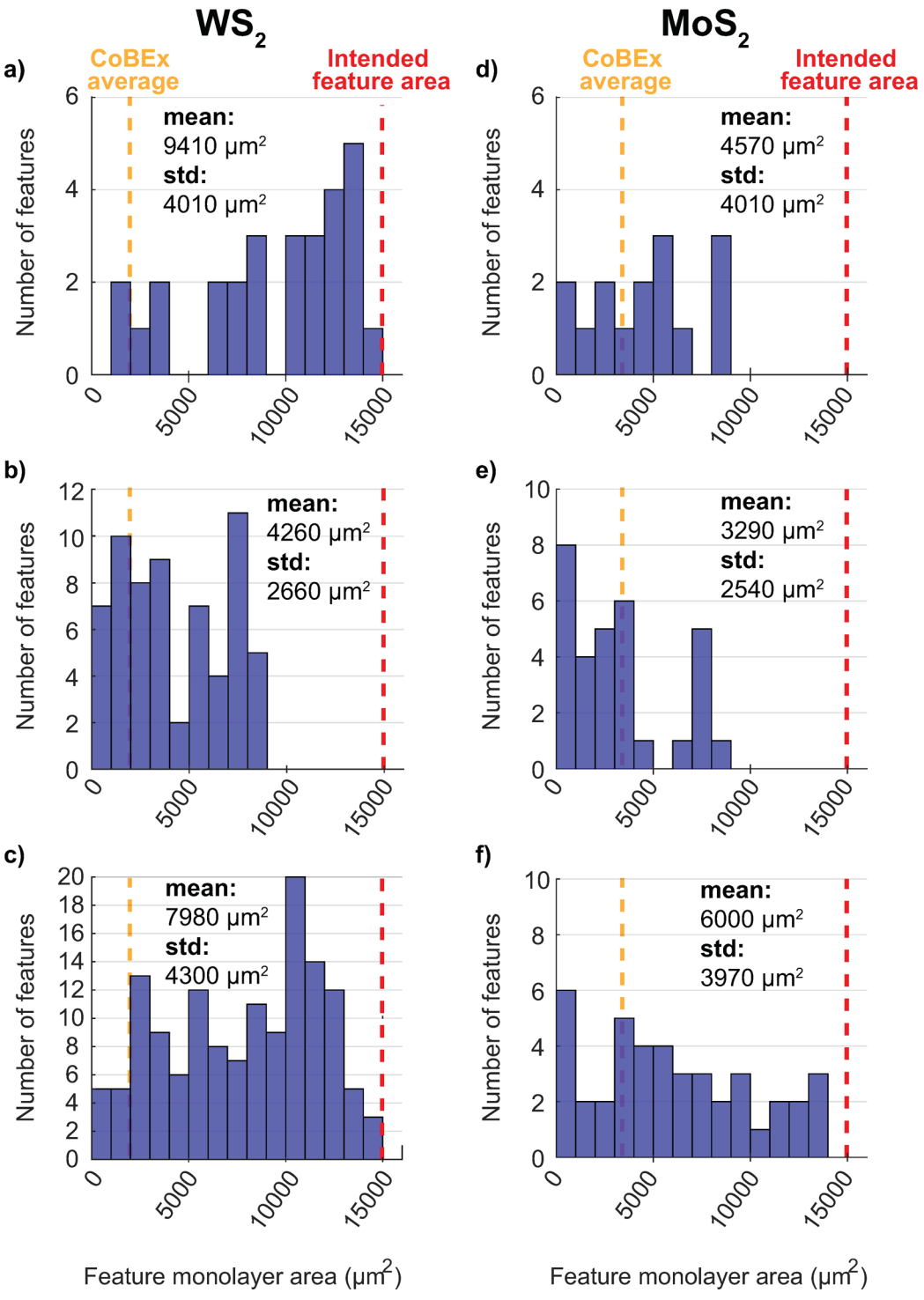

Figure 3. Yield results of the exfoliation method. Histograms (blue bars) showing the distributions of the areas of regions of continuous monolayer material transferred to three separate substrates patterned with WS_2 (a–c) and three substrates patterned with MoS_2 (d–f). Samples were all created using the process flow of Figure 1, with the exfoliated material being the only variable. The red dashed line indicates the area that would be occupied in a pattern by a full, perfect feature; the yellow dashed line shows the average area of continuous material obtained from many samples using the prior, unpatterned, gold-mediated "CoBEx" method.[26]

S4 for MoS_2). While the PL intensity of monolayer regions shows some feature-to-feature and within-feature variation, all regions with appreciable intensity in the PL images indicate monolayer material because the emitted PL intensity of a monolayer is at least 2 orders of magnitude larger than that of bilayer or multilayer material.[24,35] Spatial nonuniformity of PL intensity could be attributable to spatial variation of the density of sulfide vacancies—vacancies which can be repaired by a superacid treatment[26] as we describe below.

Meanwhile, the measured PL peak energies of representative monolayer regions show sample standard deviations of 21 meV for WS_2 (13 measurement locations; Figure 2c) and 6 meV for MoS_2 (10 measurement locations; Figure S4), which may indicate modest spatial variation of the material's environment,

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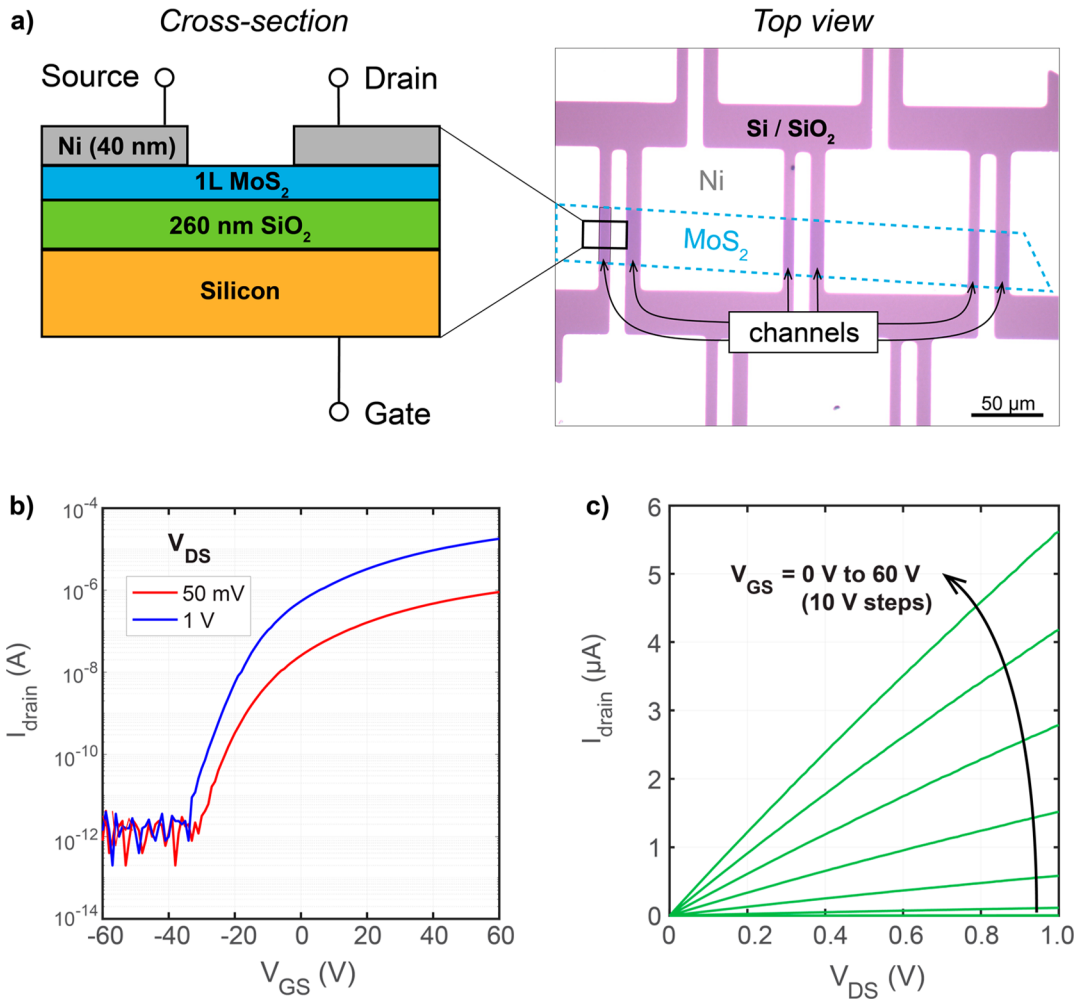

Figure 4. Device characteristics. (a) Cross-section and optical micrograph of six fabricated back-gated MoS_2 transistors with channel width up to 40 μm, defined by the patterning process, and a gate length of 10 μm defined by the Ni contacts. (b) Switching behavior of one of the devices fabricated from transferred monolayer MoS_2 material. (c) Drain current as a function of drain−source voltage.

such as from processing residue, sulfide vacancies, or strain state.[36] Raman spectroscopy (Supporting Information section S5 and Figures S5, S6, and S12) further confirms the single-layer nature of regions that had already been identified as such by both optical reflectance and PL.

Feature and Areal Yield of the Process. Figure 3 shows histograms summarizing the surface areas of regions of continuous monolayer material on three WS_2 and three MoS_2 samples. Details of how the histograms were constructed from optical reflection images are given in Supporting Information section S7. These results show that the process is capable of depositing monolayer sheets of both materials with areas larger than 10^4 μm^2. Moreover, the *average* areas of monolayer sheets are considerably higher than those obtained with unpatterned gold-mediated exfoliation[26] in all but one case (Figure 3e). We further emphasize that each histogram in Figure 3 is obtained from *one single exfoliation process* onto a single substrate, whereas the distributions characterizing unpatterned exfoliation were accumulated from many samples, with material occurring more sparsely over far larger total substrate areas.[26]

We characterize the yield of the process using two metrics: *feature yield* and *areal yield* (details in Supporting Information section S7). Feature yield refers to the number of features actually transferred as a fraction of the total number of desired features in a given area. Areal yield measures the area of monolayer material in a given feature as a fraction of the total intended feature area. Both metrics are potentially relevant for device integration. Areal yield is assessed with a custom image processing routine by determining the areas of any monolayer regions in each feature and dividing the monolayer area by the desired area of the feature. Feature yield ranges up to 67% for WS_2 and up to 54% for MoS_2 (Table S3). Mean areal yields of 63% for WS_2 and 55% for MoS_2 are obtained. While these values remain, of course, below those typical in mainstream semiconductor manufacturing, they represent exceptionally high levels in the current context of exfoliated vdW material processing and can thus accelerate experimental progress in the field by reducing time spent isolating monolayers.

Sources of Yield Loss. We have identified three processing steps that contribute most significantly to yield loss and that would therefore be a reasonable focus of future process development. First, in step 5 (as defined in the section Detailed Process Steps), some of the patterned photoresist handles do not adhere to the thermal release tape and therefore remain on the source crystal. This source of defectivity is evident from optical examination of the thermal release tape between steps 5 and 6, in which gaps are visible in

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the array of features on the tape. Strengthening binding between the PR handles and the adhesive film would help to address this issue, e.g., by applying a partially baked PR layer to the tape.

Second, in some features, the photoresist−gold bond fails during step 5, and the gold and 2D layer therefore remain on the source crystal even when the photoresist feature is transferred to the tape. This source of defectivity is again evident from optical examination of the thermal release tape immediately after step 5, in which some of the photoresist features are visible but without the highly reflective gold layer on them. To address this source of yield loss, adhesion of the photoresist to the gold should be enhanced, potentially by adding an O_2 plasma or hexamethyldisilazane (HMDS) treatment between steps 1 and 2, although this has not yet been tried.

Third, in some locations where gold polygons are visible on the substrate after step 9, optical reflectance imaging after step 10 shows that the MoS_2 or WS_2 is ultimately absent from those same locations. We attribute this component of yield loss to ingress of KI/I_2 liquid between the 2D layer and the substrate during the gold etch of step 10, washing the 2D material off the substrate. This explanation is more plausible than earlier failure of the gold−2D material interface, since that interface is formed during the gold evaporation and is known to be strong because of the Au−S bond. We found that limiting the time that elapses between step 9 (exposing the substrate and its contents to O_2 plasma) and step 10 (gold KI/I_2 processing) to below an hour greatly mitigates this third yield limitation, resulting in the yield values reported above and in Table S3. Nevertheless, further refining this apparently critical plasma treatment step and/or thermally annealing the substrate before the final gold etch may be beneficial in improving the yield of step 10 beyond the values presently reported.

Photoluminenscence Enhancement by Superacid Treatment. Representative samples were further treated in bis(trifluoromethane)sulfonimide (TFSI) superacid (details in Supporting Information section S4) to determine whether this method could improve the quantum yield of the monolayer material, as has been demonstrated previously with unstructured exfoliation.[26] Large observed increases of PL intensity in response to equal illumination after superacid treatment (Figure 2d for WS_2 and Figure S4d for MoS_2) show that indeed the superacid treatment increases the quantum yield at least 25 times in the case of WS_2 and at least 100 times in the case of MoS_2.

Electrical Characterization. Back-gated FETs with gate lengths of 10 μm were defined using photolithographically patterned nickel source and drain electrodes, laid on top of transferred MoS_2 and WS_2 monolayer regions (Figure 4; processing details are in Supporting Information section S6). Devices were then randomly selected for electrical testing from among those whose *entire channel region* had been optically confirmed to consist of monolayer material. In the case of MoS_2, 20 monolayer devices across two substrates were selected for testing; in the case of WS_2, six monolayer devices were sampled from one substrate. The I_D-V_{GS} characteristics of all tested MoS_2 and WS_2 devices are shown in Figures S7 and S8, respectively.

It is notable that all 20 of the 20 tested MoS_2 devices functioned as FETs, exhibiting strong switching behavior with on/off current ratios at V_{DS} = 1 V of between 10^3 and 10^7. Meanwhile, four of the six WS_2 devices tested showed unambiguous switching behavior at V_{DS} = 1 V, with on/off current ratios between ∼200 and 10^4. These results suggest that the transferred material predominantly retains its semiconducting performance and electrical continuity, with the evidence being especially strong for the MoS_2.

Atomic Force Microscopy and Surface Residues. Atomic force microscopy (AFM) measurements of transferred material were also performed (Supporting Information Figures S9−S11 and section S9). While the optical reflection, PL, and Raman measurements described above provide ample robust evidence of the presence of monolayer material, the AFM measurements offer additional information about the topography of transferred material. We see from the AFM topographies that there is some evidence of particle-like residues on both the transferred material and substrate after processing is complete. These residues are ∼5 nm tall, and XPS analysis (Supporting Information section S10 and Figure S11) suggests that they are composed of gold.

Our FET device characterization measurements have confirmed that our test devices, which have 10 μm channel lengths, exhibit strong switching behavior. The residues are therefore evidently sparse enough not to inhibit operation of devices at the 10 μm length scale. Because our XPS analysis of the residue indicates that it is gold, it is conceivable that as devices are scaled down, the residue might provide a current-shorting path, but such behavior has not been observed.

Another potential concern might be that surface residues could inhibit the formation of planar heterostructures requiring atomically spaced layers. To examine this possibility we formed a planar interface between two MoS_2 monolayers that were transferred sequentially using our process followed by thermal annealing (details in Supporting Information section S9 and Figure S12). The Raman spectra measured at multiple locations on this constructed bilayer are consistent with bilayer material—and *not* with two separate monolayers—which indicates that the layers became atomically close after transfer and annealing. Such behavior indicates that whatever residues were on top of the first-deposited MoS_2 layer did not inhibit the formation of intimate contact between it and the second-deposited MoS_2 layer. It is probable that the residues are so sparse that a monolayer of a 2D material can easily conform to them.

The XPS evidence that these residues are gold suggests that they could be removed, if necessary, by modification of the final gold etching step, i.e., step 10 of the process. Extended KI/I_2 acid treatment of the surface, possibly coupled with one or more of mechanical agitation, sonication, and an extended or more vigorous water or solvent rinsing protocol could assist in residue removal. Certainly for the use of this process in combination with traditional silicon electronics, any gold residue would need to be very thoroughly removed, but for novel circuit integration based entirely on 2D materials, it is not yet known how much of an issue Au contamination may be.

■ CONCLUDING REMARKS

What this new processing method essentially achieves is to control where interlayer fracture initiates in vdW solids. It is more effective than simply blanketing the source material with gold because in that case there is no control of where interlayer fracture events will initiate, and we expect that exfoliated material edges would then correspond to naturally occurring steps in the crystal structure. By introducing etched steps in the

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material at the edges of the photoresist handles, we can predetermine, at least to an extent, the locations of fracture.

We expect that a key to increasing yield will be to address the three particular defect-inducing process steps discussed above. An additional likely source of defectivity that cannot be attributed to a specific process step is the intersection of patterned gold regions with natural step changes in the height of the source material. These intersections provide opportunities for patterned handles to contact multiple layers and thereby exfoliate multilayer material. Such intersections could be reduced by maximizing grain size relative to the exfoliated feature size.

This significant step forward in 3D spatial control over exfoliation has been demonstrated here for both MoS_2 and WS_2 and in the future could enable complex integrated circuits to be fabricated more easily from 2D materials. The technique's ability to transfer monolayer sheets with areas $>10^4$ μm^2 makes it particularly appealing for the production of complex heterostructure-based circuits. We have emphasized the capability for large-area transfer although, in principle, there is no impediment to using the technique to transfer arrays of much smaller regions of material, e.g., to define many individual submicrometer transistor geometries prior to exfoliation and transfer. The challenge in that case would be to ensure a high enough feature yield to be able to construct the desired integrated circuit without missing devices. In contrast, higher functional yields may be achieved by transferring arrays of large monolayer sheets, as demonstrated, and then defining, e.g., conductive interconnect patterns to create one or more whole integrated circuits within each successfully transferred large monolayer region.

Although the present process exploits Au−S binding to achieve monolayer selectivity,[37] the basic mechanism, which hinges on a lattice constant mismatch, is expected to be applicable to other material pairs (see Supporting Information section S2), and would be a valuable focus of future studies. Additionally, metal-mediated exfoliation may find itself used in conjunction with other emerging techniques for epitaxy and transfer of thin films[16,17,38,39] to create semiconductor heterostructures.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsaelm.8b00128.

> Handle height calculations; MoS_2 photoluminescence characterization; Raman characterization; AFM topography, friction, and phase maps; XPS characterization; additional electrical characterization; comparison to existing exfoliation methods; and process yield details (PDF)

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H.K.T., J.W.A., D.C.C., and A.J. developed the project. H.M.G., E.M.Y., V.D.N., and H.K.T. conceived of the method and devised processes for deploying the method. H.M.G. performed sample fabrication. J.W.A. and C.M.T. designed the optical characterization scheme, and C.M.T. performed optical characterization and data analysis. S.B.D. fabricated transistors, and H.M.G. measured electrical characteristics. S.B.D. assisted with interpretation of device data. E.C.L. and H.M.G. created monolayer boundary identification code. H.S. performed molecular dynamics simulations. H.M.G., C.M.T., and H.K.T. drafted the manuscript. All authors edited and refined the manuscript.

Notes

The authors declare no competing financial interest.

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■ ADDITIONAL NOTES

[a]Although the etching or ion milling process does change the topography of the source material left behind after exfoliation, the source crystal can be reused, if there are enough layers remaining, by doing a blanket exfoliation with unpatterned thermal release tape to recover a close-to-flat surface.

[b]If a transparent transfer medium were chosen, such as the elastomer polydimethylsiloxane (PDMS), the technique would be compatible with optical alignment methods which would allow placement of sheets in controlled positions on a target.

[c]The use of oxygen plasma and elevated temperature has previously been shown[32] to enhance adhesion of exfoliated 2D materials to SiO_x and thereby greatly increase the transferred area of material, albeit, in that work, without control of shape or position.

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