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Letter

Ga_2O_3 metal-oxide-semiconductor field effect transistors on sapphire substrate by MOCVD

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Abstract

Si-doped gallium oxide (Ga_2O_3) thin films were grown on a c-plane sapphire substrate by metalorganic chemical vapor deposition (MOCVD) and fabricated into metal oxide semiconductor field effect transistors (MOSFETs). The Ga_2O_3 MOSFETs exhibited effective gate modulation of the drain current with a complete channel pinch-off for $V_G < -25$ V, and the three-terminal off-state breakdown voltage was 390 V. The device shows a very low gate leakage current ($\sim$50 pA mm^{-1}), which led to a high on/off ratio of $\sim 10^8$. These transistor characteristics were stable from room temperature to 250 °C.

Keywords: gallium oxide, MOCVD, MOSFET

(Some figures may appear in colour only in the online journal)

1. Introduction

Gallium oxide (Ga_2O_3) materials are an excellent candidate to replace SiC or GaN materials for high power electronic applications due to their high breakdown field, which can be predicted from their wide bandgap [1]. Ga_2O_3 has several polymorphs such as α-, β-, γ-, δ-, ε- and κ- phase. Recent research trends have shown that α- and β-phase Ga_2O_3 have been the most studied for power electronic devices [2]. Particularly, since the β-phase has become easier to access due to the availability of native substrate, research on the fabrication of the power device using the β-Ga_2O_3 has been rapidly developed. So far, β-Ga_2O_3 has been reported for molecular beam epitaxy (MBE) grown metal semiconductor field effect transistors (MESFET) on β-Ga_2O_3 substrate, metal oxide semiconductor field effect transistors (MOSFET) in depletion mode and normally off MOSFET using Si ion implantation [1, 3, 4]. Native Ga_2O_3 substrates showed very good transistor characteristics and stable operation behavior at temperatures as high as 250 °C [5]. Furthermore, various structures of power application devices such as a vertical type MOSFET and fin-array field effect transistors (finFETs) have been continuously reported [6, 7]. Another approach is to report on the power electronic devices of α-Ga_2O_3 grown on a sapphire substrate by mist chemical vapor deposition (CVD) and halide vapor phase epitaxy (HVPE), which can provide a low cost and a large area [8, 9]. Heteroepitaxially grown α-Ga_2O_3 has been fabricated into a variety of power devices, from Schottky diodes to MESFETs, and some devices have reached mass production [10–12]. This heteroepitaxial growth makes it possible to use the amazing potential of Ga_2O_3 so rapidly. However, α-Ga_2O_3 has a phase transition issue at higher temperatures [13–15]. As far as we know, there are no cases of fabricating MOSFETs for practical applications using metalorganic chemical vapor deposition (MOCVD) to grow thermally stable κ-Ga_2O_3 thin film on sapphire substrate. In this study, we fabricated and evaluated $\sim$150 nm thick *n*-type Ga_2O_3:Si thin film MOSFETs grown by MOCVD on c-plane sapphire substrate as an approach to solve these phase transition issues. The fabricated devices exhibited superior performance compared to other MOSFETs fabricated from Ga_2O_3 grown on sapphire substrate by MOCVD [16, 17]. It

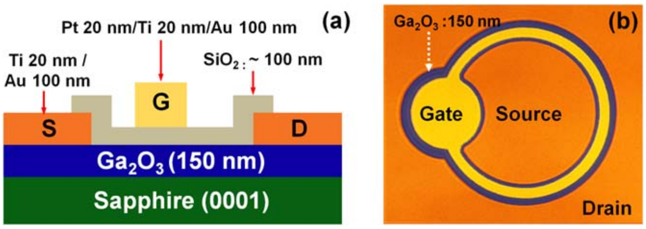

Figure 1. Schematic illustration of the (a) cross section and (b) plan view of the circular Ga_2O_3:Si MOSFET design.

was also stable from room temperature (RT) to 250 °C. This device demonstrates the possibilities of thermally stable, low cost and high scalable *n*-type Ga_2O_3 thin films MOSFET directly grown on a sapphire substrate by MOCVD for power electronics applications.

2. Experimental procedure

2.1. Material growth

A commercial horizontal-flow MOCVD reactor (AIXTRON 200/4 RF) was used to grow *n*-type ∼150 nm thick Ga_2O_3:Si thin films on c-plane sapphire at a growth temperature of 670 °C under H_2 carrier gas using a conventional trimethylgallium (TMGa) bubbler and high purity deionized water as the gallium and oxygen precursors, respectively. SiH_4 gas was used as a dopant for *n*-type doping. The growth pressure was 50 mbar and the VI/III ratio was 324; the growth rate was 10 nm min^{-1}. The Ga_2O_3:Si thin films were n-type with Hall measurement showing a carrier concentration of 2×10^{18} and a low mobility of around 1 $cm^2 V^{-1} \cdot s^{-1}$. After growth, the surface morphology and crystalline structure of the Ga_2O_3 thin films was studied using scanning electron microscopy (SEM) and x-ray diffraction (XRD) systems, respectively.

2.2. Fabrication procedure of circular Ga_2O_3:Si MOSFET

To evaluate the MOSFET performance of the *n*-type Ga_2O_3:Si, first we fabricated a simple circular type MOSFET. Figures 1(a) and (b) show a schematic illustration of the circular Ga_2O_3:Si MOSFET design. Ti/Au (20/100 nm) was e-beam evaporated to form the metal contacts for the source and drain electrodes. The source and drain metal contacts show ohmic behavior without additional annealing. The 100 nm SiO_2 dielectric layer was formed by plasma-enhanced chemical vapor deposition (PECVD) at 350 °C. Finally, the Pt(20 nm)/Ti(20 nm)/Au(100 nm) gate electrode was e-beam evaporated on the SiO_2 layer. The gate length was 15 μm, the spacing between the source/drain was 30 μm, and the diameter of the inside source circular pad was 100 μm.

2.3. Fabrication procedure of square type Ga_2O_3:Si MOSFET

In order to isolate the devices, the Ga_2O_3:Si thin film was first patterned into 200 μm wide stripes via conventional lithography and electron cyclotron resonance reactive ion etching (ECR-RIE) using CF_4. The subsequent fabrication steps were the same as for the circular design, but used the layout shown in figure 2(a). Figure 2(b) shows a false-color optical microscope image of square type Ga_2O_3:Si MOSFETs. The MOSFETs has a gate length of 10 μm (L_G), a gate-source spacing of 10 μm (L_{GS}) and a gate-drain spacing of 20 μm (L_{GD}).

2.4. Device measurement

Then both fabricated circular and square type MOSFETs were tested using a semiconductor parameter analyzer and probe station. Additionally, the temperature dependent operating behavior of square type Ga_2O_3:Si MOSFET was evaluated using the probe station with a thermal stage.

3. Results and discussions

Figure 3(a) shows a tilted view SEM image of the *n*-type Ga_2O_3:Si thin films on c-plane sapphire substrate grown at 670 °C. As can be seen in figure 3(a), the *n*-type Ga_2O_3:Si thin film was uniformly grown on the sapphire substrate without any cracks. Inset shows a cross-sectional SEM image of ∼150 nm thick *n*-type Ga_2O_3:Si thin film. The growth rate was 10 nm min^{-1}. Figure 3(b) shows an AFM image of the as-grown *n*-type Ga_2O_3:Si thin film. The as-grown *n*-type Ga_2O_3:Si thin film presents as an aggregate of 1 to 2 μm grains, with a root-mean-squared (RMS) roughness of 3.0 nm. We have previously studied our films via transmission electron microscopy (TEM) and reported them to be κ-Ga_2O_3 after investigating the relationship between the film and c-plane sapphire substrates at the atomic level [18]. κ-Ga_2O_3, is an analog of orthorhombic κ-Al_2O_3 with the space group of $Pna2_1$. XRD omega/2theta scans of the *n*-type Ga_2O_3:Si thin film on c-plane sapphire are shown in figure 3(b). Three sharp peaks are located at ∼9.5°, ∼19.4° and ∼29.9°, consistent with the (002), (004), and (006) peaks, respectively, of κ-Ga_2O_3. . In addition, to investigate the thermal stability of the grown Ga_2O_3:Si, annealing was performed under and N_2 and water vapor atmosphere at 900 °C for 20 min. Figure 3(c) shows the omega XRD data before and after annealing. Despite the high annealing temperature, no phase transition to the generally known β-phase occurred. Only a slight increase in the XRD intensity was observed after annealing, with this increase being attributed to reduction of oxygen vacancies and improved local crystallinity after annealing in the N_2 and water vapor ambient. And the FWHM value increased from slightly 808 to 927 arcsec, but no change was observed in the surface of Ga_2O_3:Si thin films after annealing. This suggest the crystal structure of our *n*-type Ga_2O_3:Si thin film is stable even at a high temperature.

Figure 4(a) shows the DC output I-V (I_D-V_{DS}) characteristics of the circular Ga_2O_3:Si MOSFET at gate voltages (V_G) from 10 to −40 V in steps of −5 V while the V_{DS} was swept from 0 to 100 V. The I_D is effectively modulated by the V_G with good saturation and sharp pinch-off characteristics. A maximum I_D of 26.7 mA mm^{-1} is obtained for V_G = 10 V and the three-terminal breakdown voltage (V_{br}) at the off state

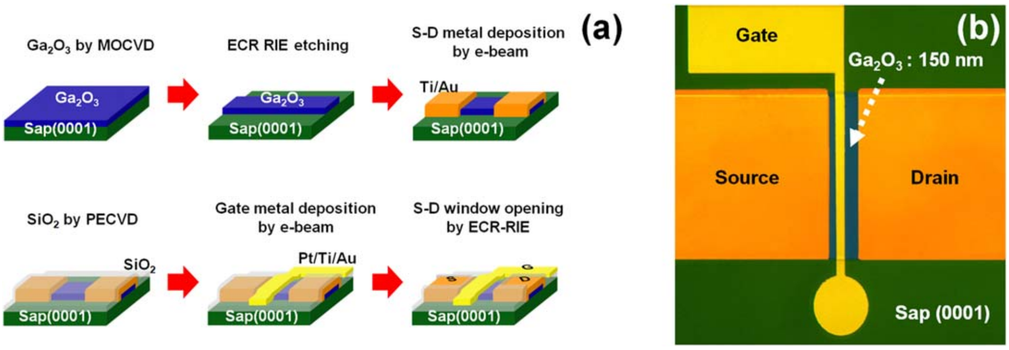

Figure 2. (a) Fabrication process for square type Ga_2O_3:Si MOSFETs and (b) optical microscope image of square type Ga_2O_3:Si MOSFETs.

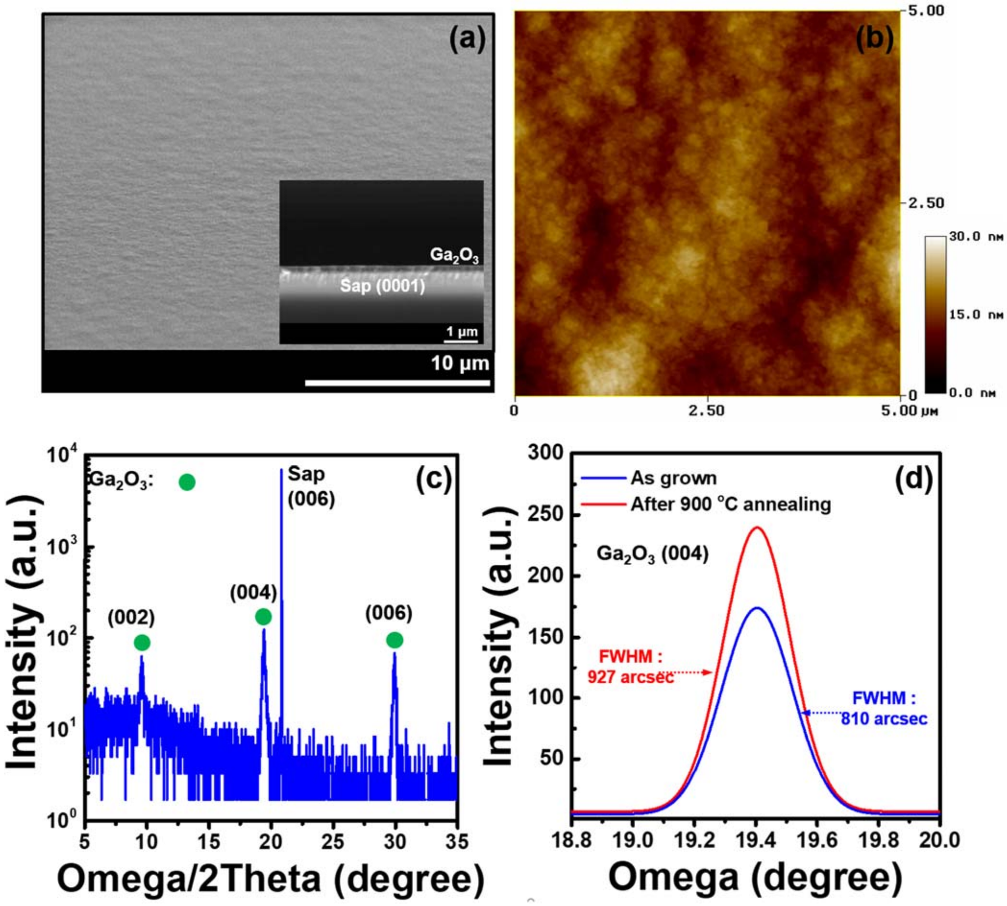

Figure 3. (a) Tilted view SEM image (Inset shows a cross-sectional SEM image), (b) AFM image and (c) XRD pattern of Ga_2O_3:Si thin films grown on c-plane sapphire substrate; (d) omega XRD of as-grown and after annealing Ga_2O_3:Si thin films.

is as high as 360 V at $V_G = -30$ V. Figure 4(b) shows the transfer characteristics at a V_{DS} of 100 V. The device exhibits depletion mode operation, and the I_D on/off ratio is over 10^7. The characteristics of this Ga_2O_3:Si MOSFET fabricated on c-plane sapphire substrate are comparable to previously reported β-Ga_2O_3 transistors using β-Ga_2O_3 homo-substrate [1, 4, 5, 19, 20].

We also investigated the characteristics of the square type Ga_2O_3:Si MOSFETs. Figure 5(a) shows the DC output I-V (I_D-V_{DS}) characteristics of the square type Ga_2O_3:Si MOSFET at gate voltages (V_G) from 10 to -40 V in steps of -5 V while the V_{DS} was swept from 0 to 100 V at RT. The I_D is effectively modulated by the V_G with good saturation and sharp pinch-off characteristics. A maximum I_D of $9.12\ \mathrm{mA\ mm^{-1}}$ is obtained for $V_G = 10$ V and the three-terminal breakdown voltage (V_{br}) at the off state is as high as 390 V at $V_G = -30$ V. Figure 5(b) shows the transfer characteristics at a V_{DS} of 100 V. The device exhibits depletion mode operation and the device shows a very low gate leakage current of 50 $\mathrm{pA\ mm^{-1}}$, which leads to a high on/off ratio of $\sim 10^8$. The maximum transconductance was $0.8\ \mathrm{mS\ mm^{-1}}$. A field-effect mobility of $2.43\ \mathrm{cm^2\ V^{-1} \cdot s^{-1}}$ was extracted from the transfer characteristics of the square type Ga_2O_3:Si MOSFET and a sub-threshold slope (SS) of

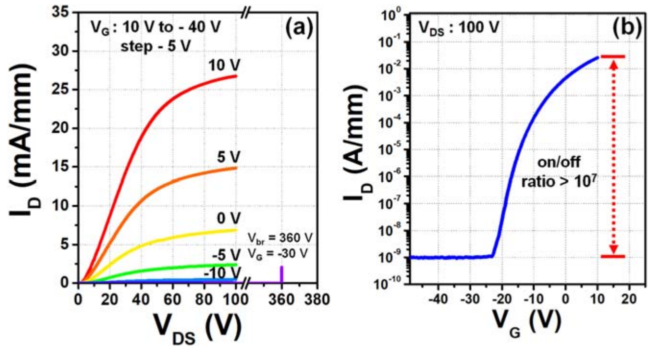

Figure 4. (a) DC I–V characteristics and (b) transfer characteristics of circular Ga_2O_3:Si MOSFET measured at RT.

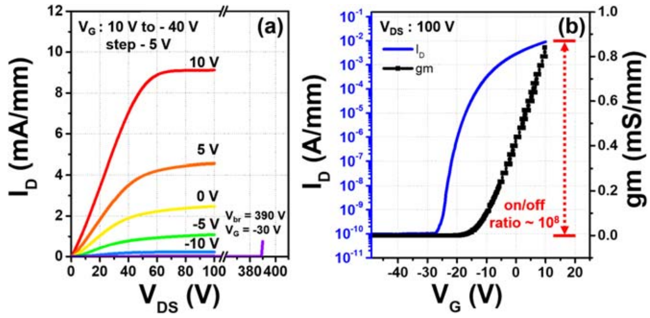

Figure 5. (a) DC I–V characteristics and (b) transfer characteristics of square type Ga_2O_3:Si MOSFET measured at RT.

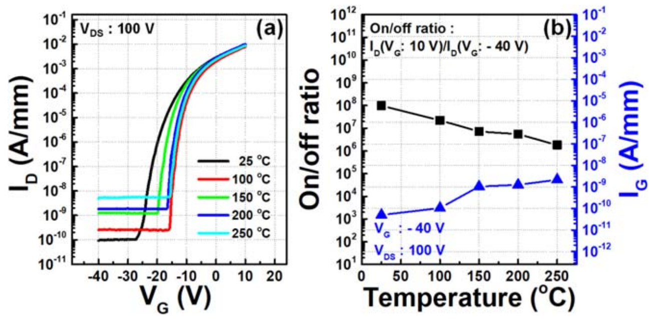

Figure 6. (a) Transfer characteristics of square type Ga_2O_3:Si MOSFET with V_{DS} 100 V and (b) on/off ratios and I_G as a function of operating temperature.

1.12 V/dec was calculated. These circular and square MOSFETs results suggest that not only have practical Ga_2O_3 MOSFETs have been fabricated, but also that Ga_2O_3:Si thin films grown on c-plane sapphire substrate by MOCVD have great potential for future power devices.

We investigated the performance of the square Ga_2O_3:Si MOSFETs at various operating temperatures ranging from RT to 250 °C in air condition using semiconductor parameter analyzer with a thermal stage. No significant degradation of the device surface was apparent after operating at the elevated temperatures figure 6(a) shows the temperature dependent transfer characteristics at V_{DS} of 100 V. The maximum I_D improved with increasing operating temperature and no significant change in the V_G required for pinch-off was observed. The on/off ratio in figure 6(b), defined as the I_D at $V_G = 10$ V divided by the I_D at $V_G = -40$ V. The I_D on/off ratios slightly decreased by increasing the I_G according to the operating temperature; however, the devices maintained the high on/off ratio even at 250 °C. The maximum I_D was maintained even after thermal cycling the device 10 times from 250 °C to RT, and it was observed that the on/off ratio of $\sim 10^8$ at RT was recovered. Temperature dependent operating performance of the circular device also showed similar behavior. All results indicate that MOSFETs fabricated from Ga_2O_3:Si grown by MOCVD on c-plane sapphire are air-stable even after the repeated high temperature measurements; this is the outstanding performance MOCVD grown Ga_2O_3 MOSFET on sapphire [16, 17].

4. Conclusion

We have demonstrated high-performance circular and square MOSFETs from Ga_2O_3:Si grown on c-place sapphire by MOCVD. The circular and square MOSFET devices showed maximum I_D of 26.7 mA mm^{-1} and 9.12 mA mm^{-1} with excellent breakdown voltages of 360 V and 390 V, respectively. And both devices exhibited high on/off ratios of over 10^7 to 10^8. Moreover, the device operated well up to at 250 °C with no significant degradation. In conclusion, MOSFETs fabricated from Ga_2O_3:Si grown by MOCVD on c-plane sapphire demonstrate the remarkable potential for Ga_2O_3 to be applied for next generation for power electronics applications.

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