Soft-FET: Phase transition material assisted **Soft** switching **F**ield **E**ffect **T**ransistor for supply voltage droop mitigation

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***Abstract*—Phase Transition Material (PTM) assisted novel soft switching transistor architecture named "Soft-FET" is proposed for supply voltage droop mitigation. By utilizing the abrupt phase transition mechanism in PTMs, the proposed Soft-FET achieves soft switching of the gate input of a logic gate resulting in reduced peak switching current as well as steep current variations (di/dt). In addition, the Soft-FET incurs lower delay penalty across a wide voltage range compared to various baseline Complementary Metal Oxide Semiconductor (CMOS) logic gate variants for the same peak current. We perform a detailed PTM parameter optimization for optimum Soft-FET performance. Soft-FETs when used as power gates achieve ~20mV lower supply droop and when used as an I/O buffer achieves 46% lower ground bounce with 8.8% improved energy efficiency.**

Keywords— Phase transition materials; Soft switching; Soft-FET; Voltage droop, power gate, I/O buffer

I. INTRODUCTION

With the rapid advances in computing systems spanning from billions of IoTs (Internet of Things) to high performance exascale supercomputers, energy efficient design is an absolute must [1]. In a modern System-on-a chip (SoC) design, supply voltage (V_{CC}) scaling is the primary driver to reduce the energy consumption [2]. The IR drop and package inductance in a power delivery network (PDN) causes large voltage droops due to peak switching currents as well as sudden changes in current activity (di/dt) as shown in Fig. 1 [3]. This voltage droop magnitude attributes to a significant portion of the supply voltage specifications. Furthermore, the deep proliferation of fine grain power domains and their complex power management strategies result in freqeunt Dynamic Voltage and Frequency Scaling (DVFS) [4]. This aggravates the voltage droop magnitude and translates into tighter specifications for the power delivery network, bulkier motherboard regulator components and ultimately degrading energy efficiency [5]. Therefore, there is a critical need to develop circuit topologies to reduce the peak switching current as well as sudden current fluctuations (di/dt) to reduce the voltage droops and to realize compact and efficient power delivery network. To this effect, many circuit topologies have been proposed to reduce the peak swithing current at the expense of larger delay and larger area [6-7].

In this paper, we propose a novel soft-switching transistor architecture abbreviated as "Soft-FET" utilizing abrupt phase change mechanism in transition metal oxides. To the best of author's knowledge, this is the first ever application of phase transition materials in power delivery using Soft-FETs for supply voltage droop reduction. The key contributions of this paper are as follows:

1. We propose a novel integration of the PTM onto the gate of baseline CMOS for soft switching named as "Soft-FET".
2. We analyze the DC and transient characteristics of the proposed Soft-FET based inverter and compare with multiple variants of the baseline CMOS inverter and quantify the effectiveness of the Soft-FET in reducing the peak current and/or di/dt.

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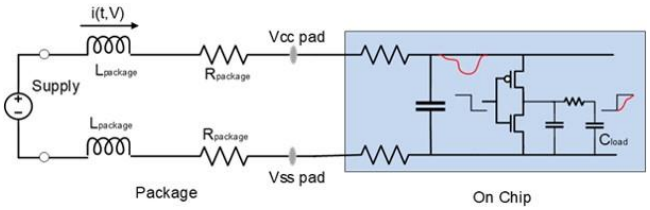


Fig. 1 Supply voltage droop in a power delivery network

3. We perform a detailed PTM device parameters variations and analyze their sensitivity to the Soft-FET peak current, and/or di/dt reduction.
4. We show the relationship between the PTM switching time and the input slew rate for optimum soft switching.
5. We present two case studies with Soft-FET power-gates and Soft-FET I/O buffer drivers and quantify the reduction in the peak switching current, supply and ground bounce.

The rest of the paper is organized as follows. In Section II, we describe the principle of operation of Phase Transition Material and the proposed Soft-FET. Section III compares the proposed Soft-FET based inverter with other CMOS variants. Section IV presents the PTM device optimization for best soft-switching benefits. Section V discusses the Soft-FET applications in power gates and I/O buffers. Section VI concludes the paper summarizing the proposed Soft-FET benefits and its effectiveness in power delivery networks.

II. PHASE TRANSITION MATERIAL AND SOFT-FET

A. Phase Transition Materials (PTM)

Transition metal oxides (such as Vanadium Dioxide (VO_2) or Niobium Dioxide (NbO_2)) exhibit abrupt insulator-metal transition on the application of external electric field [8, 9]. This unique property is currently being utilized to realize transformational circuit topologies [10-14]. Table 1 illustrates the earlier proposed applications of PTM for logic and memory applications.

For logic applications, the PTM when placed in series with the source terminal of a MOSFET (called as Hyper-FET) reduces the sub-threshold current thereby improving the I_{ON}/I_{OFF} ratio [10, 11]. Another application of PTM is a metal- insulator tunnel junction with abrupt phase transition for potential applications in TFET (Tunnel Field Effect Transistors) design [12]. For memory applications, the

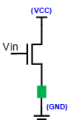
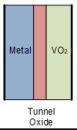
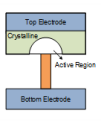
	Logic		Memory	
	Hyper-FET	**MTJ**	**PCM**	**Selector Switch**
Structure				
Key Mechanism	Resistivity difference between insulating and metallic phases	Bandgap difference between insulating and metallic phases	Resistivity difference between Crystalline and amorphous	Resistivity difference between insulating and metallic phases
Benefits	Steep Sub-threshold swing	Efficient control over tunneling	Dense reliable non-volatile memory	Reduced sneak path current

Table 1: Qualitative comparison of PTM applications

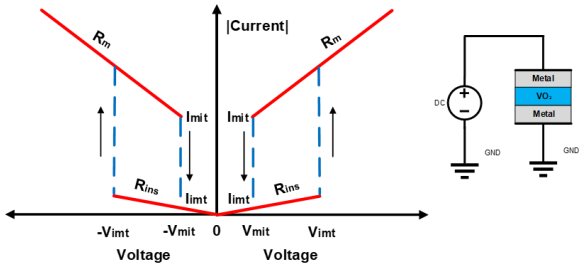


Fig. 2 Phase Transition Material: I-V characteristics

phase transition materials have been known and used extensively in Phase Change Memory (PCM) designs [13]. The resistivity difference between the crystalline and amorphous states of the material has been exploited to store the information. Recently, VO_2 based MIM (Metal-Insulator-Metal) PTM device has been shown to exhibit excellent behavior as the selector switch for the crossbar memory arrays [14]. The VO_2 MIM selector device significantly reduces the crossbar sneak path current due to its superior R_{OFF}/R_{ON} ratio and can operate at a lower voltage compared to other crossbar selector switch candidates [14].

The application of voltage bias across the two-terminal device with PTM sandwiched between metal electrodes exhibits the I-V characteristics as shown Fig. 2. Under no bias condition, PTM behaves like a resistor with resistance R_{INS} (insulator), typically in the range of few Mega-ohms (MΩ). As the voltage bias increases, current ($I=V/R_{INS}$) flows through the device. When this current (I) reaches a threshold (I_{IMT}), abrupt phase transition takes place from insulating phase to the metallic phase and the resistance drops to very low value (R_{MET}), typically in the range of few kilo-ohms (KΩ). The device continues to stay in the metallic phase (R_{MET}) for any further increase in the voltage bias. The two terminal PTM device exhibits hysteresis behavior with respect to voltage bias (Fig. 2) Reducing the voltage bias, reduces the current ($I=V/R_{MET}$) in the circuit. When the current reaches a lower threshold value (I_{MIT}), again a phase transition takes place and the resistance of the device increases back to R_{INS}. The voltage corresponding to insulating-to-metallic transition is referred as V_{IMT} ($V_{IMT} = I_{IMT}*R_{INS}$) and the voltage corresponding to metallic-to-insulating transition is referred as V_{MIT} ($V_{MIT} = I_{MIT}*R_{MET}$).

B. Soft-FET principle of operation

The two terminal PTM device when placed in series with a capacitor as shown in the Fig. 3 exhibits a unique transient behavior of the circuit. Under no voltage bias ($V_{IN}=0$), the PTM is in insulating phase with resistance (R_{PTM}) equal to R_{INS}. The transient behavior can be understood by approximating the gate of MOSFET to a capacitor as shown in Fig.3. As the voltage V_{IN} increases, the current starts charging the capacitor with a large time constant ($R_{INS}*C$) leading to slow charging of the capacitor. Thus, the V_C node voltage rises slowly (lateral portion of the staircase V_C waveform in Fig. 3) in comparison to the V_{IN} node voltage resulting in increasing voltage difference (V_{IN}-V_C) across the PTM. When this voltage difference (V_{IN}-V_C) reaches the V_{IMT}, abrupt phase transition from insulating to

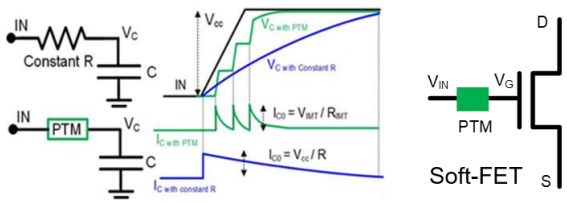


Fig. 3 Soft charging using phase transition materials

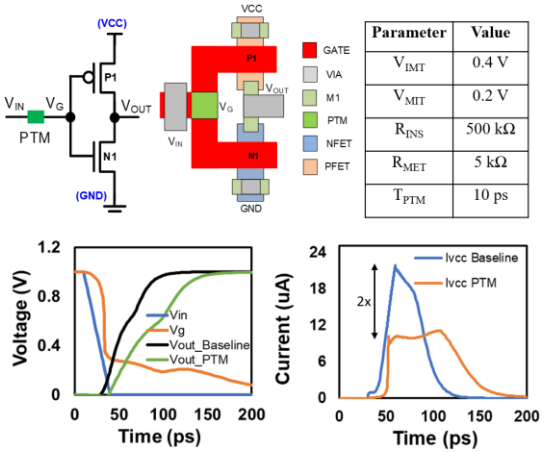


Fig. 4 Soft-FET based inverter schematics and layout; PTM device parameters; transient voltage and current waveforms

metallic phase takes place. This phase transition is accompanied by a large current flow due to transition from large insulating state resistance (R_{INS}) to a low metallic state resistance (R_{MET}) of the PTM. In the metallic phase the capacitor charges quickly owing to small time constant ($R_{MET} * C$) causing the V_C node voltage to rise steeply (vertical portion of the staircase V_C waveform in Fig. 3). Consequently, when the voltage across the PTM (V_{IN}-V_C) drops below the V_{MIT} threshold, phase transition from metallic to insulating state occurs. Again, the slow charging of the V_C node eventually leads to phase transition to the metallic phase. This cycle is repeated until steady state of the circuit is attained ($V_{IN}=V_{CC}$). With V_{IN} node at constant voltage (V_{CC}) and the V_C node charging slowly (insulating phase), the voltage difference (V_{IN}-V_C) reduces steadily leading to no further transitions. Thus, the V_C node slowly raises with $R_{INS}*C$ time constant and finally reaches the V_{IN} at a later time instant as evident from Fig.3. Notice that, during the metallic phase, PTM conducts large capacitor charging current. When compared with the constant R charging with a uniform RC time constant scenario, the PTM device exhibits stepwise capacitor charging. A similar sequence of events can be observed when the V_{IN} node voltage ramps down and exhibiting downward staircase waveform across the capacitor.

C. Soft-FET

The gradual charging of a capacitor explained in the previous subsection is central to the notion of Soft-FET transistor. Series connected PTM device at the gate terminal of a baseline MOSFET causes the gate voltage (V_G) to rise slowly compared to the input voltage (V_{IN}) leading to soft-switching operation. Hence, the proposed transistor architecture is abbreviated as "Soft-FET" to reflect its soft-transition mechanism.

III. SOFT-FET LOGIC APPLICATIONS

A. Soft-FET based inverter DC characteristics

The concept of soft (slow) charging the capacitor with the aid of a PTM can be utilized to reduce the peak switching current drawn by the logic circuits from the Vcc voltage rail. In this section, we present the analysis for the specific case of Soft-FET based inverter. As shown in Fig.4, the Soft-FET inverter is realized by placing the PTM in series with the common gate terminal of pull-up (P_1) and pull-down (N_1) transistors. The PTM layout can be envisioned as a 'special via' contact at the gate input and would not incur any area penalty for standard logic cell layouts. The DC characteristics of the inverter such as noise margin and dc output level are unperturbed by the presence of the PTM. This is unlike the earlier proposed Hyper-FET which results in slight DC noise margin degradation due to presence of insulating state PTM in its output

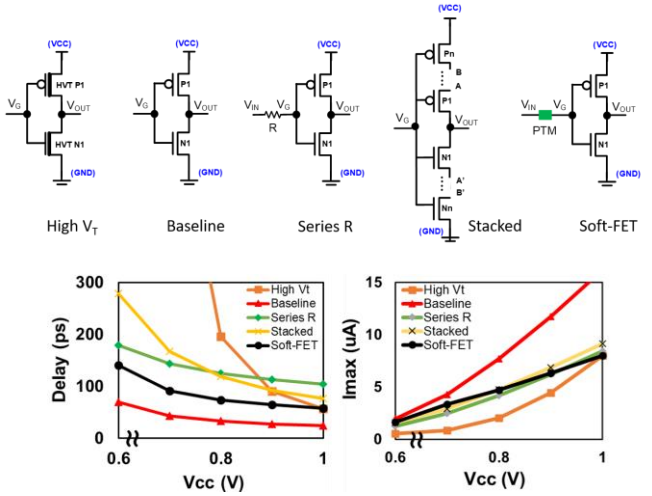


Fig. 5 Comparison of Soft-FET with various CMOS topologies for peak switching current reduction

series path. Absence of series resistance doesn't degrade Soft-FET DC ON current compared to the baseline MOSFET. However, the proposed Soft-FET doesn't reduce sub-threshold leakage current as observed in the Hyper-FET which leads to better I_{ON}/I_{OFF} ratio. The PTM device only modulates the charging/discharging of the input gate capacitor without affecting the dc behavior of the underlying MOSFET. The voltage dependent abrupt resistance change in PTMs rapidly changes the RC time constant at the gate input resulting in a soft switching transistor behavior.

B. Soft-FET based inverter transient characteristics

The Soft-FET inverter transient behavior is strongly governed by the PTM device parameters which modulates the staircase capacitor charging behavior. As the input supply voltage (V_{IN}) rises/falls, the gate of the inverter (V_G) experiences a slow rise/fall in voltage. This variation in the gate voltage modulates the current drawn from the V_{CC} rail and the current sunk into the ground. Fig. 4 describes a detailed description for the current dynamics during the falling transition of the Soft-FET inverter. SPICE simulations are performed using 40nm commercial CMOS process transistor models and a Verilog-A PTM model [15]. The PTM device parameters listed in Fig. 4 are based on the experimental VO_2 demonstrations [11] [16]. As the supply voltage (V_{IN}) starts ramping down, the PTM in insulating phase causes the slow discharge of the gate voltage (V_G) due to the large (R_{INS}*C) time constant. So, the gate voltage (V_G) stays close to V_{CC} forcing the PMOS P_1 to remain turned off resulting in a very low current being drawn from the V_{CC} rail. The increasing voltage difference (V_G-V_{IN}) when reaches V_{IMT} induces a phase transition to metallic phase. Following this transition, the gate voltage (V_G) drops below the threshold voltage (V_{TP}) and turns the P_1 transistor ON. During the metallic phase, the current drawn from the V_{CC} rail starts increasing. Note that unlike baseline CMOS, the current waveform of the Soft-FET inverter is shifted in time depending on input slew rate and the phase transition switching time. Also, in the metallic phase V_G reduces steeply and attempts to approach V_{IN} resulting in a decreasing (V_G-V_{IN}). A reverse phase transition to insulating phase occurs when the voltage across the PTM (V_G-V_{IN}) reduces below V_{MIT}. In the insulating phase, the slow discharge of V_G and corresponding slow increase in the output voltage (V_{OUT}) results in almost constant current being drawn from the V_{CC} rail. Note that the peak switching current is significantly reduced compared to the baseline CMOS due to the weak turn on of the PMOS (P_1) transistor. This implies that the PMOS transistor is weakly turned on for a longer duration exhibiting a smooth current waveform which results in reduced di/dt. Similarly, the input voltage

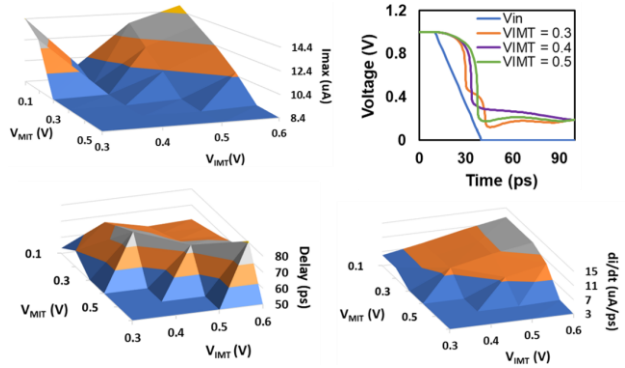


Fig. 6 Variation of I_{MAX}, di/dt and delay with the PTM device parameters V_{IMT} and V_{MIT}

ramp results in weak turn on of the NMOS transistor (N_1) lowering the current sunk into to the ground. Thus, the Soft-FET based logic circuits can exhibit reduced peak switching current and lower di/dt compared to baseline design.

C. Comparison with other peak current reduction techniques

The peak switching current and di/dt in the proposed Soft-FET is achieved using novel material properties. The same effect can also be achieved through multiple variants of baseline CMOS technology using additional transistors and/or passive resistors. It is imperative to perform a comparative study of the proposed Soft-FET inverter and CMOS inverter variants for peak current and di/dt reduction. The comparison (Fig. 5) is performed by tuning the baseline CMOS parameters (threshold voltage V_T, constant series resistance, # of transistors in the stack) such that all the cases result in approximately same I_{MAX} (peak switching current) as that of the Soft-FET inverter (i.e., iso-I_{MAX} at V_{CC}= 1V). High supply voltage of 1V is used for iso-I_{MAX} comparison as I_{MAX} is typically highest (worst) at the higher V_{CC}. SPICE simulations for minimum sized inverters are performed over a wide voltage range to evaluate the impact of iso-I_{MAX} matching on the inverter delay. For a fair comparison, all inverter topologies drive a constant FO4 load (Fan Out of 4).

In the case of High V_T (HVT) CMOS, the threshold voltages of transistors (both NMOS and PMOS) are adjusted to match the I_{MAX} of the Soft-FET inverter when operated at 1V. This HVT variant shows output delay (time between 50% input to 20 (or 80) % output rise (fall)) comparable to the Soft-FET. However, when operated at lower V_{CC}, the high V_T transistors exhibits lower I_{MAX}, but significantly larger delay compared to the Soft-FET inverter (Fig. 5). This delay degradation can be attributed to the extremely low saturation current in HVT transistors operating at lower voltages (smaller V_{GS}-V_T term). Hence, the HVT transistors although achieve same I_{MAX} as that of the proposed Soft-FET while operating at higher voltages, incur significant delay penalty at low voltages. In the second scenario, an equivalent constant gate series resistance is used in the baseline CMOS inverter to match the same I_{MAX} as that of the Soft-FET inverter (at V_{CC}=1V). This variant exhibit similar I_{MAX} but results in longer delay across the V_{CC} range compared to the Soft-FET inverter. The constant resistor in the gate causes the charging/discharging the output capacitor with large time constant leading to significantly larger delays compared to voltage dependent variable time constants in the Soft-FET. In the third scenario, stacked transistors are used (both NMOS and PMOS) to reduce the switching current in the CMOS inverter. This case also results in larger delay across the V_{CC} range compared to the Soft-FET inverter. The large delay in this scenario can be associated with the additional current required to charge the intermediate voltage nodes (A, B). Thus, the proposed Soft-FET achieves substantial peak switching current

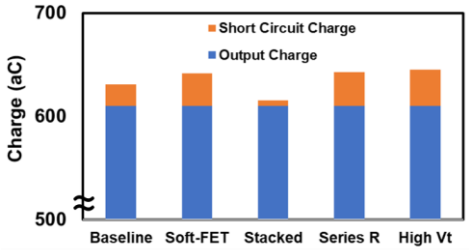


Fig. 7 Total charge comparison of Soft-FET inverter with various CMOS topologies

reduction with minimal delay penalty compared to the other CMOS topologies, over a wide operating voltage range.

IV. PTM Design Space Analysis

A. Design space exploration

The Soft-FET performance (I_{MAX} and di/dt reduction) is strongly dependent on the intrinsic device parameters (V_{IMT}, V_{MIT}, R_{INS}, R_{MET}, T_{PTM}) of the PTM material. Varying device parameters affects the soft-switching behavior of the Soft-FET. This can lead to varying peak current drawn from the V_{CC} rail for the same output load and transistor size. So, there is a need to explore the PTM device parameter design space and optimize the PTM for the best Soft-FET performance. For this analysis, we have fixed the R_{INS} (= 500kΩ), R_{MET} (= 5kΩ), T_{PTM} (= 10ps PTM switching time) values and varied the voltage thresholds (V_{IMT}, V_{MIT}). The peak current, di/dt and delay of the Soft-FET inverters are compared for the varying V_{IMT} and V_{MIT} values. The input rise time of 30ps and V_{CC} of 1V are fixed for these comparisons. Fig.6, shows the variation in the peak current of the Soft-FET inverter as a function of both V_{IMT} and V_{MIT}. As it is evident from the Fig.6, there is a dip in the I_{MAX} around certain values of V_{IMT} (around 0.4V) which is an ideal zone for the Soft-FET operation. This behavior can be understood by analyzing the transient behavior of the inverter for V_{IMT} values around 0.4V. Fig. 6 shows the gate voltage (V_G) transients for three V_{IMT} values (0.3V, 0.4V and 0.5V). When the supply voltage (V_{IN}) falls, the first pair of transition occurs, and the V_G attained when V_{IMT} equal to 0.3V is more (V_G-V_{IN} > V_{IMT}) compared to the cases when V_{IMT} equals 0.4 or 0.5 V. Thus, the voltage across the insulating PTM can reach V_{IMT} again causing a second pair of transition. Whereas, in the case of V_{IMT} equal to 0.4 or 0.5V, the V_G attained is small enough (V_G-V_{IN} < V_{IMT}) such that the voltage across the insulating PTM cannot reach V_{IMT}. Thus, the Soft-FET with V_{IMT} equal to 0.3V makes the phase transition twice (two iterations of insulator-metal transition) but the Soft-FET with V_{IMT} equal to 0.4V or 0.5V makes only one iteration of phase transition. Followed by the second phase transition (at 50ps) in the V_{IMT} equal to 0.3V, the gate voltage approaches a value close to Vss. So, the PMOS is strongly turned on (large V_{GS}) leading to larger peak current drawn from the V_{CC} rail. Similarly, the Soft-FET with V_{IMT} equal to 0.5V also makes the transition to the region with strongly turned on PMOS leading to relatively large transient current. Whereas, the Soft-FET with V_{IMT} equal to 0.4V attains a higher V_G (lower V_{GS}) leading to lower peak current being drawn from the V_{CC} rail. This implies that the Soft-FET with V_{IMT} values 0.3 and 0.5V turn on the PMOS transistor strongly compared to the Soft-FET with optimum V_{IMT} value equal to 0.4V.

Similar analysis for delay variation with intrinsic PTM parameters is in shown in Fig. 6. It is evident that the delay is large for the same range of V_{IMT} values having low peak current. This is because the inverters with higher peak current charge the output voltage quickly compared to low peak current inverters. However, the maximum of di/dt (derivative of the current drawn from the V_{CC} rail) variation with intrinsic parameters shows a different trend. The maximum di/dt of the Soft-FET inverter increases for increasing

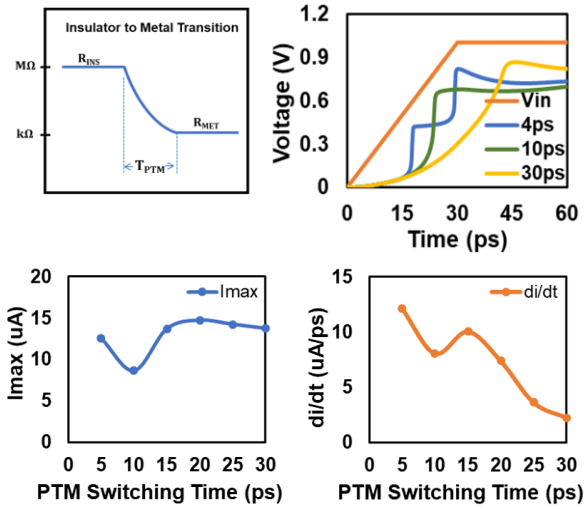


Fig. 8 Effect of PTM switching time (T_{PTM}) on I_{MAX} and di/dt

values of V_{IMT} threshold. Once again, this can be understood by looking at the gate voltage transients shown in Fig.6, As explained earlier, the Soft-FET inverter with of V_{IMT} equal to 0.3V makes two transitions, so the pull up transistor is weakly turned on during the first phase change transition followed by strong turn on during the second transition. So, both the transitions lead to smaller di/dt because of the gradual increase in the current (off current - weakly turned on - strongly turned on). Whereas, the Soft-FET inverter with V_{IMT} equal to 0.4V makes single transition to moderately turn ON condition leading to higher di/dt compared to V_{IMT} equal to 0.3V. Similarly, the V_{IMT} equal to 0.5V case makes even larger transition to strongly turned ON condition leading to a larger di/dt in comparison with other cases. Thus, the intrinsic parameters of the PTM material play a crucial role in the Soft-FET performance and must be appropriately tuned with careful device fabrication for enhancing the Soft-FET performance.

B. Design tradeoffs

The proposed Soft-FET incurs delay penalty for slow charging/discharging the output nodes as it is evident from the output characteristics shown in Fig. 5. However, as explained earlier it provides the minimal delay penalty across a wide voltage range. Moreover, a portion of the Soft-FET delay penalty can be attributed to the switching time taken by the PTM to make transition from insulating to metallic phase. Reducing the PTM switching time (T_{PTM}) can reduce the overall delay of the Soft-FET transistors.

In addition, the Soft-FET incurs increased short circuit charge compared to the baseline inverter. Soft-FET inverter short circuit duration comprises of two parts. First time interval consists of fast transition of the gate input once V_{IN} crosses V_{IMT} threshold. This narrow time duration results in lower short circuit charge compared to the baseline CMOS inverter. On the other hand, the second-time interval consists of a slowly changing gate input once the PTM has switched to the insulating phase. This longer time duration results in significant short circuit charge. The net result of compensating effects of these time intervals decide the overall short circuit charge consumed by the Soft-FET inverter. Fig. 7 shows the short circuit and output charge consumed during the falling input transition (V_{CC} = 1V) for various current reduction techniques discussed in earlier section. Soft-FET performs on par with HVT and series-R cases with respect to the short circuit charge.

C. Intrinsic PTM switching time

The intrinsic switching time (T_{PTM}) is the time taken by the PTM to make the transition from insulating phase to

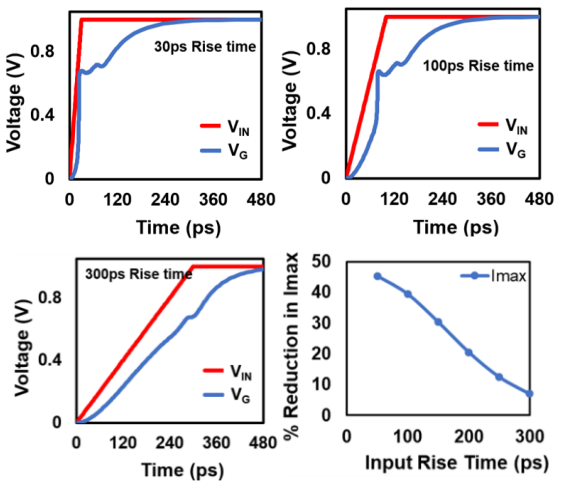


Fig. 9 Effect of input slew rate on the PTM switching behavior

metallic phase and vice versa. After the voltage across the PTM reaches the switching thresholds, the resistance of the PTM increases/decreases and reaches the desired value after T_{PTM} duration. Recent experiments have demonstrated femto-second phase transition times in VO_2 PTMs using optical excitations and switching time of ~8ps with electrical excitations [16] [17]. The switching time determines the shape of the V_G waveform and thus plays a crucial role in the performance of the Soft-FET based logic. Hence, the performance of the Soft-FET inverter is assessed for varying intrinsic switching speeds. For this analysis, all the other PTM parameters are fixed to the standard values shown in Fig. 4. For smaller T_{PTM} values V_G experiences multiple phase transitions as shown in Fig. 8. This is due the fast switching of PTM resulting in a rapid catch up of V_G node to the V_{IN} node. The final phase transition occurs close to V_{CC} causing a strong MOSFET turn on leading to larger peak current. The number of phase transitions decrease with increasing T_{PTM}. Large T_{PTM} also results in a strong transistor turn on leading to higher peak current. However, if the T_{PTM} is properly optimized then the transition occurs in a region where PMOS transistor is weakly ON leading to lower peak current drawn from the V_{CC} rail. The delay of the Soft-FET varies in a complimentary manner leading to a peak at moderate T_{PTM} values. However, the di/dt shows a decreasing trend with increasing T_{PTM}.

D. Slew rate of input signal

The slew rate of the input signal is also an important factor in the Soft-FET performance. The switching behavior of the Soft-FET is determined by the (input slew-rate/R_{PTM}*C) ratio. At higher ratios, the V_G cannot increase at the rate of V_{IN} due to large time constant. This creates an increasing voltage across the PTM and leads to the phase transition. However, at smaller ratios, the V_G can rise at the same rate of V_{IN} and thus fewer phase transition behavior is observed. Hence, the slew rate of the input signal must be appropriately tuned for obtaining the best Soft-FET performance. Fig. 9 shows the V_G waveforms for three different values of the input slew rate. The simulations are performed keeping all the intrinsic parameters of the PTM as shown in Fig. 4 and V_{CC}=1V. It is evident that the soft-switching behavior of the Soft-FET vanishes with decreasing slew rate. The reduced switching

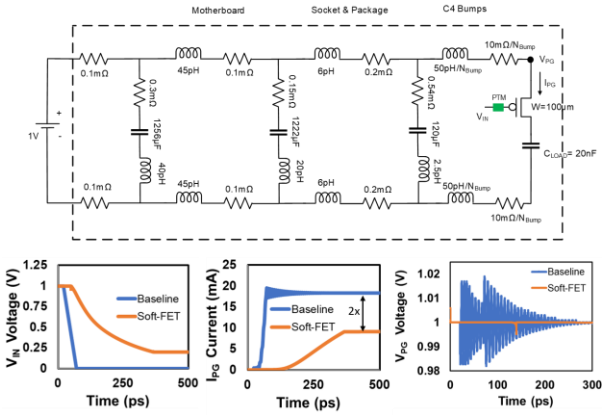


Fig. 10 Soft-FET applications in power gate design

behavior makes the Soft-FET behave more like the baseline CMOS but with increased delay. Thus, the peak current and di/dt reduction are not significant. Fig. 9 shows the percentage I_{MAX} reduction for varying values of the input slew rate. The di/dt follows similar trend to I_{MAX} but delay increases with decreasing slew rate.

E. Design recommendations

It is apparent from the previous two sections that switching speed of the PTM and the input slew rate need to be optimized for the desired reduction in peak current and di/dt. We recommend the ratio of input slew rate to the PTM switching time need be around 1.5-3. However, this ratio is strong function of V_{CC} and/or V_{IMT} parameters.

V. SOFT-FETS FOR VOLTAGE DROOP MITIGATION

This section presents two application case studies of the proposed Soft-FET transistor in mitigating the voltage droops due to high capacitive load driving.

A. Soft-FETs for power gate design

As power management is becoming crucial for extending the battery lifetime of handheld devices, the frequency of entering/exiting the sleep states become quite frequent [18]. While exiting the sleep mode, sudden surge of load charging current can cause large di/dt and can induce a voltage droop on the neighboring active units sharing the same supply rail (V_{CC}). This voltage droop needs to be margined in the supply voltage specifications which degrades the energy efficiency. The proposed Soft-FET concept can be utilized in a power-gate design with soft-transitioning gate voltage as shown in Fig. 10. The power delivery network parameters are adopted from [19]. The proposed Soft-FET concept slows down the ramp rate of the power-gate gate voltage and which reduces the current by 2X. The supply voltage droop is reduced by ~20mV using Soft-FET power gate which would result in improved energy efficiency.

B. Soft-FETs for I/O buffer design

The rapid changes in the current consumption of a circuit block having many logic gates and I/O buffers switching simultaneously combined with the series inductance of the power distribution network (PDN) results in Simultaneous Switching Noise (SSN) [20]. The SSN causes

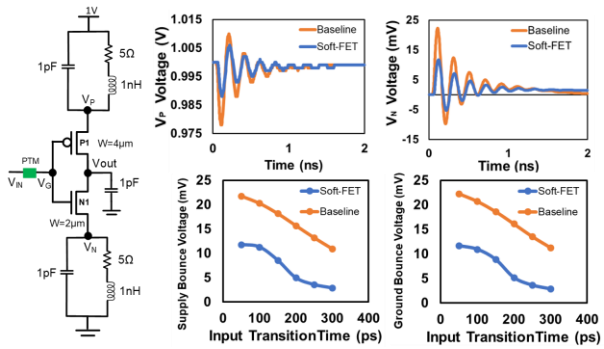


Fig. 11 Soft-FET applications in I/O buffer design

ringing on the V_{CC} and Vss rails and needs to be accounted in the supply voltage specifications. The increased voltage guard bands necessitate higher operating voltage for achieving target performance degrading the energy efficiency. Fig. 11 shows a case study of an I/O buffer driving a pad load capacitance of 1pF and experiencing a V_{CC} and V_{SS} bounce of ~22mV. The proposed Soft-FET can be effectively used to control the I/O buffer input slew rate by utilizing the abrupt phase change in the PTM. The soft-switching mechanism reduces the peak current and the di/dt lowering the SSN noise in Soft-FET I/O drivers by 46% compared to the baseline I/O drivers. In this analysis, the PTM parameters are same as shown in Fig. 4. Furthermore, the Soft-FET I/O driver achieves higher SSN improvement with increasing input transition times as shown in Fig. 11. The reduced SSN would lead to a lower operating voltage improving the energy efficiency by 8.8% when operating at V_{CC}=1V.

VI. CONCLUSION

In this paper, we proposed a soft-switching transistor architecture named "Soft-FET" utilizing the abrupt phase change mechanism in the phase transition materials. By placing an optimized PTM in series with the gate terminal of a MOSFET, its gate voltage can be changed smoothly resulting in reduced peak switching current and lower di/dt. The proposed Soft-FET based inverter shows minimal delay penalty across a wide voltage range compared to other CMOS inverter variants under Iso-I_{MAX} conditions. We presented detailed PTM parameter optimization for the best Soft-FET performance and showed its applications in power gate design and I/O buffer design to mitigate the voltage supply droops for improved energy efficiency. Preliminary experiments on VO_2 material have shown reliability > 10^9 cycles [21]. Further studies in this domain are required for obtaining high quality phase transitions in these materials.

VII. REFERENCES

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