Structural and electrical characterization of thick GaN layers on Si, GaN, and engineered substrates

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ABSTRACT

A major challenge in gallium nitride (GaN) vertical power devices and other large bandgap materials is the high defect density that compromises the performance, reliability, and yield. Defects are typically nucleated at the heterointerface where there are both lattice and thermal mismatches. Here, we report the selective area growth (SAG) of thick GaN on Si and on the newly available Qromis Substrate Technology™ (QST) substrates that lead to a significant reduction of the defect densities to a level that is nearly comparable to that on native substrates by defect annihilation. We performed a parametric study of the electrical properties of the SAG GaN layers by fabricating and characterizing Schottky barrier diodes for SAG GaN layer thicknesses of 5, 10, 15, and 20 μm for GaN-on-Si, GaN-on-QST, and GaN-on-GaN diodes. While thicker layers led to a significant reduction in defect densities and improvement in the diode forward current characteristics, the GaN-on-QST diodes exhibited nearly similar characteristics to the GaN-on-GaN diodes. Further improvement in the device structure and/or SAG growth for GaN-on-Si is needed to achieve a comparable performance as the defect densities in the GaN-on-Si are comparable to that of GaN-on-QST substrates.

I. INTRODUCTION

The success of single phase growth of gallium nitride (GaN) and indium gallium nitride (InGaN)[1] has fueled the rapid commercialization of GaN devices such as blue light emitting diodes (LEDs) and generated strong interest in GaN as the basis material for next generation high power electronic devices. The recent progress on bulk GaN crystal growth techniques such as Na-flux, Hydride Vapor Phase Epitaxy (HVPE), and ammonothermal methods have made it possible to make vertical GaN devices with low threading dislocation densities (TDDs).[2–4] However, cost, scalability, growth uniformity, and device reliability over large areas remain challenges to market adoption of technologies based on these substrates. The heteroepitaxy of GaN on cheap and technologically well-developed substrates such as Si would give an advantage to scalable and cost effective production and further the monolithic integration to Si CMOS technology. But heteroepitaxial GaN usually suffers from a large TDD which has been a critical barrier for its utility in power electronics since leakage currents and breakdown voltages are strongly correlated to the TDDs and impurities.[5–8] Earlier pioneering work on the heteroepitaxial growth of thick GaN on sapphire substrates has successfully reduced the number of dislocations and showed improved device performances.[9] However, epitaxy techniques developed on sapphire cannot be simply adopted for the growth of GaN-on-Si due both to the large in-plane thermal expansion coefficient (CTE) ($5.59\times10^{-6}\,K^{-1}$ for GaN and $2.6\times10^{-6}\,K^{-1}$ for Si) and to the 17% of lattice mismatch which combine to generate tensile stress and cracking in the GaN films that are as thin as 4 μm. Recently, we utilized selective area growth (SAG) approaches to safely deflect these mismatch stresses to grow structures that can be as thick as 20 μm for GaN-on-Si without cracking.[10] Here, we utilize these growth techniques to carry out parametric studies on

the influence of the thickness (5 μm-20 μm) of GaN drift layers on the performance metrics of GaN-on-Si Schottky barrier diodes (SBDs), GaN on newly commercialized Qromis substrate technology™ (QST) based on polycrystalline AlN[11] with matched CTE (GaN-on-QST), and benchmark the results relevant to GaN-on-GaN devices. We have succeeded in decreasing dislocation densities in heteroepitaxial GaN by growing thick SAG GaN, as demonstrated via etch pit density measurement and transmission electron microscopy (TEM), and improved SBD characteristics proven by current-voltage (I-V) and capacitance-voltage (C-V) measurements.

II. EXPERIMENT

The SAG of GaN was performed on three difference substrates: GaN-on-Si, free-standing GaN (SCIOCS), and CTE matched QST substrate (Qromis®) by a 3 × 2 in. Thomas Swan/Aixtron close-coupled showerhead metal-organic chemical-vapor-phase deposition (MOCVD) system. The starting GaN-on-Si substrate consists of a 500 nm n-type GaN layer on AlGaN/AlN buffer layers on Si(111) provided by Powdec, Inc. The 400 μm thick n-type GaN substrate (SCIOCS) was grown by HVPE and the starting QST substrate (Qromis) had ~8 μm unintentionally doped GaN. The coefficient of thermal expansion (CTE) for the QST substrate is carefully matched with the CTE of GaN resulting in negligible thermal mismatch stresses in the GaN film. We grew a 1 μm n-type GaN layer doped with Si on top of the GaN-on-QST substrate for current spreading underneath the vertical drift layer of the SBDs, a layer that is adopted for all other substrates. The sheet resistances and doping concentrations of n-GaN buffer layer for each substrate were determined by Hall effect measurements and are listed in Table I. For all types of starting substrates, the area of each sample was 5 × 5 mm^2, and strong edge effects and non-uniformities in the growth were expected: the area is chosen to be small due to the high cost of the substrates. 200 nm SiO_2 layers were deposited over these substrates by plasma enhanced chemical vapor deposition (PECVD), and 4 × 5 arrays of circular openings were patterned and dry-etched by photolithography and reactive ion etching (RIE). The design of the selective growth masks was specifically optimized for the growth of thick GaN-on-Si which is described in detail in our earlier work.[10,12] Different thicknesses of SAG and unintentionally doped (UID) GaN were grown on each substrate and calibrated to result in thicknesses of 5 μm to 20 μm, at a relatively constant growth rate of 5 μm/h for all samples, despite differences in the substrate thermal conductivities. These grown structures permitted us to perform parametric studies on the thickness dependence and the effect of substrate composition on the grown material quality and device characteristics. SBDs were fabricated by the electron beam evaporation of 200 nm Ni Schottky contacts on top of the SAG UID GaN dots that is followed by photolithography patterning and etching. The ohmic contacts on the n+GaN planar layer were defined around the UID GaN dot by photolithography and lift-off process and were composed of a Ti(30 nm)/Al(70 nm)/Ti(10 nm)/Au(50 nm) non-annealed ohmic contact deposited by electron beam evaporation. For GaN-on-GaN SBDs, the same ohmic contact was evaporated on the back of the substrate. The surrounding peripheries of the metal Schottky contacts were dry etched by BCl_3/Cl_2 RIE to a 1 μm depth to reduce the edge effects and surface leakage currents of the SBDs.

The SBD characteristics were evaluated by performing I-V and C-V measurements using a Keysight B1500A semiconductor analyzer. After all electrical measurements, the Schottky metal contacts were completely etched by a Ni wet etchant and then the samples were immersed in H_3PO_4:H_2SO_4 solution (HH solution) at 270 °C to selectively etch the threading dislocations under the Schottky contact.[13] The number of etch pits at the surface under the contact was counted under FEI Apreo scanning electron microscopy (SEM). Cross-sectional TEM images using an FEI Tecnai G(2) F30 S-Twin were also taken to evaluate TDD.

TABLE I. Substrate and buffer layer details and properties.

	GaN-on-GaN	GaN-on-QST	GaN-on-Si
Substrate growth	HVPE	NA	NA
As received GaN thickness	400 μm	8 μm	1.1 μm
Additional planar buffer layer growth	None	1 μm	None
Planar surface layer sheet resistance	0.12 Ω/□	42.3 Ω/□	210 Ω/□
Surface layer doping density	5.5 × 10^{18} cm^{-3}	7.8 × 10^{18} cm^{-3}	4.1 × 10^{18} cm^{-3}
SAG GaN in 350 μm diameter dot	5-20 μm	5-20 μm	5-20 μm

III. RESULT AND DISCUSSION

A. Evaluation of defect densities as a function of thickness on each substrate

The defect preferential etching under the Ni Schottky contacts was performed on all 12 samples. Figure 1 shows the top-view SEM images of the SAG GaN dot surfaces with an area of 25 μm^2 after defect selective etching. The HH solution reveals mixed and screw dislocations as large hexagonal pits and edge dislocations as small pits.[13,14] The dislocation densities of each sample can be estimated by direct counting of these etched pits and dividing the counted pit number by the 25 μm^2 area. The dislocation densities of the starting substrates are estimated to be ~10^9 cm^{-2} for the GaN-on Si, ~10^8 cm^{-2} for the GaN-on-QST substrate, and ~10^6 cm^{-2} for the GaN substrate. The top view SEM images were chosen at random from 20 SAG GaN dots in the same sample, and the etch pit densities are averaged from all of the 20 dots for comparison. As shown in Fig. 1, the GaN-on-Si samples showed a clear linear reduction of the pit density from 1.8 × 10^7 cm^{-2} to 3.4 × 10^6 cm^{-2} with an increase in the GaN thickness. The same trend of dislocation density reduction was observed in GaN-on-QST samples from 3.5 × 10^6 cm^{-2} to 9.0 × 10^5 cm^{-2} where the overall etch pit densities were about one order of magnitude smaller than GaN-on-Si. No pits were observed from GaN-on-GaN samples within the area of

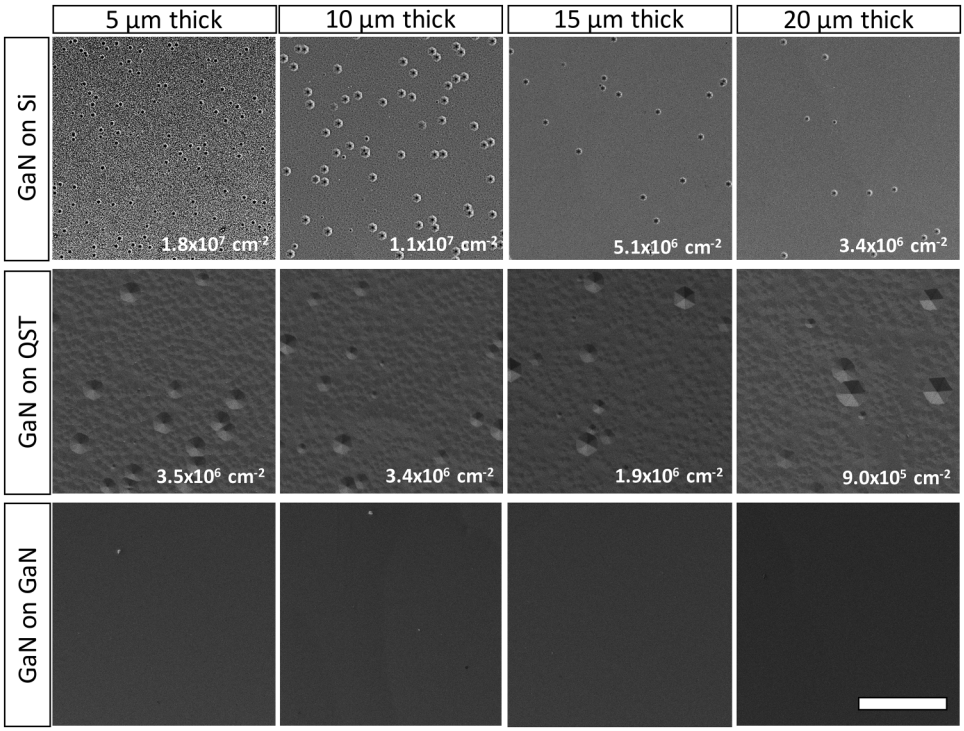

FIG. 1. Top view SEM images of GaN surface after defect selective etching. Linear reduction of defect densities was observed in GaN-on-Si and GaN-on-QST with increasing the thicknesses. The GaN-on-GaN samples did not show any surface pits after the etching. The scale marker is 10 μm.

25 μm^2 which indicates that the defect densities of the GaN-on-GaN are less than 1.6×10^5 cm^{-2} at the surface of the SAG GaN dots.

The number of dislocations measured by the etch pit densities is usually underestimated because two or more adjacent dislocations may be combined into one large etch pit. Therefore, dislocation density was also estimated from cross-sectional TEM slices made at the center dot for all 12 samples as shown in Fig. 2. It is important to note that the numbers quoted below are deduced from one TEM slice/lamella to support the trends observed with the etch-pit density experiments; an accurate estimate of the TDDs from TEM characterization must be obtained from a large number of TEM slices/lamellas. One can observe that for the 5 μm thick GaN-on-Si, many dislocations nucleated at the interface with the Si substrate and prevailed up to 4 μm from the GaN/Si interface. However, only less than 10% of dislocations made it to the surface of the 5 μm thick GaN-on-Si dot that was grown for 1 h, due to the tendency of the dislocations to bend and annihilate. As the thickness increased, the probability of annihilation became larger, which resulted in a lower dislocation density for thicker GaN films. Numerous earlier studies have reported the dislocation bending in SAG by epitaxial lateral overgrowth.[15,16] We believe that the dislocation bending in our samples was not caused by either facet termination or dielectric layer masking, but by stress generation and resultant atom/vacancy diffusion from/to the dislocation cores.[17–19]

Interestingly, the bending of dislocation was not only observed in highly stressed GaN-on-Si samples but also in GaN-on-QST samples where there is minimal thermal stress between the GaN and the substrate material. The dislocation density of 20 μm thick GaN-on-Si is almost the same value as 5 μm GaN-on-QST. The reduction of dislocation density in GaN-on-QST could be related to compressive stress generated at the SAG mask/regrowth interface since this reduction was much faster than in planar regions. Additionally, by the nature of the enhanced reactant collection and growth rates at dot edges, stresses due to thickness non-uniformities (thicker at dot peripheries compared to dot center) are likely to contribute to dislocation bending and annihilation. In the cross-sectional TEM images of the GaN-on-GaN SAG, there is no evidence of threading dislocations within the TEM lamella width of 10 μm which indicates that the dislocation density for the GaN-on-GaN samples is below 1×10^6 cm^{-2}.

B. Evaluation of SAG electronic properties by Schottky barrier diode characterization

The fabricated SBDs were characterized by I-V and C-V measurement. Since no doping impurities were intentionally added during the growth, and at moderate unintentionally

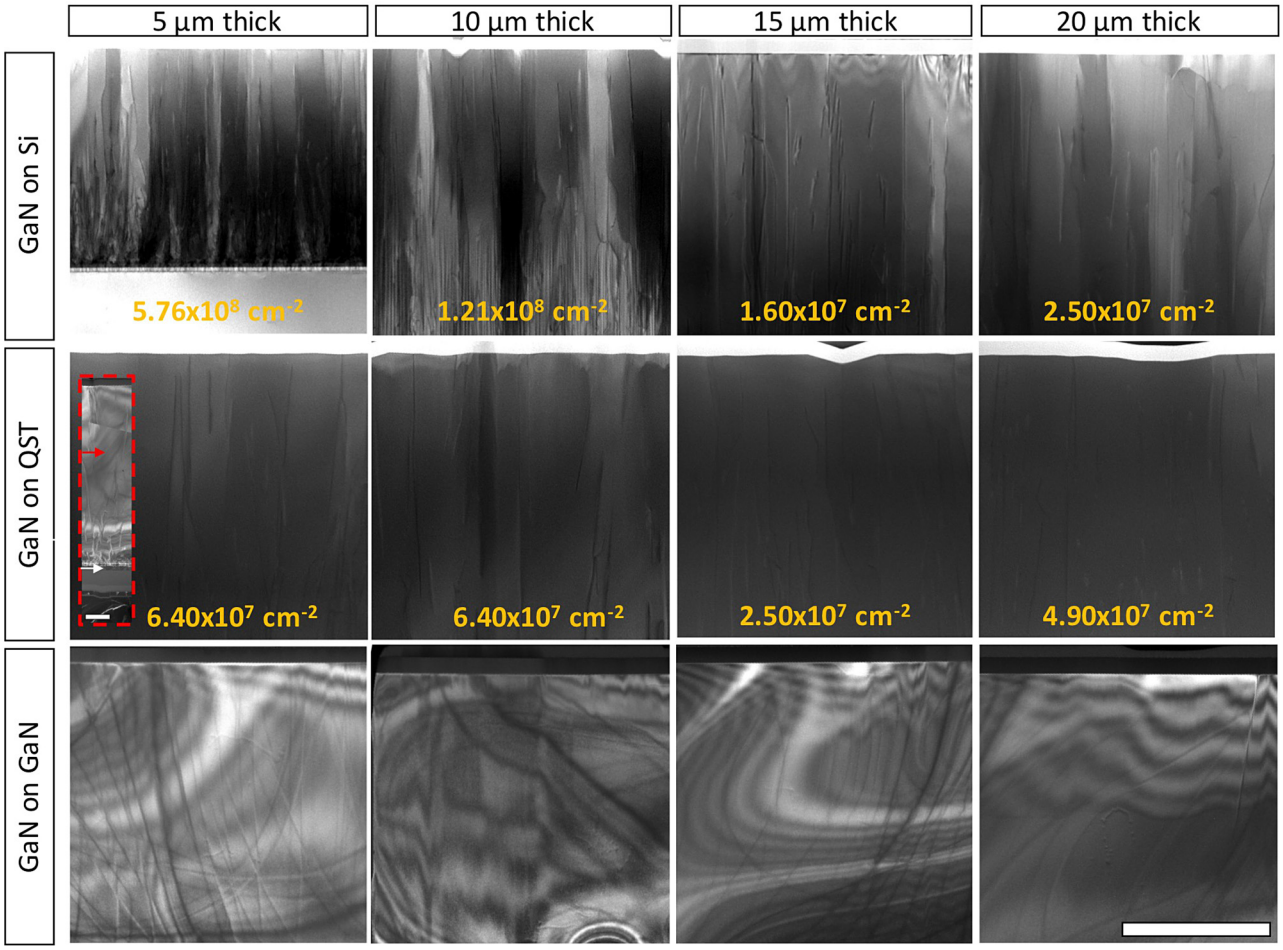

FIG. 2. Cross-sectional TEM images under the Schottky contact (g = [0001]). The width of the imaged sections is 10 μm and the scale bar is 5 μm. The inset for the 5 μm thick GaN-on-QST is a larger field of view TEM image that shows the interface with the Si layer (white arrow) and the location of the pre-grown planar GaN layer (red arrow) prior to SAG. The inset scale marker is 2 μm.

doped layers, the SBD current is dominated by thermionic emission (TE). Under forward bias with $V_D > 3\,kT/q$, the SBD current can be expressed by the fundamental TE diode current equation,

$$I = I_s[\exp(qV_D/nkT)], \tag{1}$$

where q is the fundamental electron charge constant, V_D is the voltage applied across the diode, k is the Boltzmann constant, and T is the absolute temperature. I_s can be expressed by[20]

$$I_s = A_{eff}A^{**}T^2\exp[-q\phi_{B(IV)}/kT], \tag{2}$$

where A_{eff} is the effective area of the SBD contact and A** is the Richardson constant. The diode ideality factor, n, and the Schottky barrier height, $\phi_{B(IV)}$, are extracted by fitting the semi-log I-V characteristics for each diode. The diode turn-on voltage is defined as the inflection voltage that is determined by extrapolating a fitted line to the linear region of the forward I-V characteristics.

For a standard reverse biased SBD, the carrier concentration can be extracted from changes in the capacitance by depletion width modulation with applied bias according to[20]

$$N_d = \frac{2}{q\varepsilon_0\varepsilon_s}\left[-\frac{1}{d(1/C_d^2)/dV}\right], \tag{3}$$

where ε_0 is the permittivity of free space, ε_s is the dielectric constant of the semiconductor material, and C_d is the depletion layer capacitance. The carrier concentration, N_d, is estimated from the slope of $1/C_d^2$ as a function of voltage. The intercept of this $1/C_d^2$ with the voltage axis gave the built-in potential which was used to estimate the barrier height

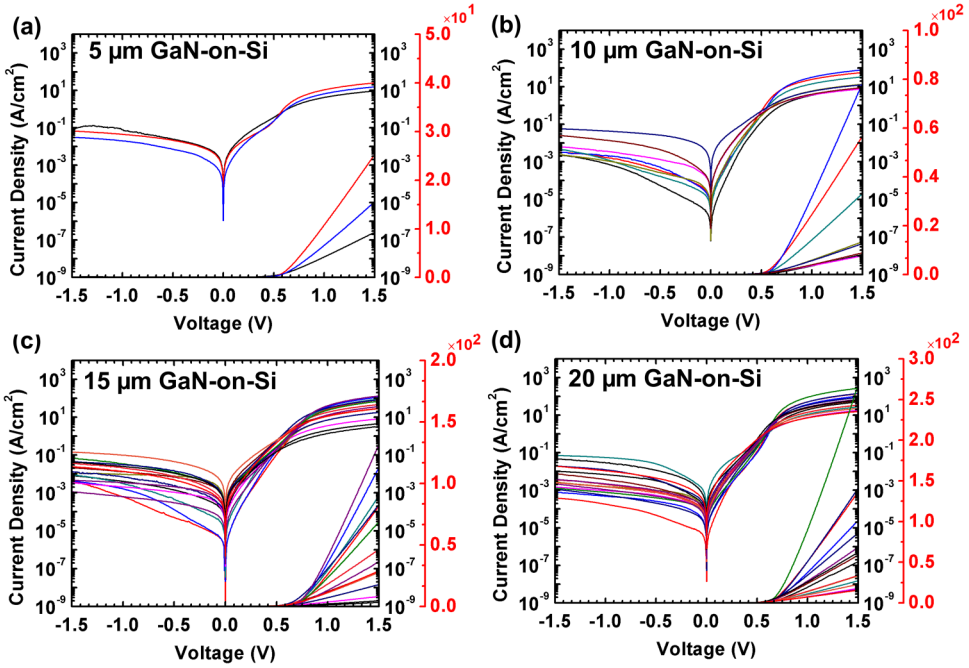

FIG. 3. Linear and semi-log scale I-V characteristics of GaN-on-Si SBDs with different thicknesses of (a) 5 μm, (b) 10 μm, (c) 15 μm, and (d) 20 μm. IV characteristics from all 20 devices in an individual array (same substrate) are plotted with different colors in (c) and (d). For thinner layers (5 μm and 10 μm) of (a) and (b), multiple dots were cracked and, therefore, the number of functional devices is lower than that for thicker layers. The red axis shown in the right side is the linear scale axis.

TABLE II. GaN-on-Si SBD characteristics.[a]

	5 μm thick (GaN-on-Si)		10 μm thick (GaN-on-Si)		15 μm thick (GaN-on-Si)		20 μm thick (GaN-on-Si)	
	Best	**Avg ± stdev**	**Best**	**Avg ± stdev**	**Best**	**Avg ± stdev**	**Best**	**Avg ± stdev**
Ideality factor	2.65	3.81 ± 1.45	2.05	3.01 ± 0.90	2.40	3.32 ± 0.60	**1.13**	2.36 ± 0.60
V_{on} (V)	0.64	0.62 ± 0.03	0.66	0.61 ± 0.03	**0.79**	0.70 ± 0.06	0.76	0.67 ± 0.05
$\phi_{B(IV)}$ (eV)	0.60	0.55 ± 0.06	0.63	0.57 ± 0.05	0.64	0.56 ± 0.04	**0.73**	0.62 ± 0.06
$\phi_{B(CV)}$ (eV)	1.21	1.13 ± 0.06	1.16	1.11 ± 0.03	**1.30**	1.19 ± 0.05	1.13	1.11 ± 0.02

[a]The values in bold font show the best values among all measured devices.

according to

$$\phi_{B(CV)} = V_{bi} + \varphi_n. \tag{4}$$

Here, $\varphi_n = kT/q \ln(N_c/N_d)$ is the doping potential that is determined for the doping concentration determined from Eq. (3). The effective density of states in the conduction band edge is given by $N_c = 2(2\pi m^* kT/h^2)^{\frac{3}{2}}$, where the effective electron mass of GaN is $m^* = 0.22m_0$.[21]

Figure 3 shows the linear and semi-log scale I-V characteristics for GaN-on-Si SBDs with different thicknesses. For the 5 μm thick GaN-on-Si sample, the incomplete formation of hexagonal facets for such thin layers does not relieve thermal stresses as previously described,[10] and as a result, there were only 3 uncracked GaN dots out of 20 in this sample. The number of uncracked dots increased with GaN film thickness by deflecting the stresses to the surface hexagonal facets that were complete and flat. The reverse leakage current in the SBD decreased linearly with increasing GaN thicknesses, in accord with the linear reduction of dislocation densities. One of the major conduction paths for current in metal-contacted GaN is known to be through screw dislocations whereas edge type dislocations retain the Schottky contact characteristics with metals.[22] The reduction of the screw dislocations verified by Figs. 1 and 2 contributed significantly to the reduction of leakage currents from 10^{-1} A/cm^2 to 10^{-3} A/cm^2. In addition, the slope of the linear I-V plots should ideally decrease with thickness since the diode resistance, $R_{diode} = t/A_{eff} \cdot q \cdot \mu \cdot n$, should linearly increase with thickness, where t is the thickness of the drift layer, q is the

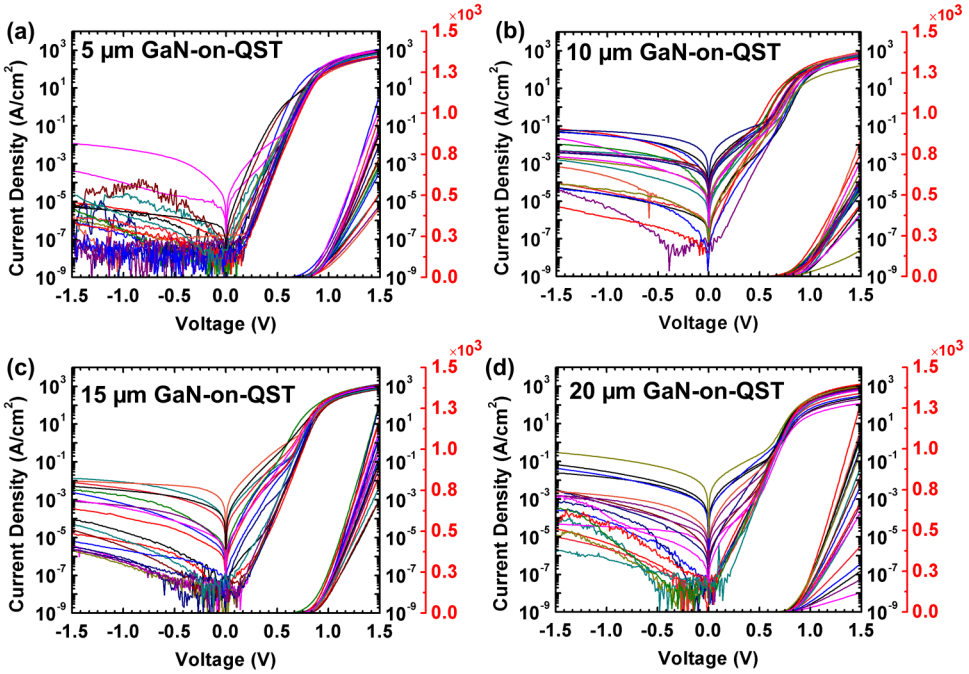

FIG. 4. Linear and semi-log scale I-V characteristics of GaN-on-QST SBDs with different thicknesses of (a) 5 μm, (b) 10 μm, (c) 15 μm, and (d) 20 μm. IV characteristics from all 20 devices in an individual array (same substrate) are plotted with different colors. The red axis shown in the right side is the linear scale axis.

TABLE III. GaN-on-QST SBD characteristics.[a]

	5 μm thick (GaN-on-QST)		10 μm thick (GaN-on-QST)		15 μm thick (GaN-on-QST)		20 μm thick (GaN-on-QST)	
	Best	**Avg ± stdev**	**Best**	**Avg ± stdev**	**Best**	**Avg ± stdev**	**Best**	**Avg ± stdev**
Ideality factor	**1.11**	1.31 ± 0.31	1.47	1.74 ± 0.78	1.58	1.98 ± 0.24	1.18	1.51 ± 0.30
V_{on} (V)	0.98	0.95 ± 0.03	**1.01**	0.95 ± 0.05	0.93	0.89 ± 0.02	0.94	0.91 ± 0.01
$\phi_{B(IV)}$ (eV)	**0.96**	0.89 ± 0.07	0.89	0.78 ± 0.06	0.81	0.70 ± 0.05	**0.96**	0.84 ± 0.08
$\phi_{B(CV)}$ (eV)	1.37	1.34 ± 0.03	**1.39**	1.35 ± 0.02	1.32	1.30 ± 0.02	1.33	1.29 ± 0.02

[a]The values with bold font show the best values among all measured devices.

electron charge, n is the free electron concentration in the drift layer, and μ is the electron mobility in the drift layer.[5] However, the slope of the linear I-V plots shown in Fig. 3 increased with thickness, which suggests an increase of the electron mobility assuming that the unintentional n-type doping in the drift layer does not change for 5-20 μm thick drift layers. Earlier studies have shown that changes in the background (O and Si) doping concentration in the growth direction (c-axis) during SAG GaN growth were confined to the first 5 μm.[23–25] Therefore, the effects of dielectric decomposition and unintentional incorporation of Si and O from the dielectric mask can be neglected especially for SBDs with thicknesses above 5 μm. By considering the potential for Coulombic interaction between electrons and charged dislocation lines, the large reduction of TDDs significantly improved the electron mobility in the drift layer for thicker GaN,[26] which we estimated to be, on average, about three times higher for the 20 μm thick layers than the 5 μm layer. The absolute numbers for the mobility are not reported because of the lack of a specific method to accurately measure the contact and series resistances in our structures. It is important to note that changes in the background doping concentration due to TDD annihilation and dominance of surface leakage current or confinement of current transport to the outermost layers of the drift region may also contribute to the lower R_{on} of the thicker GaN drift layers. As shown in Table II, the ideality factor, barrier height, and turn on voltage of the SBDs were also improved with increasing the GaN thicknesses. These improved characteristics are attributed to the improved Schottky contact interface quality with fewer surface defects for thicker GaN films.

Figures 4 and 5 show the linear and semi-log scale I-V characteristics for GaN-on-QST and GaN-on-GaN SBDs with different thicknesses. The leakage currents and forward SBD

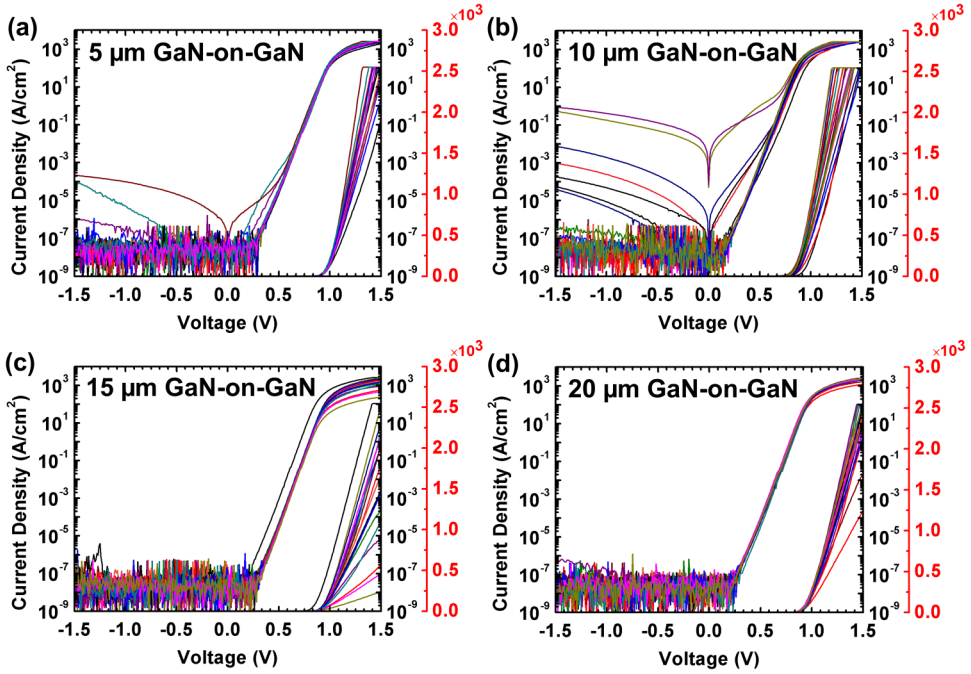

FIG. 5. Linear and semi-log scale I-V characteristics of GaN-on-GaN SBDs with different thicknesses of (a) 5 μm, (b) 10 μm, (c) 15 μm, and (d) 20 μm. IV characteristics from all 20 devices in an individual array (same substrate) are plotted with different colors. The red axis shown in the right side is the linear scale axis.

TABLE IV. GaN-on-GaN SBD characteristics.[a]

	5 μm thick (GaN-on-GaN)		10 μm thick (GaN-on-GaN)		15 μm thick (GaN-on-GaN)		20 μm thick (GaN-on-GaN)	
	Best	**Avg ± stdev**	**Best**	**Avg ± stdev**	**Best**	**Avg ± stdev**	**Best**	**Avg ± stdev**
Ideality factor	1.13	1.16 ± 0.03	1.16	1.23 ± 0.13	**1.11**	1.12 ± 0.01	1.12	1.14 ± 0.02
V_{on} (V)	**0.98**	0.96 ± 0.01	0.94	0.89 ± 0.02	0.96	0.93 ± 0.02	0.95	0.94 ± 0.01
$\phi_{B(IV)}$ (eV)	**1.09**	1.07 ± 0.02	1.00	0.95 ± 0.07	**1.09**	1.08 ± 0.01	**1.09**	1.06 ± 0.02
$\phi_{B(CV)}$ (eV)	1.35	1.22 ± 0.07	**1.37**	1.22 ± 0.06	1.31	1.20 ± 0.08	1.29	1.06 ± 0.02

[a]The values in bold font show the best values among the all measured devices.

characteristics are better than those obtained on GaN-on-Si SBDs as further discussed below. In contrast to the GaN-on-Si SBDs, there is no clear correlation between SBD characteristics and GaN thicknesses. We attribute this to the lower number of screw dislocations that result in negligible degradation of the leakage current. However, we observed some inhomogeneity in the SBD characteristics for GaN-on-QST and GaN-on-GaN that are due to the interface roughness of the non-optimized Schottky contacts.[27] With SEM, we observed that the long-range (several microns) surface roughness for GaN-on-QST substrates increased with thickness and believe that this increase in surface roughness led to an increase in the leakage current with film thickness as observed in Fig. 6(b). In addition, morphological changes within a given array contribute to the spread of the characteristics as further discussed for Figs. 7–9. Tables III and IV show that the lowest ideality factors in GaN-on-QST and GaN-on-GaN are quite similar; however, the uniformity and standard deviations of GaN-on-GaN are superior to those of GaN-on-QST. The ideality factors, barrier heights, and turn-on voltages for GaN-on-QST and for GaN-on-GaN SBDs were superior to those of GaN-on-Si SBDs. It is also important to note that the R_{on} and the currents obtained on the GaN-on-GaN SBDs did not scale with the different drift layer thicknesses further suggesting that series resistances (spreading resistance under the SBD dot) or contact resistances dominate the overall impedance of the SBD.

Figure 6 summarizes the I-V characteristics for the best devices for any given SAG thickness among the different studied substrates. For the thickest and best performance devices, the leakage current for the GaN-on-Si SBDs were still about 4 orders of magnitude higher than those of the

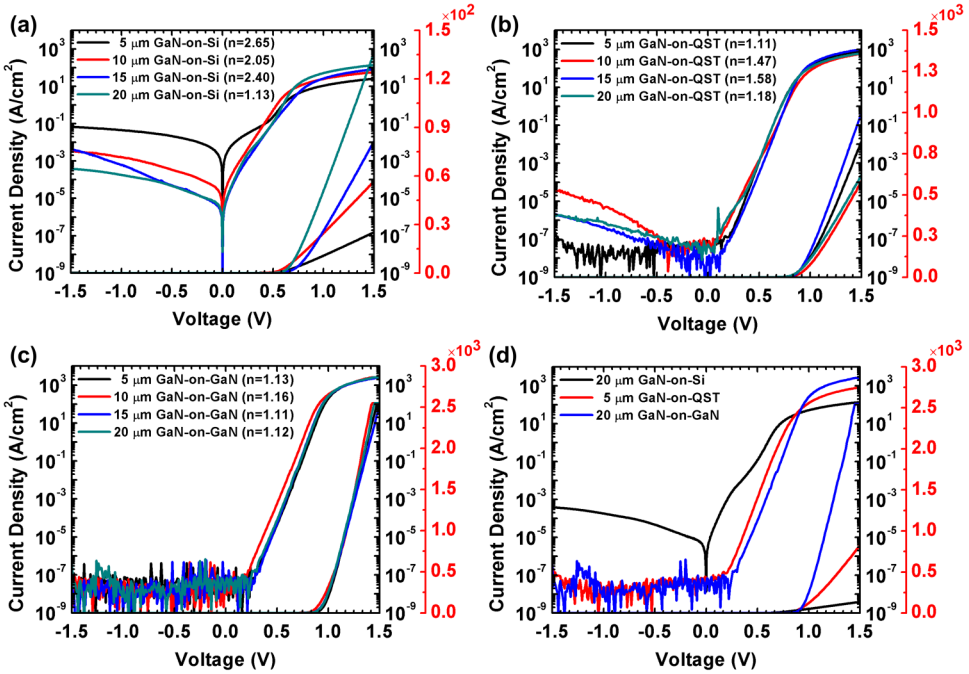

FIG. 6. Linear and semi-log scale I-V characteristics of the best SBDs for any given SAG thickness and on all studied substrates for (a) GaN-on-Si, (b) GaN-on-QST, and (c) GaN-on-GaN. (d) Comparison of the best performance devices from all three types of substrates.

other two substrates. Given that all structures are grown similarly and are expected to have similar surface leakage currents, the large leakage current in GaN-on-Si SBDs cannot be attributed to surface current leakage. We believe that the significant increase in the leakage current may come from the buffer leakage current at the lower and defective GaN/AlGaN layers near the interface with Si. The GaN-on-Si substrate contains only 500 nm n+GaN grown on top of 1.1 μm undoped

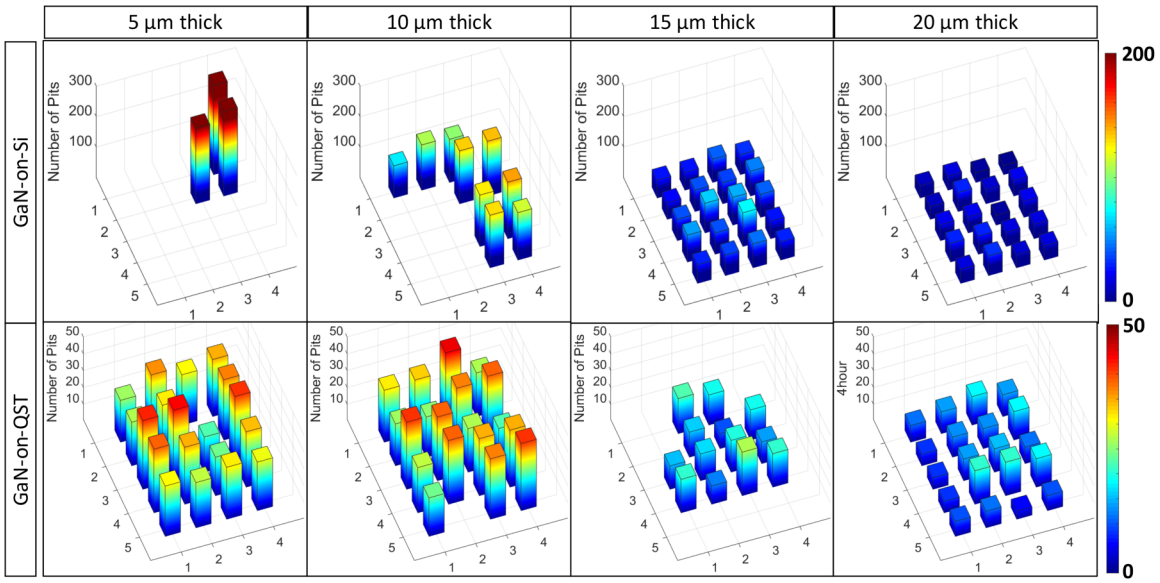

FIG. 7. 3D color map of etch pit counts for each dot in the SAG arrays on the GaN-on-Si and GaN-on-QST.

buffer and transition layer that is highly defective and used for current spreading under the SBDs such that the high density of defects prior to annihilation penetrated deeper into the GaN drift layer. In contrast, the 8 μm planar undoped buffer layer on the QST substrate readily contains the highly defective regions. Since we grew a 1μm thick n+GaN layer (Table I) on top of this buffer layer, current spreading under the SAG pattern has to be solely contained in the 1μm n+GaN layer. This shields the SBDs on QST substrates from current passage in the defective regions (contained in the 8μm buffer layer) at the substrate interface and therefore explains their much lower leakage currents. Engineering the current spreading layer doping concentration and thickness has been shown to be highly influential on the breakdown voltages of vertical devices.[28] Further improvement of the SAG layer growth and structure as well as the device structure for GaN-on-Si is required in order to achieve comparable levels of leakage current and overall SBD performance.

For all devices, the Schottky barrier heights measured by I-V are smaller than those obtained from C-V measurements. The differences in these values might come from the presence of an insulating layer or charges existing at the Schottky interface, deep impurity levels, image force barrier lowering, and edge leakage currents.[21,29,30] Consistently through both types of Schottky barrier height measurements, the barrier heights for GaN-on-Si SBDs were significantly lower compared to those made on other substrates which is most likely due to the higher leakage currents for SBDs made on Si.

The SAG GaN SBDs do not only depend on the growth thickness and substrate type but also on the location of the GaN dots within a given array. As noted above, there are 20 SAG GaN dots on the same substrate and the results were averaged over these 20 dots. Figure 7 shows the mapping of the defect densities over all dots in the array per substrate. As noted earlier from Figs. 1 and 2, the defect densities in GaN-on-Si and GaN-on-QST decreased linearly with increasing the thickness. However, the outermost GaN dots tend to show relatively lower defect densities than the dots near the center region, due to their larger height compared to the central ones. This higher growth rate originates from the enhanced Ga adatom collection at the outermost GaN dots since the effective dielectric mask spacing is large.[12] The ideality factor color map is shown in Fig. 8. As previously discussed, the ideality factor for GaN-on-Si samples decreased linearly with the thickness, whereas the GaN-on-QST and GaN-on-GaN were readily better and did not show a notable further improvement. As shown in Fig. 8, there is a trend that the outermost dots for a given array showed a higher relative

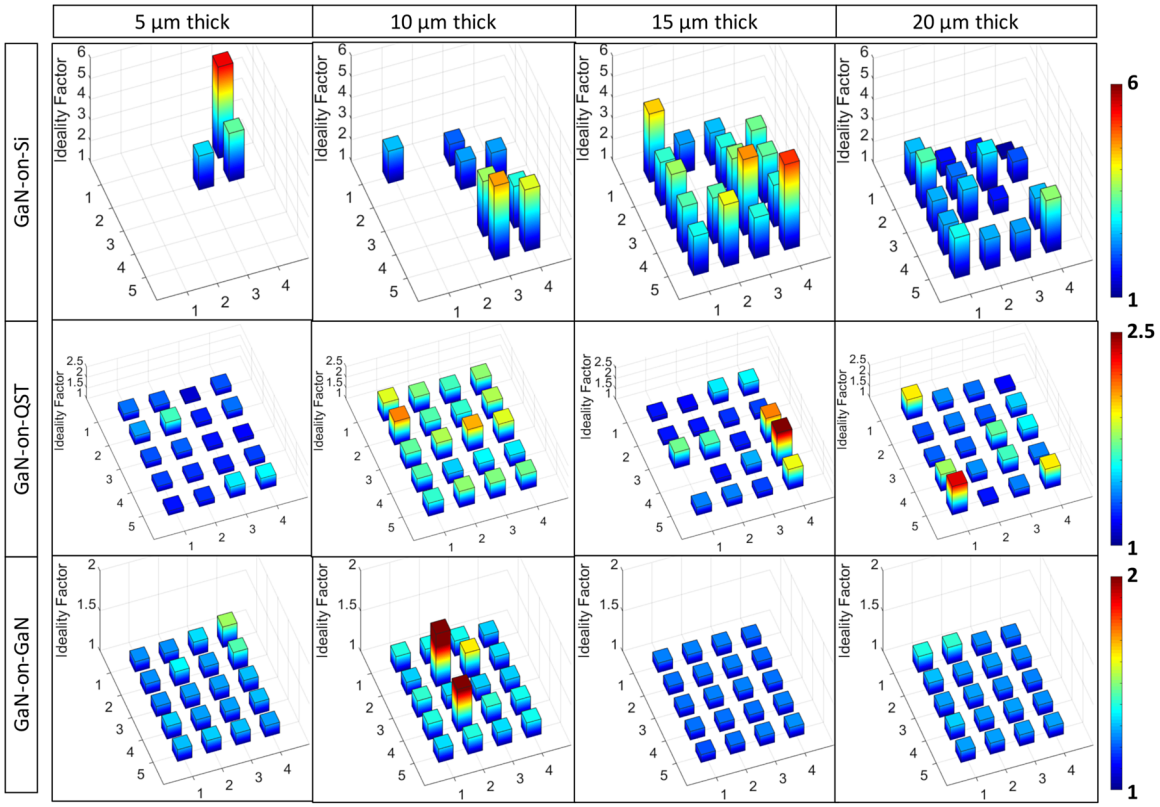

FIG. 8. 3D color map of ideality factors of each dot in the SAG arrays for the GaN-on-Si, GaN-on-QST, and GaN-on-GaN.

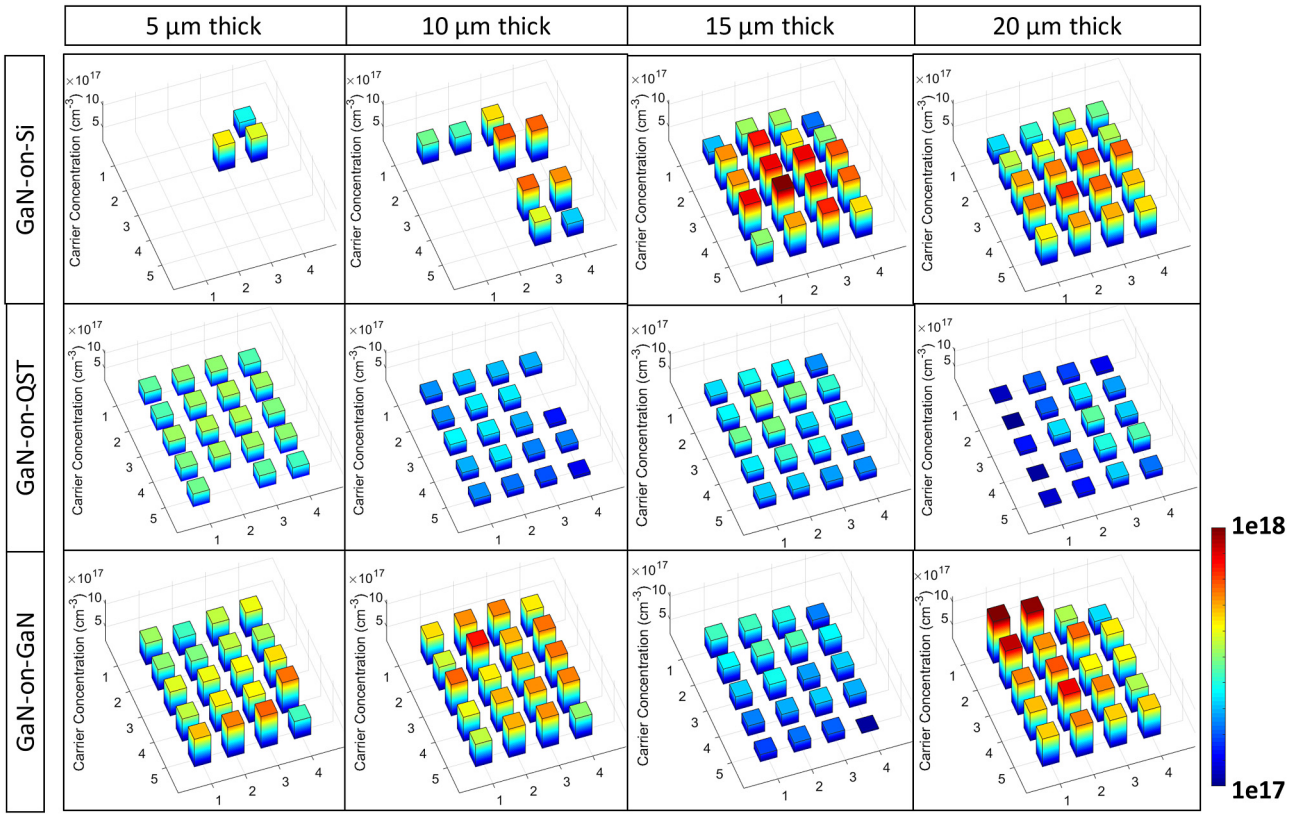

FIG. 9. 3D color map of carrier concentration of each dot in the SAG arrays for the GaN-on-Si, GaN-on-QST, and GaN-on-GaN.

ideality factor than those of the center dots. This discrepancy comes from the surface roughness due to the fast growth rate for the outermost dots that result in non-ideal Schottky contact interfaces. Even in the GaN-on-Si samples, a similar trend can be observed from Fig. 8, but the reduction of defect densities at the edges was much more significant than the influence of surface roughness on the ideality factor. Therefore, the average ideality factors reduced linearly by increasing the thicknesses. In terms of carrier concentration map in Fig. 9, there was no clear dependence of the thicknesses and substrates for the samples fabricated in this work. Prior works established the incorporation of unintentional dopants through the decomposition of the dielectric mask or due to the presence of residues from the dielectric mask at the regrowth interface.[31–33] For the incorporation of dopants from the dielectric mask, the collection volume for the outermost dots in the arrays is expected to lead to a larger incorporation of unintentional dopants, which contradicts our findings. The outermost dots have consistently resulted in the lowest carrier concentration. Therefore, we speculate that

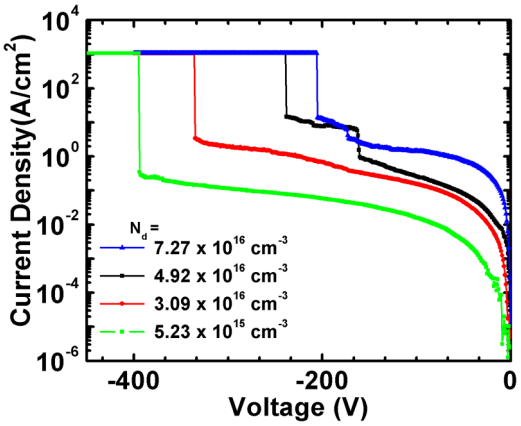

FIG. 10. Breakdown characteristics of GaN-on-QST SBDs fabricated on 20 μm thick drift layers with different carrier concentrations. All the SBDs have no edge termination.

TABLE V. SBD breakdown characteristics for GaN-on-QST substrates with different carrier concentrations.

	SBD 1	SBD 2	SBD 3	SBD 4
N_d	7.27×10^{16} cm^{-3}	4.92×10^{16} cm^{-3}	3.09×10^{16} cm^{-3}	5.23×10^{15} cm^{-3}
V_{BR}	−205	−239	−336	−395
W_{dep} at 0 V	116 nm	141 nm	178 nm	434 nm
W_{dep} at V_{BR}	1.67 μm	2.19 μm	3.28 μm	8.63 μm
E_{max}	2.47 MV/cm	2.19 MV/cm	2.06 MV/cm	0.92 MV/cm

the lower carrier concentration at the four corners can be explained by (i) reduced impurity incorporation by the fast growth, (ii) increased carbon concentration by the lower local V/III ratio due to the higher collection of Ga adatoms, (iii) slightly lower growth temperature near the edge of the substrate, etc. Further investigation by secondary ion mass spectrometry may be required to understand the origin of the unintentional doping impurity and the source of the low carrier concentration at the edge of the array.

Through a careful optimization of the growth conditions, we were able to achieve low carrier concentration in the drift layers of GaN-on-QST SBDs. The device breakdown characteristics for 4 SBDs are shown in Fig. 10 (SBD 1-SBD 4, respectively). The carrier concentrations for these SBDs were determined by the C-V measurement technique and are listed in Table V. The breakdown voltages (V_{BR}) increased with decreasing the carrier concentration as shown in Table V. These breakdown voltages agree with simple one-dimensional calculations of the maximum electric field at the Schottky contact ($E_{max} = qN_dW_{dep}/\varepsilon_0\varepsilon_s$, where W_{dep} is the depletion width at V_{BR}). The breakdown electric field was estimated to be 0.91-2.47 MV/cm which is within the range of breakdown fields (0.84 MV/cm–1.3 MV/cm)[34–36] obtained from state of the art GaN SBDs and lower than the theoretical value of 3.75 MV/cm, especially for the higher biased device (SBD 4).[37,38] This is mainly attributed to non-optimized device structure, especially lack of an edge-termination process and the presence of large fields at the edge of the contact with high applied voltage.

In summary, we compared the thickness and substrate effects on the material and device characteristics for SAG GaN-on-Si, GaN-on-QST, and GaN-on-GaN. The selective area growth of heteroepitaxial GaN on foreign substrates successfully reduced the significant number of dislocations by annihilating TDDs with thick GaN layer growth. The leakage current in GaN-on-Si decreased linearly with increasing thickness due to the reduction of screw dislocations. Thermally matched QST substrates showed promising device characteristics that were comparable to the devices fabricated on bulk GaN substrates. Even though the GaN-on-Si samples showed a comparable number of dislocation densities to the QST substrates, the leakage currents were still higher than those of the QST substrate and the GaN substrate. This may originate from the leakage in the thin buffer layers for the GaN-on-Si substrates. Further improvement of the epitaxial structure may further enhance the performance of the GaN-on-Si samples to be comparable to those on QST and GaN substrates.

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