Auxiliary Power Supply for Medium-voltage Power Converters: Topology and Control

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***Abstract*—This paper presents an isolated auxiliary power supply for medium-voltage power electronics systems. The proposed converter comprises two stages: a non-isolated ac/dc stage that connects directly to medium-voltage line, and an isolated dc/dc stage that provides 100 W output power at 24 V, with 10 kV isolation. The proposed modular ac/dc stage uses just one active semiconductor device per module, features an internal capacitor voltage balancing, and achieves power factor correction by employing predictive current control. High switching frequency operation of both converter stages enable reduction in system size and weight when compared to traditional low-frequency transformer-based approach. The proposed converter is simulated and its operation is validated experimentally on a 100 W prototype.**

Keywords—auxiliary power supply, medium voltage, modular multilevel converter, power factor correction, SiC MOSFET

I. Introduction

With recent developments in wide bandgap power semiconductor technology that can operate at higher switching frequencies, the MV power electronic systems are becoming an attractive option for various applications including solid-sate transformers [1], renewable energy systems [2] and transportation electrification [3]. A very important aspect of each of these systems is the auxiliary power supply, which powers control, measurement, and gate drive circuits of the system. One of the most challenging requirements for an auxiliary power supply in a MV power converter is to provide a high step-down ratio and high voltage isolation in a reasonably simple, compact, and cost-effective package. Two approaches can help meet these requirements [4]: the first relies on a low-frequency (50/60 Hz) potential transformer that connects directly to the MV grid. Although reliable and simple, the main disadvantage of this system is its substantial size and weight (the 2,400/120 V transformer weighs almost 30 lb.), and a more compact solution would be preferred if the overall system power density is critical. The other approach, which brings advantages of reduced weight and size, makes use of a dc voltage already present in the system, such as dc bus voltage or the voltage across one of the system capacitors.

Researchers reported a number of MV auxiliary power supplies based on the high-step-down dc/dc converters. A flyback converter proposed in [5], connects to 1600 V dc and provides 72 W at 24 V output, with 78.3% efficiency, by using 4,000 V Si MOSFET and a commercial controller. However, due to limited voltage blocking capability of commercial devices, the single-flyback approach is not suitable for input voltage levels above a few kilo-volts.

To overcome the issue of limited voltage blocking capability of commercial devices, researchers have proposed cascaded connection of flyback converters in [6]-[8]. An input-series flyback converter with multiple outputs is proposed and evaluated in [6]. Series-connected flyback converters operate synchronously using integrated flyback transformer and the converter is able to achieve input voltage sharing (IVS) without additional control. In this converter, the flyback switches need to operate synchronously in order to avoid voltage sharing issues between the modules. However, as authors point out, the input voltage sharing at higher power levels is worse than that of the input-series-output-parallel (ISOP) converters with additional IVS controllers. Larger input capacitors alleviate the IVS issue.

The auxiliary power supply proposed in [7] uses six ISOP-connected flyback converters. Bootstrap capacitors supply the six local drivers and a single controller IC drives all switches simultaneously. In order to achieve balanced voltage sharing between the input capacitors, the magnetizing inductance of each transformer needs to be carefully designed and well matched. Since a single IC controller supplies and controls all switches at the same time, a local driver for each switch eliminates the influence of the parasitic inductance of the long traces on the gate drive operation. If the gate charge of the switching devices is different, an additional bleeding resistor is necessary for each local driver to avoid the spurious turn-on due to the bootstrap capacitors' voltage unbalance.

Researchers identified several practical challenges of implementing ISOP topologies [8]. First, the series-connected converters are not identical, which can cause deviations in the input voltage and output current distribution. In the worst-case scenario, this could result in the input voltage of one of the converters converging to zero and input voltage of other converters increasing beyond the blocking voltage of semiconductor devices. Therefore, active voltage balancing control schemes are typically required for ISOP topologies. The converter proposed in [8] is based on a master/slave concept, where the master converter controls the output voltage, while the slave converters control the input voltages and output currents. The decoupled control for the master and slave converters help keep the input capacitor voltage well-balanced despite the inherent converter non-idealities.

Another proposed solution is a non-isolated power supply based on a tapped-inductor synchronous buck converter [9]. Six MOSFETs in series with specially designed non-isolated driver circuit make up a high voltage switch. The main advantages of the proposed topology are the autonomous operation, self-triggered turn-off procedure, and zero-voltage switching turn-on of high-voltage switch cell. Good voltage sharing between the series-connected MOSFETs of a high-voltage switch cell was achieved during the synchronous switch turn-on interval, but significant imbalance was observed during the high-voltage switch turn-off interval. A much tighter timing of the turn-off signal or larger snubber capacitors can improve the voltage sharing. However, using larger snubber capacitors increases the tapped-inductor energy storage requirement and reduces the efficiency and switching frequency, which was already relatively low (2 kHz).

In [10] we proposed a novel auxiliary power supply for medium voltage applications that connects directly to the MV ac input. The proposed topology consists of two stages: the first serves as a non-isolated ac/dc+PFC stage, while the second is a simple low voltage dc/dc converter that provides galvanic isolation. The first stage makes use of the proposed Multi-cell Series-parallel (MCSP) converter, which is a simplification of the MMSPC proposed in [11-12]. In comparison to [5-9], this method allows for the direct connection to the ac line which provides a generic solution for any MV application, where the dc bus may not be available; may be split into multiple independent capacitors (for example if a modular multilevel converter is used); or the dc bus may be inaccessible. In this work we expand on the basic topology presentation in following ways: 1) considerations of parameter sensitivity, effect of one-cycle delay, and design guideline for input inductor to ensure stability; 2) experimental results at medium voltage; 3) detailed comparison and verification of the proposed predictive control compared to the traditional PI control approach; and 4) detailed topology comparison with others proposed in the literature, arguing the novelty and advantages of proposed topology.

The rest of this paper is organized as follows. The proposed modular topology of the ac/dc stage is introduced and its basic operating principles explained in Section II. Section III analyzes the control strategy of the proposed system. In section IV, we consider one-cycle delay compensation on system stability. Simulations of the proposed system are presented in Section V, and the experimental verification is presented in Section VI. Section VII concludes the paper.

II. The Proposed Multi-cell Series-parallel Converter

A. The Multi-cell Series-parallel converter topology

The proposed step-down ac/dc converter was first introduced in [10]. The topology shares similarities with switched capacitor topologies, and with modular multilevel converters. The basic building block is shown in Fig. 1, and was derived from the modular multilevel series parallel converter (MMSPC) introduced in [11] and further evaluated in [12]. Details on the simplification of the MMSPC to the proposed MCSP converter are given in [10]. The proposed topology has the advantage of intrinsic balancing of its

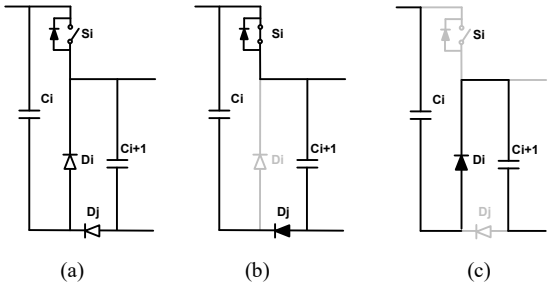

Fig. 1. (a) The basic cell of the proposed ac/dc converter, (b) Parallel connection of the capacitors, (c) Series connection of the capacitors

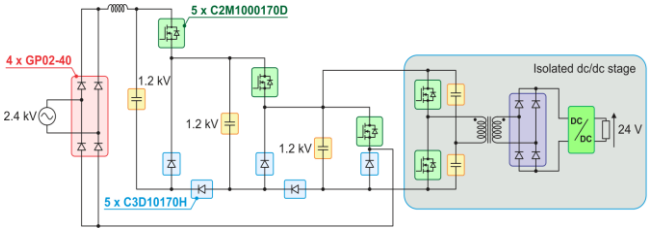

Fig. 2. Proposed auxiliary power supply topology based on proposed MCSP converter [10]

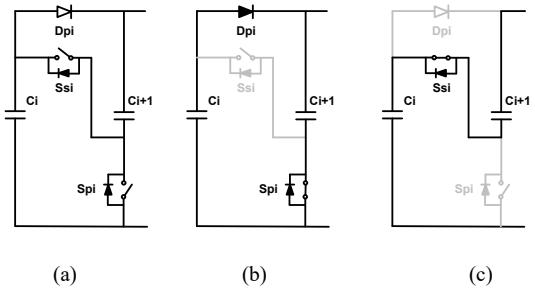

Fig. 3. Structure of basic SC cell, (b) Parallel (c) Series connection [13]

modules' voltage, which makes it ideally suited for the auxiliary power supply presented in this paper.

The MMSPC converter, which is generalization of the traditional MMC converter, allows both series (either positive or negative) and parallel connections between the module capacitors; this means that any voltage between 0 V and the sum of all module capacitor voltages can be produced at the terminals of the module string. Voltage balancing between different modules is achieved by periodically connecting the capacitors of adjacent modules in parallel, while still executing the correct modulation required by the application.

Although a conventional MMSPC is capable of bidirectional operation, its application as a power supply requires only unidirectional power flow: from high-voltage ac input to dc output. Considering the application, the simplified converter cell consists of two capacitors (Ci, Ci+1) to transfer the energy, only one active switch (Si), and two diodes (Di, Dj), as shown in Fig. 1. The topology of the proposed auxiliary power supply is shown in Fig. 2. Our approach, shown in Fig. 1 is similar, but simpler than the switched capacitor (SC) cell proposed in [13-15] (see Fig. 3), since it uses fewer switches to achieve the series and parallel connectivity.

Table I summarizes the proposed topologies. By comparing the number of components and characteristic, one can conclude that the proposed solution presents a viable alternative design. We should note that the proposed topology can connect to both an ac or a dc source, making the proposed topology a versatile solution to supplying auxiliary power.

TABLE I. TOPOLOGY COMPARISON

Metric	MCSP [Proposed]	Flying Capacitor [4]	ISOP Flyback [7]
Power MOSFETs (1.7 kV)	5	6	5
Power Diodes (1.7 kV)	5	5	0
Low Voltage Output Diodes	4	4	5
High Frequecny TRs	1	1	5
DC Link Capacitors	3	5	5
Input Voltage (ac Gird Approach)	2.4 kVac (Yes)	3.6 kVdc (No)	3.6 kVdc (No)
Balancing Characteristic	Self Balancing	Depends on Gate timing	Special TRs are required
Size, Weight	Good	Intermediate	Intermediate

Normalized to input 3.6 kVdc (2.4 kVac) and 1.7 kV devices from the references

TABLE II. BALANCING EFFECT ACCORDING TO SWITCHING STATE

Mode	Switching state	Balancing effect	Composed voltage	Connection
0	(1, 1, 1)	-	$0V$	3B
1-a	(0, 1, 1)	$V_{bus,2}, V_{bus,3}$		1S+2B
1-b	(1, 0, 1)	$V_{bus,1}, V_{bus,2}$	$1V_{bus}$	2P+1B
1-c	(1, 1, 0)	$V_{bus,1}, V_{bus,2}, V_{bus,3}$		3P
2-a	(0, 0, 1)	-		2S+1B
2-b	(1, 0, 0)	$V_{bus,1}, V_{bus,2}$	$2V_{bus}$	2P+1S
2-c	(0, 1, 0)	$V_{bus,2}, V_{bus,3}$		1S+2P
3	(0, 0, 0)	-	$3V_{bus}$	3S

(B: bypass, S: series connection, P: parallel connection)

TABLE III. OPERATING REGIONS AND CURRENT RIPPLE EQUATIONS

Region	Current Ripple
1	$\Delta i_{L\_up} = \frac{\lvert v_{in}\rvert}{Lf_s}(d-\frac{2}{3}),\ \Delta i_{L\_down} = \frac{v_{bus}-\lvert v_{in}\rvert}{Lf_s}(1-d)$
2	$\Delta i_{L\_up} = \frac{\lvert v_{in}\rvert - v_{bus}}{Lf_s}(d-\frac{1}{3}),\ \Delta i_{L\_down} = \frac{2v_{bus}-\lvert v_{in}\rvert}{Lf_s}(\frac{2}{3}-d)$
3	$\Delta i_{L\_up} = \frac{\lvert v_{in}\rvert - 2v_{bus}}{Lf_s}d,\ \Delta i_{L\_down} = \frac{3v_{bus}-\lvert v_{in}\rvert}{Lf_s}(\frac{1}{3}-d)$

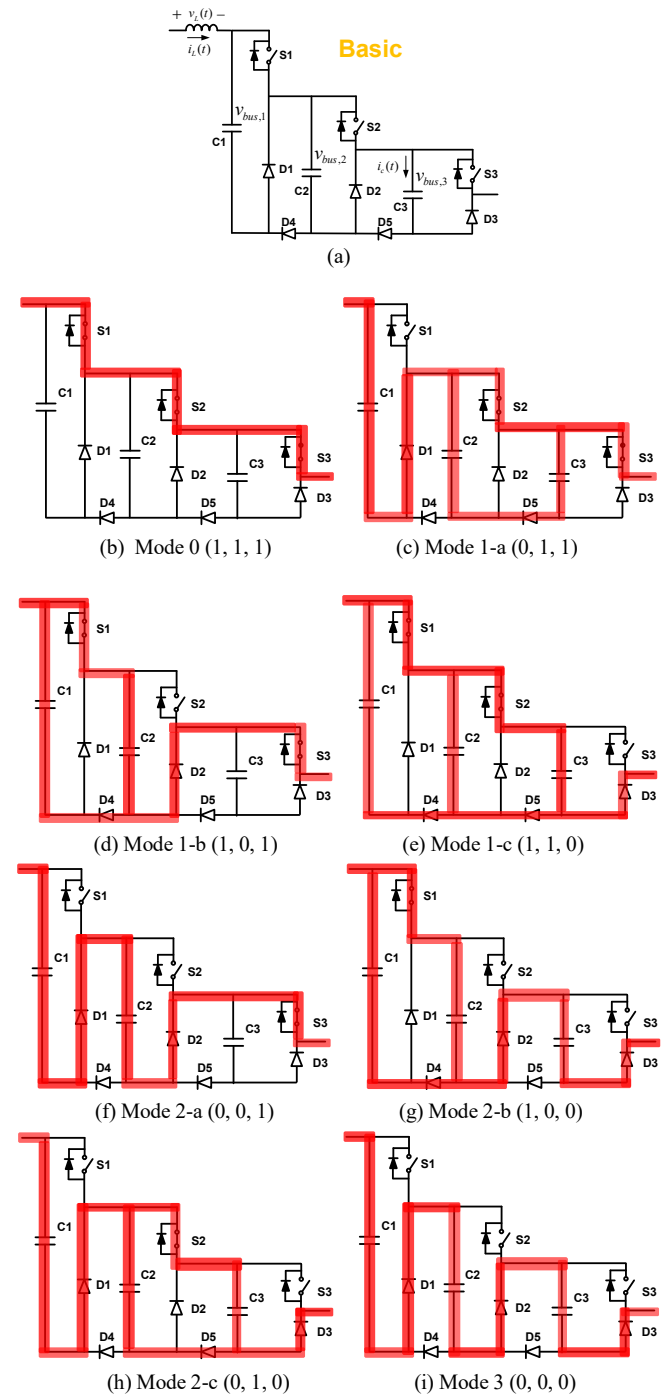

Fig. 4. Operating modes of the proposed MCSP converter: (a) converter topology, (b) Mode 0: 0 V, (c) Mode 1-a: 1 Vbus, (d) Mode 1-b: 1 Vbus, (e) Mode 1-c: 1 Vbus, (f) Mode 2-a: 2 Vbus, (g) Mode 2-b: 2 Vbus, (h) Mode 2-c: 2 Vbus, i) Mode 3: 3 Vbus

B. Operating principles of the MCSP converter

Referring to Fig. 4, depending on the combination of switching states of the switches S1, S2 and S3, the proposed converter can produce 0 V, $1V_{bus}$, $2V_{bus}$, or $3V_{bus}$ at the right-hand side of the input inductor by connecting the dc bus capacitors in series or in parallel, as shown in Fig. 4. Table II

lists four different operating modes achieved by the proposed converter.

Modes 1 and 2 have three possible switching states, where Mode 1-c is the most beneficial for the internal voltage balancing, since all three capacitors connect in parallel. Since parallel modes achieve voltage balancing, there is no need for an additional balancing algorithm. With natural capacitor balancing, only one dc-link voltage sensor is required for dc bus voltage control. In this work, we use the interleaved PWM scheme, depicted in Fig. 7, which results in three distinct regions defined by the amplitude of the input voltage. The interleaving scheme cycles through all states associated with a particular mode during a switching period and, as a result, all the capacitor voltages are balanced. In detail, Mode 0 and Mode 1 alternate at the switching frequency in Region 1 ($|v_{in}|<V_{bus}$). In the same way, in Region 2 ($V_{bus}<|v_{in}|<2V_{bus}$), the equivalent circuit is changing between Mode 1 and 2. In Region 3 ($2V_{bus}<|v_{in}|<3V_{bus}$), the modules' connections are changing between Mode 2 and 3. Referring to the equivalent circuits in the Fig. 4, Table III shows the equations of input inductor current.

III. The Control of the Proposed Converter

The predictive control approaches can be classified as deadbeat control, which eliminates the classic linear controller; and model predictive control (MPC), which is based on a cost function [16]. Finite control set MPC (FS-MPC) is an attractive approach that solves the optimization problem without requiring a modulation scheme, while considering the system constraints (typically current, voltage, active/reactive power and switching state). However, the FS-MPC requires defining a cost function, which may lead to implementation challenges since there is a need to determine the correct weighing factors in the cost function [16]-[17]. On the other hand, deadbeat control requires setting the desired current reference in the predictive model [17].

For the proposed topology, a simple constraint guarantees the generation of the optimal PWM modulation. In addition, in terms of control objectives, the proposed topology offers intrinsic dc bus voltage balancing feature, obviating the need for its inclusion in a cost function. Due to the unidirectional nature of the application, power factor control is a sufficient performance constraint (i.e. it is not necessary to set an active and reactive power command as in [16]-[17]). Moreover, even though the switching state in the cost function equation can assure a reduced number of switching commutations, the MPC relies on region detection for proper operation by determining the region boundary when multiple cells are used [18]-[19]. To further improve the MPC performance, we propose a simple predictive control that averts region detection with interleaved modulation scheme.

A. Predictive Control Strategy

The current in the medium-voltage, low-power, auxiliary power supply is expected to be very small, due to the high input voltage. To address the issue of dealing with a very large voltage and very small current, we propose a robust predictive controller adapted from [21]. The key innovation is the

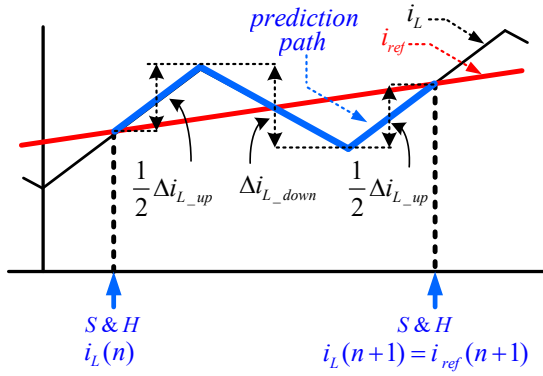

Fig. 5. Prediction path trajectory

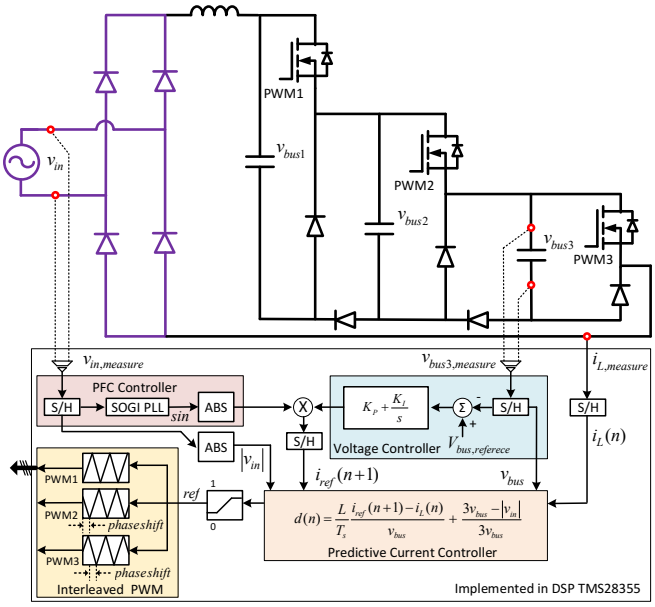

Fig. 6. Predictive control block diagram

selection of the of the prediction path, illustrated in Fig. 5, which simplifies the control to that of a simple boost converter. Equation (1) describes the prediction path, illustrated in Fig. 5.

$$i_L(n)+\frac{1}{2}\Delta i_{L\_up}+\Delta i_{L\_down}+\frac{1}{2}\Delta i_{L\_up}=i_{ref}(n+1) \tag{1}$$

Considering operation in Region 1 from Table III and substituting into (1), the duty cycle $d_1(n)$ in Region 1 is a function of input voltage, bus voltage, inductor current, inductance, sampling time, and current reference:

$$i_L(n)+\frac{|v_{in}|}{Lf_s}\left(d_1-\frac{2}{3}\right)-\frac{v_{bus}-|v_{in}|}{Lf_s}(1-d_1)=i_{ref}(n+1) \tag{2}$$

$$d_1=\frac{i_{ref}(n+1)-i_L(n)}{v_{bus}}\frac{L}{T_s}+\frac{3v_{bus}-|v_{in}|}{3v_{bus}} \tag{3}$$

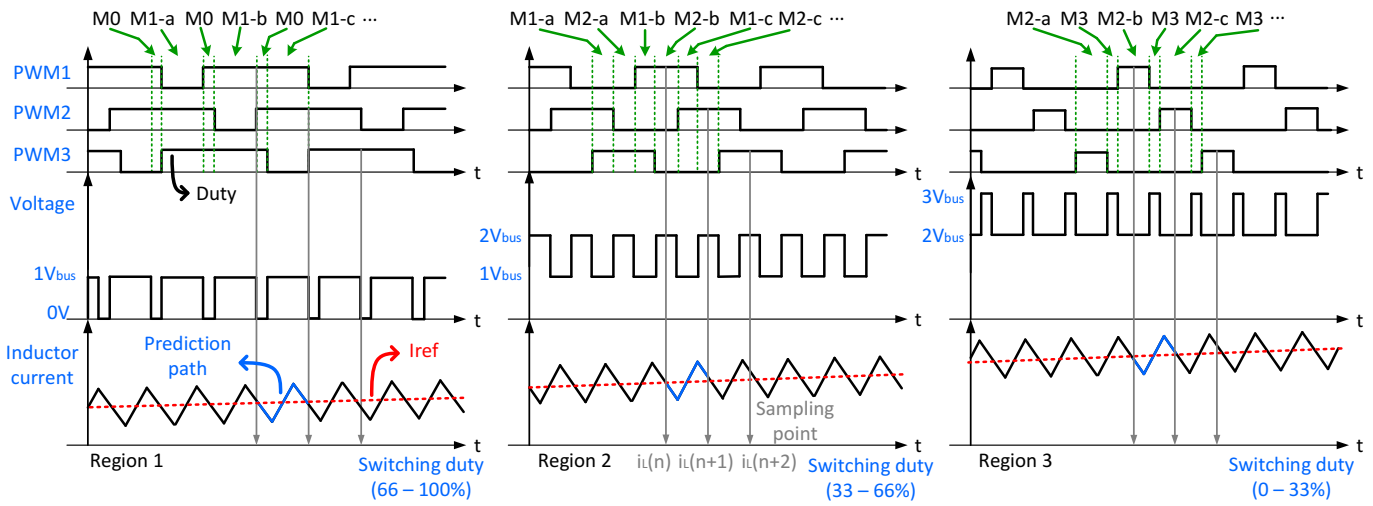

Fig. 7. Modulation, sampling and prediction path for the proposed converter with varying current reference depending on the region (left) (0 V, 1 Vbus) with mode 0 and 1; (middle) (1 Vbus, 2 Vbus) with mode 1 and 2; and (right) (2 Vbus, 3 Vbus) with mode 2 and 3

Similarly, by substituting the equations that describe operation in Region 2 in (1) results in:

$$d_2 = \frac{i_{ref}(n+1) - i_L(n)}{v_{bus}} \frac{L}{T_s} + \frac{3v_{bus} - |v_{in}|}{3v_{bus}} \tag{4}$$

Finally, in Region 3, the duty cycle equation becomes:

$$d_3 = \frac{i_{ref}(n+1) - i_L(n)}{v_{bus}} \frac{L}{T_s} + \frac{3v_{bus} - |v_{in}|}{3v_{bus}} \tag{5}$$

Consequently, it is evident that equations (3-5) are identical, and (6) applies in all operating regions:

$$d = d_1 = d_2 = d_3 = \frac{i_{ref}(n+1) - i_L(n)}{v_{bus}} \frac{L}{T_s} + \frac{3v_{bus} - |v_{in}|}{3v_{bus}} \tag{6}$$

Based on (6), a predictive current controller is implemented with conventional PI voltage controller and PFC control, as shown in Fig. 6. In this work, second order generalized integrator PLL algorithm [22] is utilized and only one capacitor voltage (V_{bus3}) needs to be sensed, due to natural capacitor balancing. Looking closely at the second term of (6), which is a static component (operating point of the converter), the duty varies from 1 to 0 as the input voltage $|v_{in}|$ goes from zero to its peak value close to $3v_{bus}$. Referring to Fig. 7, as the duty cycle varies from zero to 100%, the system naturally shifts from Region 1 (corresponding to duty cycle of 66 – 100%), Region 2 (corresponding to duty cycle of 33 – 66%) and Region 3 (corresponding to duty of 0 – 33%). Interleaving also ensures that in each region, the system cycles through all operating modes. For example, in Region 1, the Modes are repeated between Mode 0 and among Modes 1-a, 1-b or 1-c in sequence (see Fig 7). In consequence, depending on the pulse width and the first term of the (6), which is a dynamic component that regulates the current to the reference, the rectified voltage operated in three modes, as shown in Fig. 7. The current and voltage sampling occurs at the peak of the triangle carrier, with the sampling frequency equal to the effective switching frequency. The following equations show the applied phase shift and relation of frequencies.

$$phase\,shift = \frac{2\pi}{N}, \quad f_{S/H} = f_{sw,eff} = N \times f_{sw} = 1/T_s \tag{7}$$

Where, N = the number of modules.

B. *Mode Boundary and Critical Conduction Condition*

Since the proposed predictive controller assumes continuous conduction mode (CCM), our goal is to maintain continuous current whenever possible. In Region 1, the inductor current ripple is:

$$\Delta i_L = \frac{V_{in}}{2L}\left(d - \frac{2}{3}\right)T_s \tag{8}$$

Next, we derive the dc component of the inductor current in Region 1 based on the principle of capacitor charge balance:

$$I_L = \frac{V_{bus}}{3R(1-d)} \tag{9}$$

Finally, we find the conversion ratio by analyzing the inductor voltage waveform:

$$M(D) = \frac{V_{bus}}{V_{in}} = \frac{1}{3(1-d)} \tag{10}$$

Substituting (10) in (9) yields the expression for I_L becomes

$$I_L = \frac{V_{in}}{9R(1-d)^2} \tag{11}$$

Therefore, the conditions for CCM and DCM are:

$$I_L > \mathrm{V}i_L \quad for\ CCM \tag{12}$$

$$I_L < \mathrm{V}i_L \quad for\ DCM \tag{13}$$

Now, substituting the CCM solutions of (8) and (9) into (12), yields the relation for CCM operation:

$$\frac{2L}{RT_s} > 9(1-d)^2\left(d - \frac{2}{3}\right) \quad for\ CCM \tag{14}$$

Next, we represent the mode boundary in terms of the load resistance R,

TABLE IV. CCM-DCM MODE BOUNDARY FOR PROPOSED CONVERTER

Range	$R_{crit}(D)$	$\min_{0\le d\le 1}(d, R_{crit})$	
Region 1	$\frac{2L}{9(1-d)^2(d-\frac{2}{3})T_s}$	$d=\frac{7}{9}$	
Region 2	$\frac{2L}{9(\frac{2}{3}-d)^2(d-\frac{1}{3})T_s}$	$d=\frac{4}{9}$	$\frac{81}{2}\frac{L}{T_s}$
Region 3	$\frac{2L}{(1-3d)^2 dT_s}$	$d=\frac{1}{9}$	

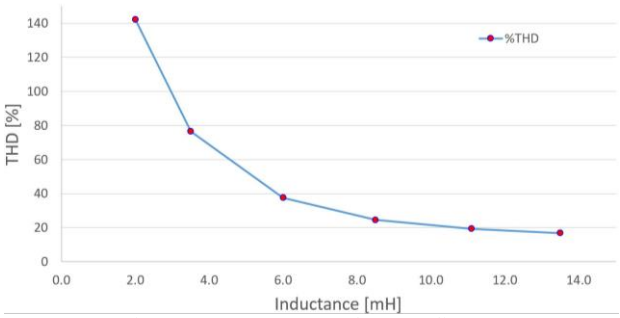

Fig. 8. Current THD vs. Inductance diagram

$$R_{crit}(D) < \frac{2L}{9(1-d)^2(d-\frac{2}{3})T_s} \quad for\ CCM \tag{15}$$

When we look into the envelope (U curve) of the equation (15), the $R_{crit}(D)$ (boundary points between DCM and CCM) should have a lower value than its boundary if the converter is to operate in CCM region. Therefore, the minimum value of the $R_{crit}(D)$ occurs when d is equal to $7/9$ in Region 1.

$$\min_{\frac{2}{3}\le d\le 1}(R_{crit}) = \left.\frac{2L}{9(1-d)^2(d-\frac{2}{3})T_s}\right|_{d=\frac{7}{9}} = \frac{81}{2}\frac{L}{T_s} \tag{16}$$

Following the same procedure, outlined in (8-16), yields the critical load condition of resistances $R_{crit}(D)$ in regions 2 and 3 respectively. The results are summarized in Table IV. The unified minimum value of $R_{crit}(D)$ helps to determine the inductance and load power condition in order to operate the proposed converter in CCM. Even though the proposed converter is designed for CCM operation, it is difficult to maintain CCM around the current zero-crossing, without making the inductor size exceedingly large. Thus, the converter will operate in mixed conduction mode, trading off the inductor size against the current total harmonic distortion.

Fig. 8 shows the input current THD versus inductance. Referring to the diagram above and the equations in Table IV, we selected an inductor of 8.5 mH. The proposed converter operates in mixed conduction mode (MCM) with reasonable input current THD. We note that the high THD of the auxiliary power supply is acceptable, given that for MV equipment, the ratings of the auxiliary power supply are typically 3-5 orders of magnitude smaller than the rating of the main device.

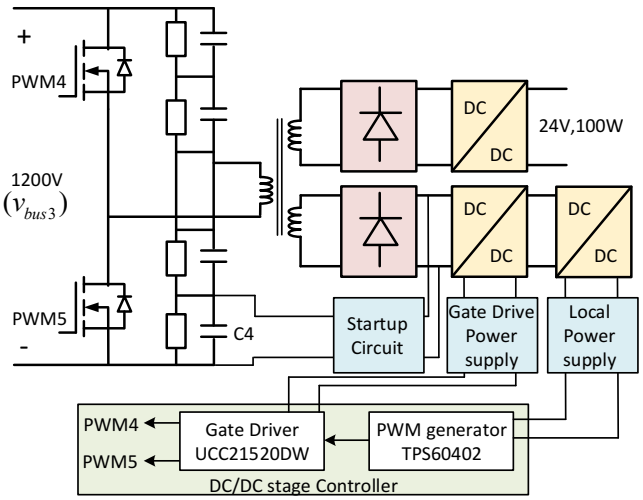

Fig. 9. Detailed configuration of the dc/dc stage

C. DC/DC Stage

A 1200/24V isolated dc/dc half-bridge (HB) converter is built, as shown in Fig. 9. The transformer is made using nanocrystalline vitroperm 500F core, with 190:13:6 turns in primary, secondary and tertiary windings respectively. The transformer was tested for isolation at 10 kV dc, which is applied for 10 minutes between any two windings. The primary side operates in open loop by using gate driver IC with 100 kHz switching frequency, whereas a switching regulator operates on the secondary side. The tertiary winding supplies power to the local control circuit and the gate driver after the startup transient ends. The startup circuit acts as a temporary power supply, since the tertiary winding is not initially energized.

IV. IMPLEMENTATION

A. Considerations on the One-cycle Delay

The practical implementation of the proposed system requires considering a one-cycle delay due to the time required for sensing analog values and performing the required calculations. In addition, in the carrier based PWM scheme, the optimal duty cycle at the instant [n] can only be applied after the instant [n+1]. Therefore, two-cycle prediction is introduced to mitigate the oscillation in the line current resulting from one-cycle delay [20]-[21]. Instead of [n+1]th instant duty cycle equation, in order to regulate the current at instant [n+2], we have used previous calculations representing the sampling and duty cycle calculations in step [n]. Now, the optimal duty cycle equation can be rewritten as (18) based on the two-step prediction path (17).

$$i_L(n) + \Delta i_{L\_up}(n) + \Delta i_{L\_down}(n) = i_L(n+1) \tag{17}$$

$$d(n+2)=\frac{i_{ref}(n+2)-i_L(n+1)}{v_{bus}}\frac{L}{T_s}+\frac{3v_{bus}-|v_{in}|}{3v_{bus}} \quad (18)$$

Since the predicted duty cycle takes one more switching period to calculate, all variables (v_{in} , v_{bus} and i_L from measurement circuits) need to be constant within two consecutive cycles. The drawback is that even if the sampling frequency is increased, it would still be difficult to achieve the fast dynamic response as in the case of one-cycle prediction. However, the auxiliary power supply application does not require a fast dynamic response.

B. Parameter Sensitivity

Equation (6) infers constant inductance in calculating the optimal duty cycle, assuming that the low frequency $|v_{in}|$ and v_{bus} are constant. In practice, inaccurate inductance estimation may cause oscillations and may affect the performance of the control system. To address this, we evaluate the effect of inaccurate inductance estimation, and determine its effect on system stability. Based on (6), the dynamic part of the duty cycle calculation is affected by the error in the inductance estimation. Therefore, the resulting duty cycle is defined for the ideal and the actual case as shown in (19) and (20):

$$d_{\substack{dynamic\\ideal}}=\frac{i_{ref}(n+1)-i_L(n)}{v_{bus}}\frac{L}{T_s} \quad (19)$$

$$d_{\substack{dynamic\\actual}}=\frac{i_{ref}(n+1)-i_L(n)}{v_{bus}}\frac{L_{est}}{T_s} \quad (20)$$

In (19) and (20) L is the nominal inductance, while L_{est} is its estimated value. The duty cycle difference between the nominal and estimated value is:

$$\Delta d(n)=d_{ideal}-d_{actual}=\frac{\Delta i_L(n)}{v_{bus}T_s}(L-L_{est}) \quad (21)$$

where $\Delta i_L(n)=i_{ref}(n+1)-i_L(n)$. To find the error in the inductor current at the sampling step (n+1), we define:

$$\Delta i_L(n+1)=\Delta d(n)T_s\cdot(\Delta i_{L\_up}-\Delta i_{L\_down}) \quad (22)$$

Where Δi_{L_up} and Δi_{L_down} are defined in Table III to represent the up and down slopes of the inductor current in three regions. Looking closely at the equations, we conclude that the ($\Delta i_{L\_up}-\Delta i_{L\_down}$) is always v_{bus}/L. Substituting into (22), the inductor current error at sampling step (n+1) becomes:

$$\Delta i_L(n+1)=\frac{\Delta i_L(n)}{v_{bus}T_s}(L-L_{est})\cdot(\frac{v_{bus}}{L})T_s$$
$$=\Delta i_L(n)\left(\frac{L-L_{est}}{L}\right) \quad (23)$$

After m switching periods, the inductor current perturbation becomes,

$$\Delta i_L(n+m)=\Delta i_L(n)\left(\frac{L-L_{est}}{L}\right)^m . \quad (24)$$

There are two cases when we interpret the stability of (24) as $m\to\infty$:

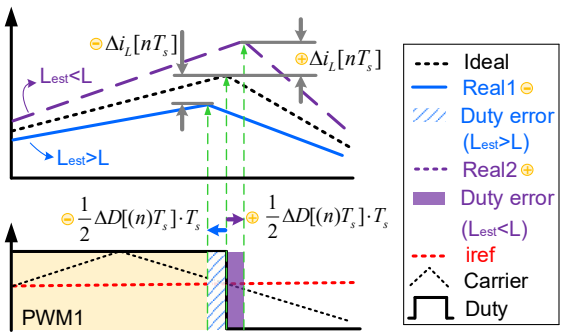

Fig. 10. Estimation of the inductance with parameter sensitivity

1) $L_{est}>L$: When the estimated inductance is larger than the ideal, the slope angle is lower than the ideal case, as shown Fig 10. In this case, setting $L<L_{est}<2L$, ensures that the current error does not diverge. One possible way is to set L_{est} as in [20]:

$$L_{est}=\frac{L\cdot d\cdot|v_{in}|}{d\cdot|v_{in}|-2\cdot L\cdot i_{sensed}} \quad (25)$$

However, in the proposed topology, (25) differs in all three operating regions, requiring region detection for L_{est} calculation, which negates the advantages of the proposed predictive controller.

2) $L_{est}<L$: In this case, the slope is slightly larger than the ideal one (see Fig. 10). Based on (24), when the inductance is underestimated, the system will remain stable without oscillations. Since the estimated inductance acts as proportional gain in predictive controller, its value controls the dynamic system response. Equation (20) shows that the dynamic performance deteriorates when the estimated inductance value is significantly smaller than the actual value; therefore, the estimated inductance is set to 90% of the nominal value, as in [21].

C. Circulating and inrush current

When a connection between two adjacent modules changes from series to parallel, an inrush current occurs. As an example, Fig. 11 shows that the mode change from 2-b to 1-c, results in V_{dc2} and V_{dc3} moving from a series to a parallel connection. Even though the proposed topology has the intrinsic voltage-balancing characteristic, in practice, component non-idealities result in slightly different voltages of dc-link capacitors. The imbalance of the capacitor voltages produces an inrush current (I_{sw2}) that is suppressed by the device on-resistance ($R_{on,2}$) and any parasitic inductance. Since the circulating current passes through the switching device, the devices need to be oversized to handle the circulating current. The circulating current magnitude will be a function of the device ON resistance, the parasitic inductance of the line connecting the storage elements, and the properties of the storage elements themselves. For example, the value of the capacitance that forms the voltage sources V_{dcn} will strongly influence the voltage differential that results

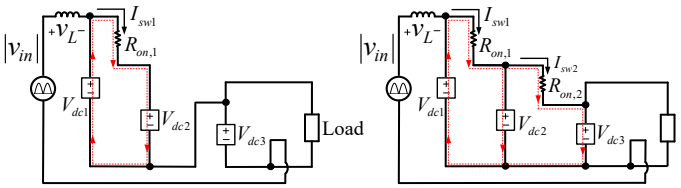

Fig. 11. Equivalent circuits including the on-resistors of switching devices.

during the series connection of the modules. Further, the equivalent series inductance and resistance (*ESR* and *ESL*) of the storage element itself will strongly influence the circulating currents, where the larger ESR and ESL will attenuate the circulating currents. Therefore, the system layout and component selection can effectively minimize the circulating currents in the system.

V. Simulation Results

Simulations of the converter operation, done in PLECS, validate the presented analysis, as illustrated in Fig. 12. Converter thermal models allow for efficiency and loss breakdown estimation, shown in Fig. 13. Figure 14 illustrates the advantages of the proposed system in terms of size and weight reduction in comparison to a potential transformer. Fig. 16 shows the boundary condition between current DCM and CCM, proving that the proposed converter operates in CCM for the majority of the half-cycle. Figure 17 compares the performance of the predictive current controller to a traditional PI controller. The traditional PI current controller operates in a stable condition with optimal THD based on [23]. A phase margin needs to be well designed, because a lower phase margin gives a faster transient response, but may also introduce instability in the transient response with undershoot or overshoot. Using that criteria, we designed the phase margin value to be in the range from 50 – 55° .

For the PI controller, proportional gain:

$$K_{pI,PI} = \left(\left| G_{PL,I}(f_{CI,PI}) \right| \cdot \sqrt{1 + \left(\frac{f_{ZCC}}{f_{CI,PI}} \right)^2} \right)^{-1} \tag{26}$$

where, $\left| G_{PL,I}(f_{CI,PI}) \right|$ is the magnitude of the plant transfer function as below:

$$G_{PL,I}(s) = K \cdot \frac{1}{1 + \frac{s}{\omega_{LPF}}} \cdot \frac{1}{\frac{s}{\omega_{id}}} \cdot e^{-sT_{DLY}} \tag{27}$$

Here, the coefficient K consists of peak value of the triangular carrier, full-scale range, and current sensing gain, while $\omega_{id} = V_o / L$ can be defined from a transfer function at the crossover frequency. The terms $f_{CI,PI}$ and f_{ZCC} are bandwidth and zero frequency of the current compensator respectively. The integral gain is expressed as:

$$K_{iI,PI} = 2\pi f_{ZCC} K_{pI,PI} \tag{28}$$

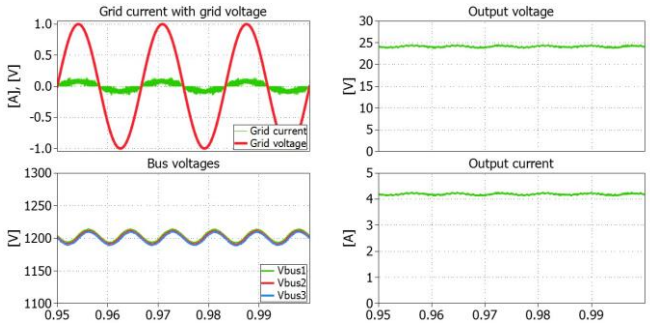

Fig. 12. Steady state response of the system, with 2400 V ac at the input and 24 V dc at the output, supplying 100 W to the resistive load.

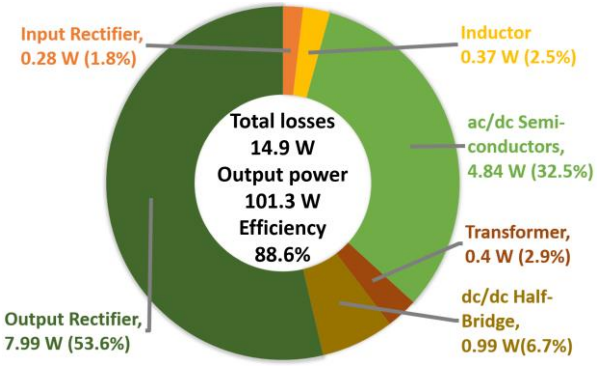

Fig. 13. Simulated system efficiency and power loss breakdown

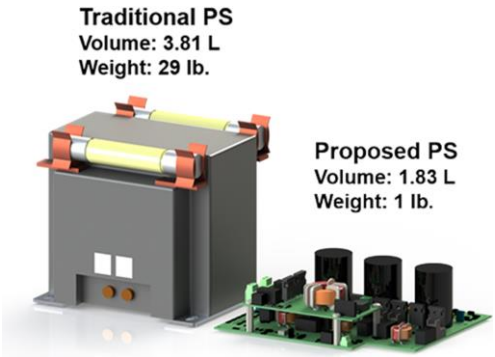

Fig. 14. 3D rendering of the proposed system compared to the traditional solution with potential transformer [10]

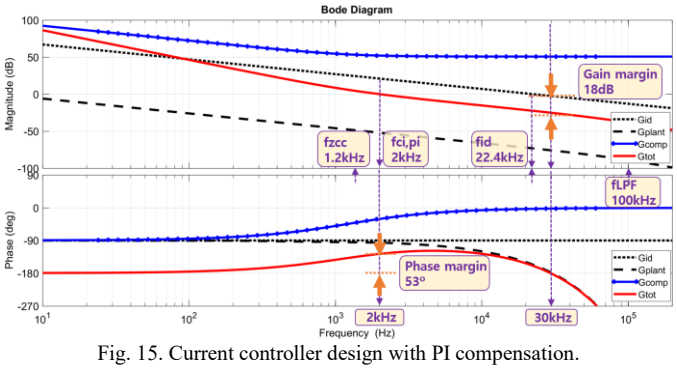

Fig. 15. Current controller design with PI compensation.

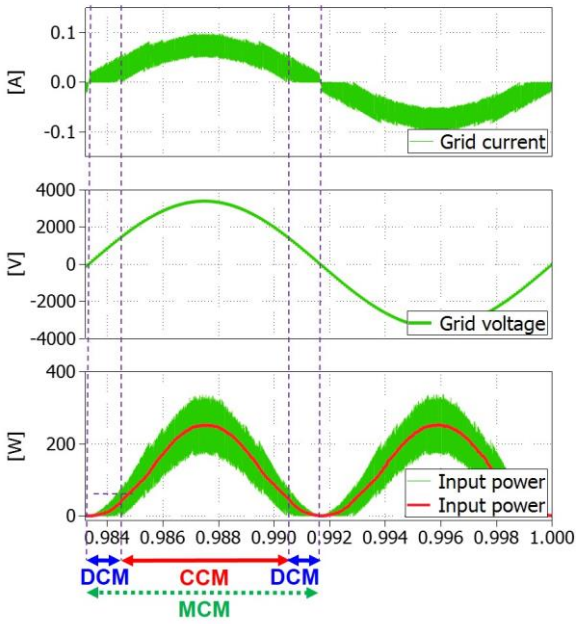

Fig.16. Simulation verification of MCM operation during one cycle

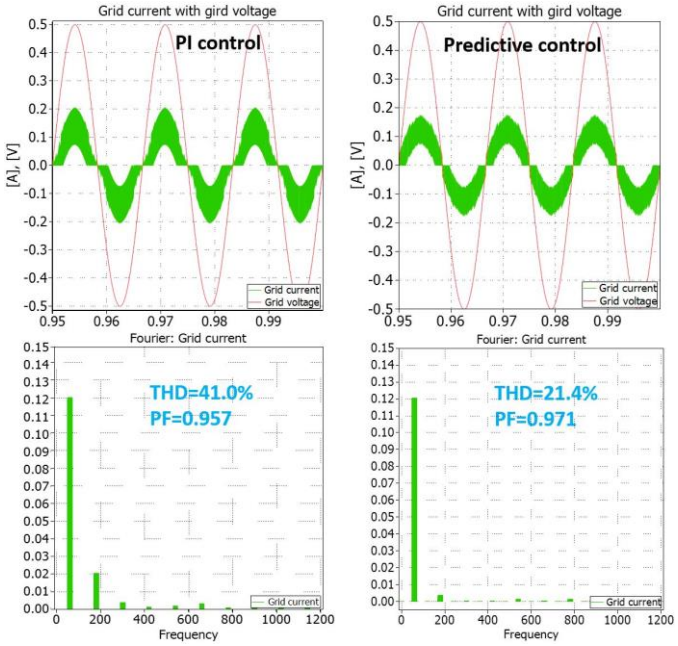

Fig. 17. Comparison of the proposed predictive control with a PI controller

In this case, $f_{CI,PI}$ is selected to be 2 kHz, and the PI gains are selected to be $K_{pI,PI} = 343.5$ and $K_{iI,PI} = 2590231$. In the z-domain the gains are $K_{plz,PI} = K_{pI,PI} = 343.5$ and $K_{ilz,PI} = K_{iI,PI} \cdot T_s \cdot (1/2) = 8.634$. Fig. 15 shows the bode plots of PI compensator with a phase margin of 53°

VI. Experimental Results

Experimental results were obtained using a prototype converter shown in Fig. 18. The semiconductor devices, passive components and operating values used in the prototype

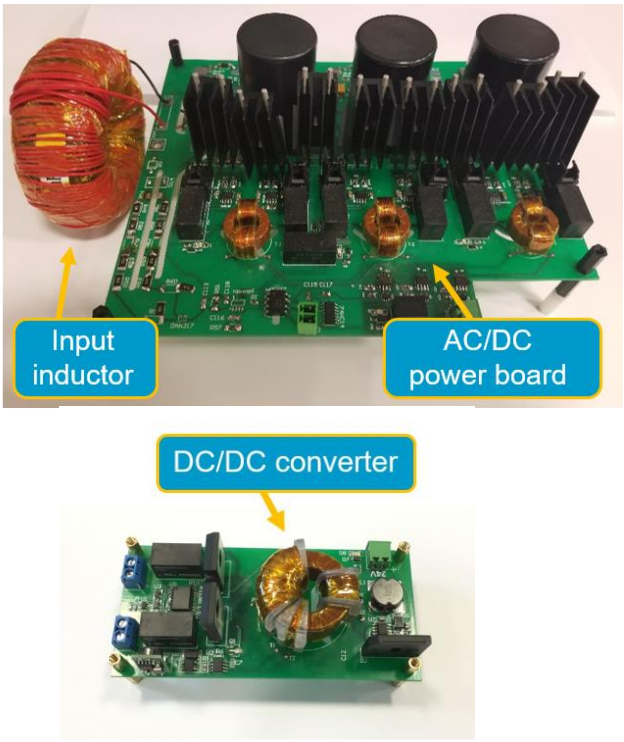

Fig. 18. The experimental setup: (top) ac/dc part of the system, (bottom) dc/dc part of the system

TABLE V. Parameters and Components

Parameter	Value	Component	Part number
v_{in} (Input voltage)	2400 Vrms (target)	$C_1 = C_2 = C_3$ (dc link cap)	UNL15W4P7K
v_o (Output volage)	24 Vdc	SiC MOSFETs	C2M1000170D
P_o (Ouput power)	100 W	SiC Diodes	C3D10170H
L_{in} (Input inductor)	8.5 mH	Input Rectifer Diodes	GP02-40
f_{sw} (Switching frequecny, ac/dc)	50 kHz	Ouput Rectifer Diodes	CDBC5100-G
f_{sw} (Switching frequecny, dc/dc)	100 kHz	Input Current Sensor	LA 25

converter are listed in Table V. The experiments are conducted separately for the ac/dc and dc/dc stages. For the ac/dc stage, the experimental results are obtained at 1.5 kV input ac RMS voltage with 125 W at the output as shown in Fig. 19 and 20. The PFC control performs well and the capacitor voltages are well balanced, as shown in Fig. 19 and 20. The output stage was tested at full voltage (input 1200 V dc) and rated output power of 100 W, and the waveforms are shown in Fig. 21. In order to compare the performance of the proposed predictive controller to the traditional PI controller, the tests are conducted in the proposed converter under same experimental conditions (500 V RMS input ac voltage and 30 W at the output). Test results for both controllers are shown in Fig. 22

and Fig. 23. The results are consistent with the simulations, shown in Fig. 17. With respect to input current THD, power factor and dc bus voltage ripple, experimental results show that proposed predictive control performs better than the PI controller. Due to the high voltage and extremely light load, the value of input THD is comparatively high. However, it is acceptable for an auxiliary power supply, since its current will be superimposed on the much larger input current of the medium-voltage converter.

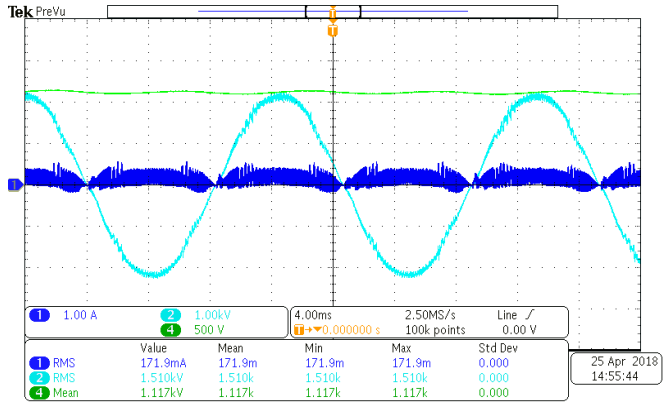

Fig.19. Converter input voltage and current with predictive control applied CH1: input current; CH2: input voltage; CH4: third bus capacitor voltage

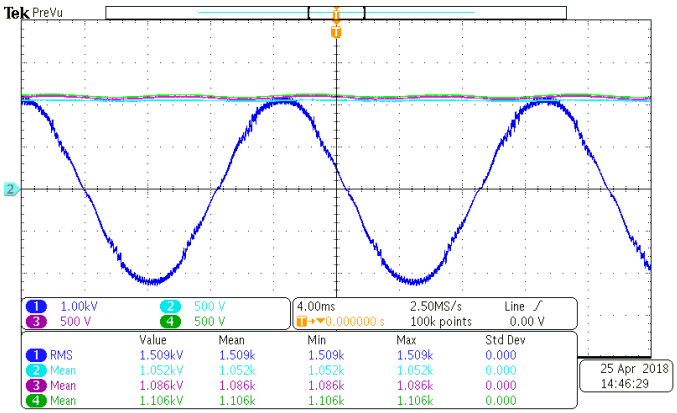

Fig.20. DC-link voltages with predictive control applied. CH2: third bus capacitor voltage; CH3: second bus capacitor voltage; CH4: first bus capacitor voltage

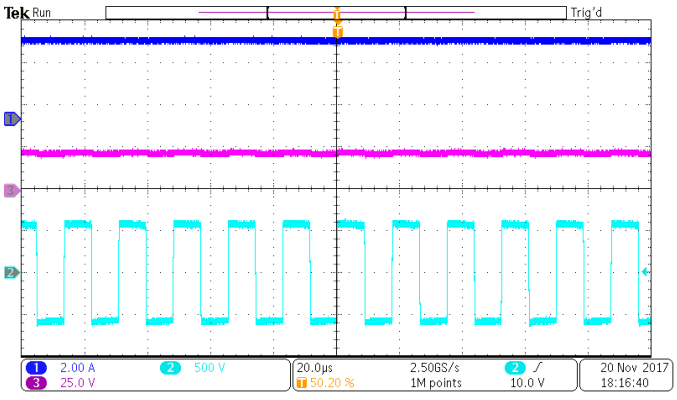

Fig.21. The experimental results for the dc/dc stage, with 1.2 kV at the input and 24 V at the output, supplying 100 W to the resistive load CH1: output current; CH2: output voltage; CH3: transformer primary voltage

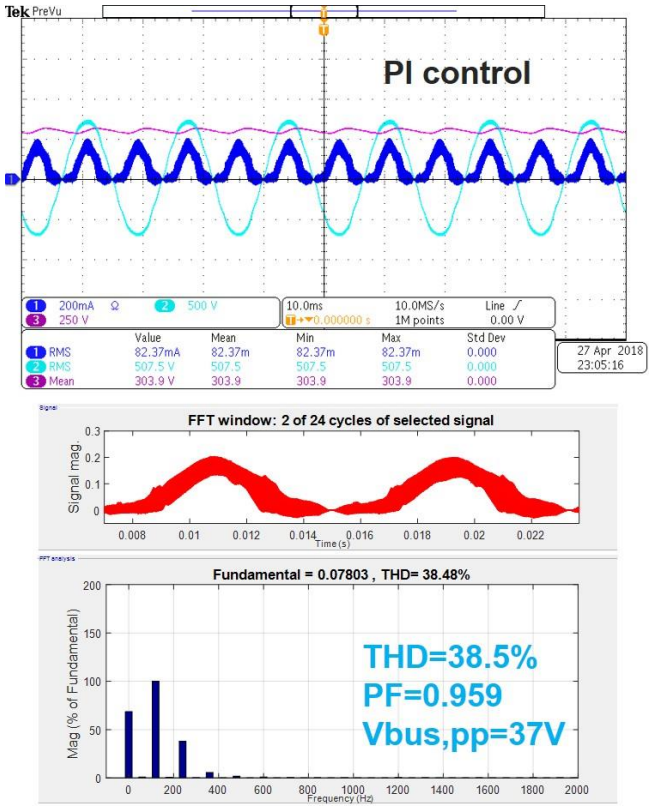

Fig. 22. The experimental results for the ac/dc stage with PI control at 500 V ac input voltage with 30 W load

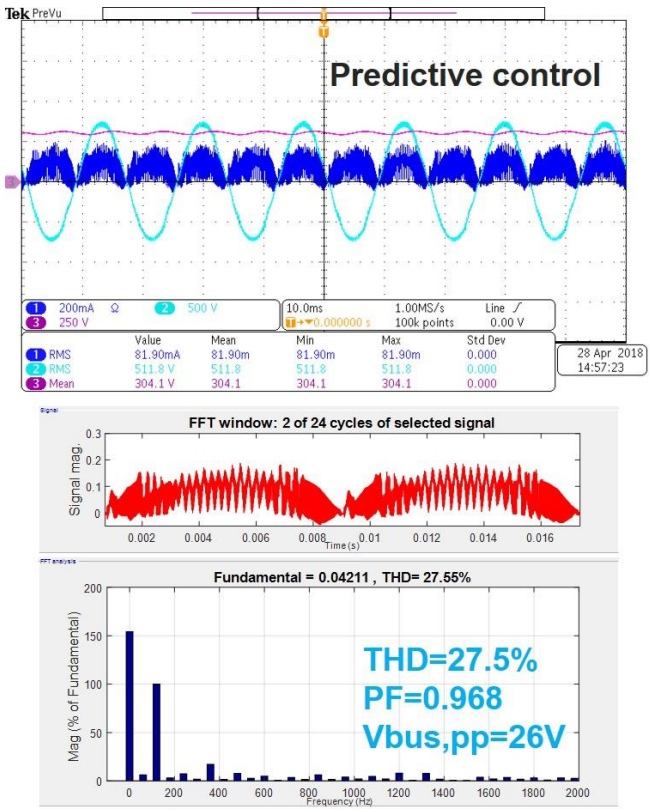

Fig. 23. The experimental results for the ac/dc stage with proposed predictive control at 500 V ac input voltage with 30 W load

VII. Conclusion

An auxiliary power supply for MV power electronics systems was presented in this paper. The proposed topology allows connection directly to the MV ac line, making the system more versatile, than the traditional converters that connect to the intermediate dc link, which can vary in voltage, and may be difficult to access in some topologies. The proposed topology uses a variation of the MMSPC topology, which provides effective semiconductor utilization, and requires no additional balancing algorithm due to the intrinsic balancing effect. Further, we have proposed and validated a predictive control that simplifies the control problem to that of a simple boost topology. In addition, a boundary condition analysis helps to determine the boost inductor value with reasonable input current THD and high power density. We demonstrated the system operation at 2,000 V and 100 W. The topology can be scaled-up to support higher MV distribution voltages by cascading the proposed basic cells.

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Disclaimer

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