Power and Data Integrity in Monolithic 3D Integrated SIMON Core

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***Abstract*—Monolithic 3D ICs have vertical interconnects that are comparable in size to local vias, thereby permitting extremely fine-grained vertical integration. SIMON, a lightweight block cipher, is designed and characterized at the Graphic Database System (GDS) level in two types of monolithic 3D design styles: transistor-level, where nMOS and pMOS transistors are split between tiers, and gate-level, where individual gates are partitioned among the tiers. The two 3D implementations as well as a 2D implementation are compared and characterized in terms of area and power. Furthermore, the effect of monolithic inter-tier vias (MIVs) on power and data integrity is analyzed for each custom 3D design. It is shown that power delivery for transistor-level monolithic 3D design is more challenging since all of the pMOS transistors (that are connected to the supply voltage) are located in the bottom tier where there are limited metal resources due to technology constraints.**

***Index Terms*—Monolithic 3D integration, power integrity, power delivery networks, ground bounce**

I. Introduction

Monolithic 3D (mono3D) integration, unlike other vertical integration technologies, provides unprecedented device and interconnect density [1]. Furthermore, mono3D integration is compatible with emerging memory architectures and device technologies. For example, carbon-nanotube field effect transistor (CNFET) logic and resistive random access (RRAM) memory layers have been implemented in mono3D SoCs [2]. Communication among the tiers is achieved through monolithic inter-tier vias (MIVs), which have comparable dimensions to local metal vias [3]. The security of mono3D ICs has recently received attention, with layout level techniques such as logic locking, as introduced in [4].

There are various design styles associated with mono3D ICs, as shown in Fig. 1. The primary approaches are transistor-level, gate-level, and block-level integration (which is not discussed in this work). Transistor-level mono3D involves placing nMOS and pMOS transistors within different tiers and represents the finest-grained integration. This design style requires the development of a new standard cell library, but allows for existing EDA tools (developed for 2D flows) to be used [5].

Gate-level integration allows for individual gates to be placed in either tier. This approach permits the use of existing 2D standard cell libraries, but requires a partitioning method and related EDA algorithms for cell placement [6].

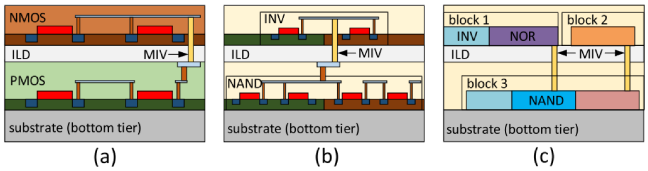

Fig. 1. Design styles for mono3D technology: (a) transistor-level, (b) gate-level, (c) block-level.

In this paper, a previously developed Mono3D PDK and cell library [7] is extended for gate-level integration, while supporting a custom design methodology. This methodology is used to design a lightweight encryption core, SIMON, in both transistor-level and gate-level implementations. SIMON is a lightweight block cipher designed for the Internet-of-things (IoT) devices and optimized for compact hardware implementations [8]. Several works have characterized data integrity for 3D ICs. For example, [9] develops a compact model for through silicon via (TSV) to transistor noise coupling, and [10] analyzes the signal integrity of a 3D implantable neurotransmitter sensing circuit. This work emphasizes mono3D power delivery architectures and focuses on analyzing power and data integrity for both transistor-level and gate-level mono3D implementations.

The rest of this paper is organized as follows. Section II provides a background of the design used. Section III discusses the various 3D power distribution networks analyzed in this work. In section IV, simulation results on ground bounce and power integrity are shown for different power distribution networks. Finally, the paper is concluded in Section V.

II. Background on SIMON

Most of the IoT devices are resource constrained in terms of both area and power [11]. SIMON is a Feistel based block cipher that is lightweight allowing for good performance regardless of platform (ASIC or FPGA) [12]. This paper is focused on a 32/64 SIMON implementation, meaning that 32 bits of plain-text are encrypted with a 64 bit key in 32 rounds.

A. Round Function

The operation of the round function for all configurations of SIMON is shown in Fig. 2. The input is put into two words

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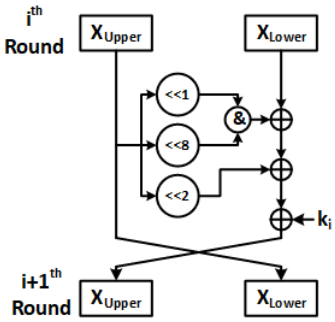

Fig. 2. Round function of SIMON.

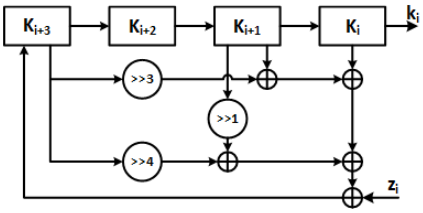

Fig. 3. SIMON key expansion for m=4.

and ran through a series of left circular shifts, bitwise XORs, and bitwise ANDs. At the end of each round, the two word blocks hold the input text for the next round. In each round, X_{upper} performs the operations to compute cipher text, while the current bits in X_{upper} are saved into X_{lower} for use in the next round. After a certain amount of rounds, depending on which configuration of SIMON used, the final cipher text is generated.

B. Key Expansion

The SIMON block cipher uses a different key in each round, as generated by the key expansion function. The operations used are bitwise XOR and right circular shifts. Also, a single bit round constant Z_i is used to eliminate slide properties, circular shift symmetries and introduce randomness [8]. SIMON has multiple key functions depending on what security configuration is chosen (the number of key words *m*), this paper uses the key expansion function for m=4. As shown in Fig. 3, K_i is the key for the current round, which is written to the highest block K_{i+3}. All of the keywords are then shifted one block to the right.

C. Bit Serialized Architecture

Different levels of parallelism (bit level, round level, and encryption level) can be achieved when designing a block cipher [13]. In this work, a bit serialized implementation is used from [14] to achieve the smallest area and lowest power consumption. This is a FIFO based implementation where the parallelism level is one bit of one round of one encryption engine per clock cycle. The round and key expansion functions for the bit serialized implementation are shown, respectively, in Fig. 4 and Fig. 5.

Three fully custom SIMON cores are developed in 2D, transistor-level 3D and gate-level 3D technologies to evaluate the effect of number of MIVs and various power delivery

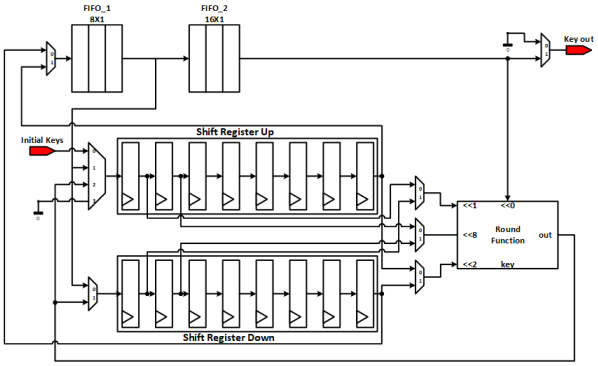

Fig. 4. Bit serialized round function.

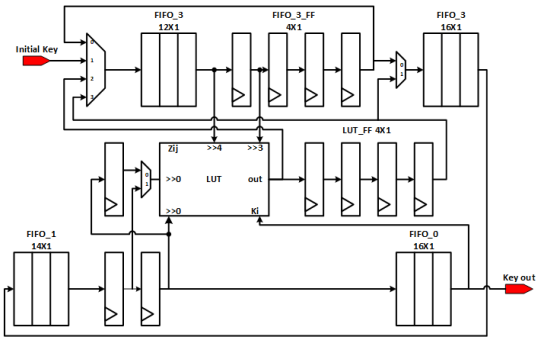

Fig. 5. Bit serialized key expansion.

networks. The three designs are also characterized in terms of area and power.

III. Proposed Implementation

The proposed implementations in this work utilize a fully functional PDK and cell library developed for transistor-level monolithic 3D ICs in the 45 nm technology node [15]. This library has been extended in this work to gate-level mono3D implementation. The primary focus is on power delivery and the effect of number of MIVs on the power supply noise.

It is important to note that current mono3D fabrication technology causes degraded devices in the top tier due to stringent process temperature requirements [16]. Thus, the pMOS devices of the transistor-level design are placed in the bottom tier (due to inherent lower mobility). The Mono3D library has two metal layers in the bottom tier and 10 metal layers in the top tier. Since SIMON is designed in full custom methodology, the partitioning of the gates among the two tiers (for gate-level mono3D) is achieved while considering overall area as well as connectivity among cells (interconnect length). The gate-level design uses the 45 nm standard cell library from *Nangate* [17].

Correct operation of the SIMON cores is verified for each implementation. The test vectors consist of initial keys `16'h 1918 1110 0908 0100` and plain-text `8'h 6565 6877`. The correct output of `8'h c69b e9bb` is obtained, as shown in Fig. 6 for the 2D implementation. Note that the encrypted output signals from the monolithic 3D implementations also demonstrate accurate results, but with degraded power/data integrity (depending upon the power network and

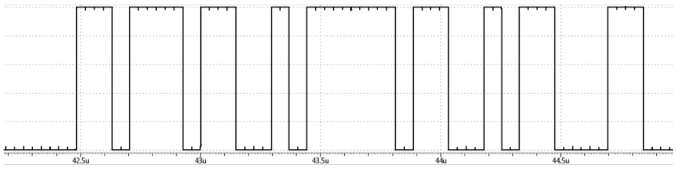

Fig. 6. Functional verification of the SIMON32/64 core in 2D implementation.

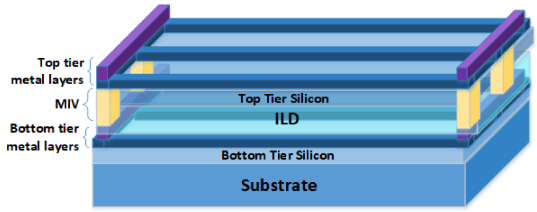

Fig. 7. Routed power network in monolithic 3D technology.

MIV number) due to ground bounce, as discussed in Section IV and illustrated in Fig. 11.

A. Power Delivery Networks in Mono3D ICs

The power delivery networks explored within this work are a routed network and power grid. The transistor-level mono3D design uses a routed network. The gate-level mono3D design is implemented with both a routed network and power grid. The number of MIVs within the power grid is varied for the gate-level mono3D design to evaluate the effect on power supply noise and ground bounce. Designing power delivery networks for monolithic 3D ICs is challenging due to limited metal resources within the bottom tier, which contains approximately half of the design.

In transistor-level mono3D, all of the pMOS devices are in the bottom tier, which has only two metal layers. Thus, it is not suitable for a power grid. Alternatively, a grid in the upper tier would need considerable vias and MIVs, thereby causing routing blockages. The routed network connects all of the power rails within the bottom tier and has MIVs and via-stacks run across the vertical sides of the power rails to connect with top tier since power pins are only available within the top tier. An example of a routed power network in mono3D ICs is shown in Fig. 7.

The power grid network in the gate-level implementation is designed with via stacks in the power and ground rails in the bottom tier and MIVs going to the upper metal layers in the top tier, but on both the horizontal and vertical rails within the design. The upper tier has a two layer grid, this approach reduces the overall impedance. An example power grid in mono3D ICs is shown in Fig. 8.

IV. Simulation Results

The bit serialized SIMON32/64 block cipher is designed in 2D, mono3D transistor-level, and mono3D gate-level, all using 45 nm CMOS technology. All of the circuits are powered with a DC source of 1 V and have a clock frequency of 13.56 MHz. The layouts of the 2D, transistor-level and gate-level mono3D implementations of SIMON are depicted in Fig. 9.

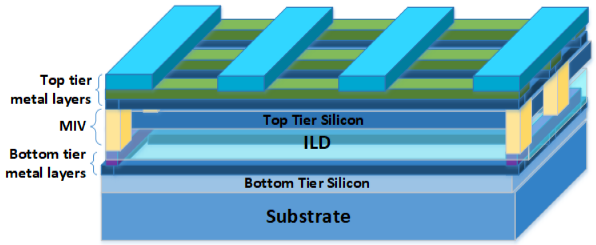

Fig. 8. Power grid network in monolithic 3D technology.

TABLE I
COMPARISON OF 2D, 3D TRANSISTOR-LEVEL AND 3D GATE-LEVEL MONO3D SIMON IMPLEMENTATIONS.

SIMON Core	Average Power	Area (μm^2)	Footprint (μm x μm)
2D Schematic	75.44 μW	N/A	N/A
2D Layout	87.29 μW	1638.24	41x40
Transistor-level Routed	86.71 μW	1289.01	32x20
Gate-level Routed	85.84 μW	1427.17	48x15
Gate-level Grid	86.38 μW	1427.17	48x15

A. Power and Area Characterization

The power consumption for all implementations of SIMON is listed in Table I. Since device power dominates due to relatively small dimensions, the power consumption is similar in all implementations. Transistor-level mono3D consumes approximately 10% less footprint than gate-level due to more fine-grained 3D integration. The transistor-level and gate-level designs have approximately 60% and 50% smaller footprints, respectively, than the 2D design. The 2D design is more than twice as large as the two 3D designs because of the custom design methodology prioritizing interconnect length over area.

TABLE II
PARTITIONING OF GATE-LEVEL SIMON

Tier	Average Power
Top	34.77μW
Bottom	40.67μW

B. Gate-Level Design Partitioning

Manual partitioning is used for the gate-level mono3D design since SIMON is a sufficiently small circuit. In order to verify that the gate-level design was evenly split, different power supplies were connected to the gates corresponding to each tier. At the schematic level, the average power of each tier was determined, as listed in Table II. The slight mismatch in bottom and top tier power consumption is due to prioritizing overall interconnect length during partitioning.

C. Power Supply Noise

Power integrity is an important concern for monolithic 3D ICs due to the fine grained MIVs permitting highly parallel and dense designs. The average power supply noise in the gate-level mono3D SIMON implementation with a power grid is 1 mV and the peak power supply noise is 67 mV. For the transistor-level mono3D implementation, these numbers are, respectively, 3 mV and 181 mV, as depicted in Fig. 10. This result is expected due to the power grid used in gate-level implementation. Since all of the pMOS devices are placed within the bottom tier (where there are limited metal resources)

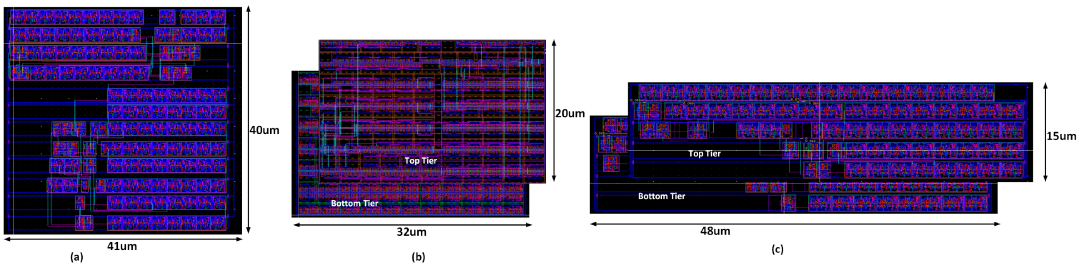

Fig. 9. Full custom SIMON layout Views: (a) 2D (b) transistor-level mono3D, (c) gate-level mono3D.

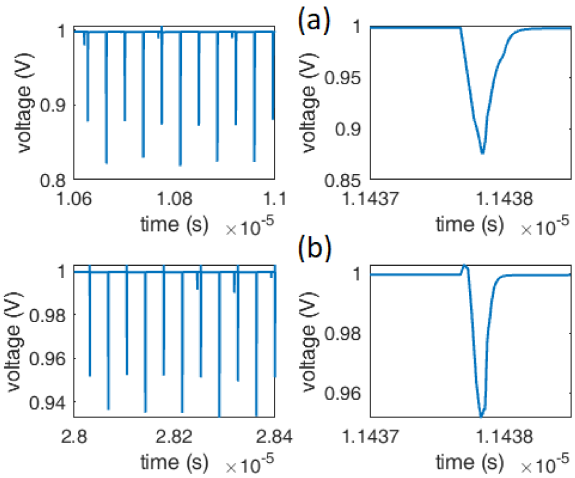

Fig. 10. Time domain power supply noise and zoomed view: (a) transistor-level, (b) gate-level.

in transistor-level mono3D, satisfying power integrity is significantly more challenging.

D. Effect of Ground Bounce on Data Integrity with Varying Number of MIVs

Significant ground bounce was experienced during the rising and falling edges of the clock signal. The number of MIVs was varied to see the effect of ground bounce on data signals (ciphertext). This analysis was performed for the mono3D gate-level design with the power grid. In each case, the MIVs are distributed homogeneously along the vertical sides of the power and ground rails. The negative effect of ground bounce on data signals was significantly reduced with approximately 21 MIVs. However, the effect of increasing the number of MIVs saturated once 150 MIVs were inserted, as shown in Fig. 11. Note that if the number of MIVs is not sufficient, significant voltage spikes can be observed, such as the 0.49 V at logic high. Thus, ensuring a certain number of MIVs connecting the power distribution networks among tiers is a critical component to mitigate the effects of ground bounce on data integrity.

E. Effect of Number of MIVs on Power Supply Noise

The number of MIVs in the power grid of the gate-level mono3D SIMON is varied and the effect on peak power supply noise is analyzed. In each case, the MIVs are distributed homogeneously along the vertical sides of the power and ground rails. When there are only 21 MIVs in the power

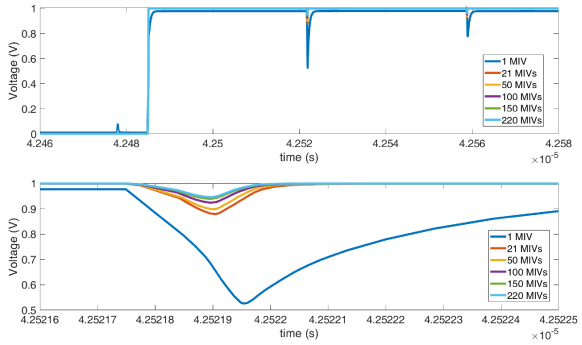

Fig. 11. The effect of ground bounce on output data (ciphertext) integrity (top) and zoomed view (bottom) as a function of number of MIVs.

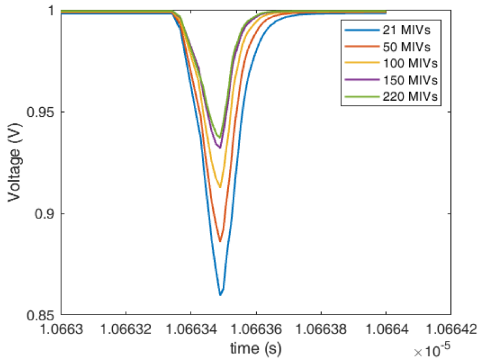

Fig. 12. Effect of number of MIVs on peak power supply noise.

distribution network, the peak power supply noise is 146 mV. Increasing the number of MIVs to 50 and 100 alleviates this issue by decreasing the peaks to 118 mV and 92 mV, respectively. The power supply noise approximately stabilizes when there are 150 MIVs in the PDN, where the peak power supply noise is 73 mV. With 221 MIVs, there is a peak voltage drop of 67 mV. Thus, the number of MIVs has significant impact on power integrity in mono3D ICs.

V. Conclusion

Three full custom implementations of the SIMON block cipher are realized in 1) conventional 2D technology, 2) transistor-level mono3D technology, and 3) gate-level mono3D technology. A routed network and power grid are developed and compared for the mono3D implementations. Simulation results demonstrate that it is more challenging to ensure power integrity in transistor-level mono3D ICs and the number of MIVs has significant impact on both power and data integrity.

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