Devices and Circuits Using Novel 2-D Materials: A Perspective for Future VLSI Systems

Giovanni V. Resta, *Student Member, IEEE*, Alessandra Leonhardt, Yashwanth Balaji, Stefan De Gendt, *Senior Member, IEEE*, Pierre-Emmanuel Gaillardon, *Senior Member, IEEE*, and Giovanni De Micheli, *Fellow, IEEE*

***Abstract*— Here, we review the most recent developments in the field of 2-D electronics. We focus first on the synthesis of 2-D materials, discussing the different growth techniques currently available and assessing their strengths and weaknesses. Moreover, we describe a possible roadmap to enable CMOS compatible integration of 2-D materials. We then shift our attention to 2-D devices and circuits and review the state of the art. Among the plethora of device concepts, we look closely at 2-D tunnel FETs (TFETs) and negative-capacitance FETs (NC-FETs) for low-power applications. We also put a particular emphasis on doping-free polarity-controllable systems that use electrostatic doping to eliminate the need for physical or chemical doping. We conclude with an analysis of simulations of scaled devices and discuss the possibilities enabled at circuit level by 2-D electronics.**

***Index Terms*— 2-D materials, beyond CMOS, doping-free, growth, integration, low power, polarity control, scaling, transfer, transition metal dichalcogenides (TMDCs).**

I. Introduction

RESEARCH on 2-D materials has experienced remarkable growth in the last decade. Major semiconductor companies are looking with interest at this novel class of materials, in the hope of addressing the shortcomings that are making scaling of silicon-based electronic devices increasingly difficult.

Despite the diversity in conduction properties and atomic composition, all 2-D materials are composed by covalently bonded in-plane layers that are held together by weak van der Waals interactions to form a 3-D crystal. Each layer has a uniform thickness ranging from 0.3 to 0.7 nm, depending on its atomic structure [e.g., graphene is composed by a single layer of carbon atoms, while, in general, a transition metal dichalcogenide (TMDC) layer with a general formula of MX_2 is composed by a transition metal (M), sandwiched between two chalcogen atoms (X)] [1], [2]. The weak van der Waals interaction is present in the out-of-plane direction thanks to the pristine surface of each layer, i.e., the absence of dangling bonds. This peculiar layered structure, together with certain optical and electrical properties, had already been discovered in 1947 for graphite [1] and in 1969 for TMDCs [2]. However, it was not until the pioneering work of Novoselov *et al.* [3] in 2004 that a graphite monolayer (now commonly known as graphene) was isolated and studied, effectively marking the beginning of 2-D electronics. However, the semimetallic nature of graphene prevents it to be used as the primary vehicle for novel digital transistors and circuits. Among the TMDC materials, the most studied are the ones formed by group IV [zirconium (Zr) and hafnium (Hf)] and group VI metals [molybdenum (Mo) and tungsten (W)]; however, other materials formed by different metals, such as platinum (Pt), rhenium (Re), and tin (Sn), are currently gaining interest. These materials show a semiconducting behavior and have exhibited excellent electrical properties [4]–[6], which will be further analyzed in Section IV. The presence of a sizeable bandgap (1–2 eV) makes the TMDC materials appealing for electronics applications, as it allows us to realize devices with low leakage level and high ON/OFF current ratios [7]–[10]. Among the other remarkable features of TMDCs, their layered structure provides 2-D films of controllable uniform thickness with dangling-bond-free interfaces. Moreover, their extreme thinness and low in-plane dielectric constant alleviate short-channel effects (SCEs) and drain-induced-barrier-lowering (DIBL) [11], [12], which are detrimental to device performance. The high effective mass of charge carriers (especially with respect to III–V materials) helps reducing direct source-to-drain tunneling at ultrascaled dimensions [13], [14], providing a better control of the device's OFF state by the gate terminals. The 2-D materials are appealing for future VLSI systems, and there are several areas in which they could bring novel functionality in electronic systems. However, several challenges still remain for high-quality growth and successful integration, and experimental demonstrations are still far from simulated devices performances.

This review is organized as follows. In Section II, we focus on the synthesis of 2-D materials. We highlight the different

Manuscript received February 6, 2019; revised March 18, 2019; accepted March 26, 2019. Date of publication June 4, 2019; date of current version June 26, 2019. This work was supported in part by the IMEC beyond CMOS Program and in part by the National Science Foundation (NSF) under Career Award 1751064. *(Corresponding author: Giovanni V. Resta.)*

G. V. Resta and G. De Micheli are with the Integrated Systems Laboratory, Swiss Federal Institute of Technology Lausanne (EPFL), 1015 Lausanne, Switzerland (e-mail: giovanni.resta@epfl.ch).

A. Leonhardt and S. De Gendt are with imec, B-3001 Leuven, Belgium, and also with the Department of Chemistry, Katholieke Universiteit Leuven, B-3001 Leuven, Belgium (e-mail: alessandra.leonhardt@imec.be).

Y. Balaji is with imec, B-3001 Leuven, Belgium, and also with the Department of Material Technology, Katholieke Universiteit Leuven, B-3001 Leuven, Belgium.

P.-E. Gaillardon is with the Department of Electrical and Computer Engineering, The University of Utah, Salt Lake City, UT 84112 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TVLSI.2019.2914609

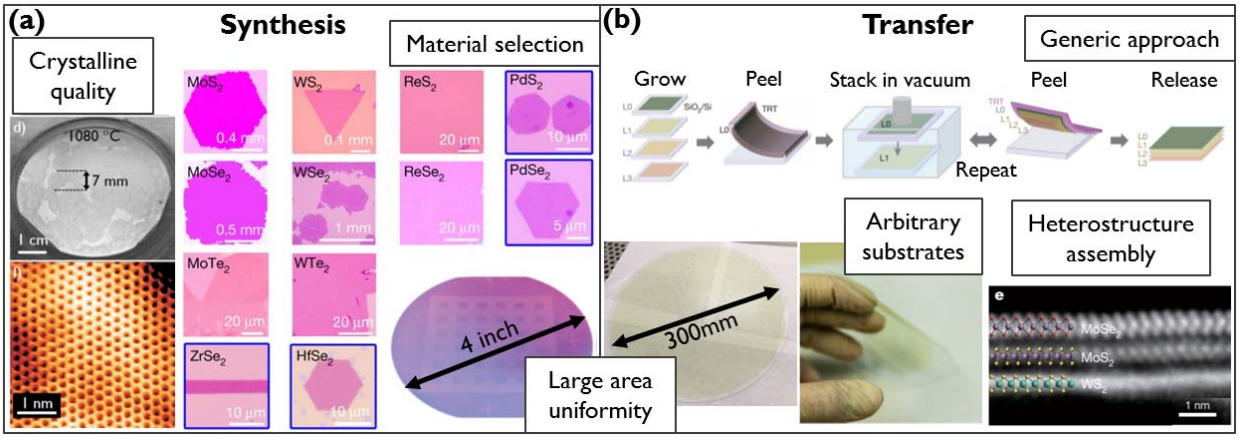

Fig. 1. Relevant metrics for synthesis and transfer of 2-D materials, with notable examples. (a) Crystalline quality and wide material selection are important to allow HP devices. (b) Transfer is a generic approach to allow integration in arbitrary substrates or assembly of heterostructures. Large area uniformity is essential to both synthesis and transfer, allowing low variability in material properties over wafer scales. Adapted with permission from [19], [46], [53], and [61].

approaches that are considered for the growth of 2-D materials on existing CMOS logic, back-end-of-the-line (BEOL) integration and discuss the need for the development of an efficient transfer technique. We also focus on the possibility of synthesizing lateral and vertical heterostructures, which are appealing for TFETs applications. In Section III, we describe a possible roadmap to enable CMOS compatible integration of 2-D materials, highlighting the main challenges that still have to be overcome. In Section IV, we shift our attention to 2-D devices and circuits and review the state of the art. Among the plethora of device concepts, in Section V, we look more closely at 2-D tunnel FETs (TFETs) and negative-capacitance FETs (NC-FETs) for low-power applications. Section VI is dedicated to doping-free polarity-controllable systems that use electrostatic doping to eliminate the need for physical or chemical doping on 2-D materials. Finally, in Section VII, we look at scaling opportunities for different types of 2-D devices and evaluate their projected performances.

II. Synthesis and Transfer of 2-D Materials

The first works with monolayer (1L) and multilayer (ML) 2-D materials were all done on exfoliated flakes, from the pioneering work on graphene [3], which led to a Nobel Prize in physics, to several demonstrations with TMDCs [7], [21]–[23]. Exfoliation results in high crystalline quality flakes that are used to understand the fundamental properties of 2-D materials and pave the way for future applications. The nondeterministic nature of mechanical exfoliation, however, leads to fluctuations in flake thickness, lateral size, and shape, all of which make it nonscalable to industrial integration. Logic circuits have been demonstrated on such exfoliated flakes [8], [24]–[27], but most reports involve a small number of devices and low level of integration. If the 2-D materials are to be considered for CMOS integration, large-area, uniform, and high-quality synthesis becomes a critical aspect to realize their full potential for future electronic circuits. Fig. 1(a) presents relevant metrics for the synthesis of 2-D materials, namely the crystalline quality (e.g., grain size) of the grown layers, the possibility of growing a number of different materials, and the large area uniformity of the synthetic layer. Two main synthesis approaches exist: growth directly on the device wafer, as often done for TMDCs [15], [17], [28] or growth on an optimized substrate, with a subsequent transfer step [18], [29] for integration. The optimal growth substrate changes with respect to the 2-D material grown, with metal films being used for graphene [16], [30] and crystalline hexagonal-boron nitride (h-BN) [31], while the best results for TMDCs have been obtained with sapphire [32], [33] or silicon dioxide (SiO_2) [34]. Direct growth is limited by the maximum temperature allowed at different process steps, especially when 2-D materials are cointegrated with a standard silicon CMOS technology. This poses a challenge since heterogeneous cointegration is an attractive route to enhance the speed or functionality of silicon chips by employing 2-D materials alongside the current architectures. Examples include using graphene boosting for interconnects [35], where the presence of a graphene layer leads to a resistivity reduction in the metal line, and 2-D TMDC transistors at the BEOL [36], which can provide further functionalities in the framework of 3-D scaling. However, if the growth is limited to 450 °C, for BEOL integration, the resulting material, particularly 2-D TMDCs, is highly defective [37], [38]. Besides prohibitive temperatures, the growth environment (corrosive or metal-containing gases) can also result in lower reliability of the dielectric where the 2-D material is grown. When using a dedicated growth substrate, the temperature limitations are lifted, which allows this approach to achieve high crystalline quality [30], [32]. The growth substrate can be carefully selected and tailored to achieve the best possible synthesis, where the layer-by-layer growth has been demonstrated with precise atomic control and reduction of strain and doping effects [39]. This temperature flexibility comes at the expense of an additional transfer step, which decouples the growth parameters from the device integration.

A transfer allows high-quality 2-D materials to be integrated into arbitrary substrates, which ranges from the standard CMOS wafers [either in the front-end-of-the-line (FEOL) or BEOL] to flexible substrates [18]. It is, in principle, a generic

approach, which allows the manipulation of different 2-D materials with the same method [20]. In the context of logic devices, uniform transfer of large-area 2-D materials is a key challenge. Transfer relies on interface interactions between the original substrate, the 2-D material, and the target wafer and is normally done using water- or acid-assisted intercalation [18], [29], [40], [41], which can introduce additional contamination or material modifications [42]–[44]. Understanding those interactions and being able to develop an all-dry process is critical to achieve a uniform and repeatable transfer, which has minimal impact on the 2-D material. By allying 300-mm growth capabilities with standard wafer bonding tools, a uniform 300-mm dry transfer was recently reported [19]. Fig. 1(b) shows the transfer process, with notable examples of each of these metrics. Besides transferring the 2-D materials onto the arbitrary substrates, understanding the interactions present after transfer and the impact of different substrates is also necessary. During this integration step, the 2-D material is transferred onto a wafer surface, which may have a series of nonidealities, such as roughness, topography, surface chemistry, and contamination, among others. Due to the atomically thin nature of the 2-D material, it is highly sensitive to the surrounding environment, and these nonidealities can cause unintentional doping, strain, and increased defectivity. This surface must be carefully engineered in order to result in stable and reliable transistor operation. Current understanding is that other 2-D materials are the ideal substrates for both graphene and TMDC devices [45]–[47].

In the context of transistor fabrication, heterostructures are inherently required, either between TMDCs and conventional metals and oxides or more exotic TMDCs/graphene, TMDC/hBN, or TMDC/TMDC heterostructures [22], [48]. These can be realized by the above-discussed two techniques, either *in situ* growth or assembly *ex situ* through transfer. The growth of vertical (WSe_2/SnS_2, MoS_2/WSe_2, WS_2/MoS_2, graphene/h-BN, and so on) [49]–[52] and lateral (WS_2/WSe_2, WSe_2/MoS_2, WS_2/MoS_2, and so on) [50], [53] heterostructures presents encouraging results. The main figure of merit in terms of heterostructures is atomically abrupt interfaces, being them vertical or lateral, since this is an important requirement for applications such as TFETs (as will be discussed in Section V-A). This is why, the *in situ* growth of the heterostructure—as opposed to assembly *ex situ*—is an appealing technique, where the presence of contamination at the interfaces is drastically reduced. In vertical heterostructures, atomically sharp junctions are easier to be obtained since the layered nature of 2-D materials can be exploited, but achievements in terms of growth techniques also allow atomic stitching of lateral heterostructures [53], [54]. Nonetheless, high-quality, large-area heterostructure assembly has also been demonstrated either by sequential transfers of different 2-D materials one on top of the other [55] or by using a 2-D material to pick up a different one [20], [56]. Beyond their use in established transistor architectures, heterostructures also present interesting physical phenomena, such as tightly bound excitons [57], [58] and plasmonic effects [59], [60], which can lead to exciting new device concepts in the future. These considerations in terms of growth and transfer of 2-D materials lead us to the discussion of what are the required milestones to be achieved for their integration with current CMOS technology.

III. Roadmap for CMOS Integration of 2-D Materials

When evaluating the integration of 2-D materials on future consumer and industrial applications, several different aspects should be taken into account. Their atomically thin nature and high mechanical strength make them perfect candidates for high-performance (HP) flexible electronics [25], [62]. Their electronic structure, featuring an indirect-to-direct bandgap transition, makes them promising for optoelectronics [63]. Their large surface-to-volume ratio results in great potential for both energy storage [64] and sensing [65] applications. While other roadmaps include these aspects [66], [67], we will primarily focus on the potential of 2-D materials as speed and functionality boosters alongside the standard CMOS technology. The 2-D materials are excellent candidates for this application due to their ultrathin and self-passivated nature and for featuring high mobilities even at the atomic thickness limit.

For that to turn into reality, the 2017 IEEE IRDS roadmap [68] mentions several requirements that have to be fulfilled, which are listed in the following. The list combines requirements for graphene (●), TMDCs (○), and shared requirements (◐). We would like to add that some of the aspects IRDS mention only for graphene, are also challenges for TMDCs, and are added as shared requirements in the list in the following:

- ● bandgap formation with high mobility and ON/OFF ratio greater than 10^4;
- ● armchair/zigzag nanoribbon formation;
- ○ improvement of contact resistance;
- ◐ large-area synthesis with low defect density;
- ◐ growth or transfer at controlled locations;
- ◐ growth or transfer of high-quality material at low temperature;
- ◐ thickness control;
- ◐ defect-free contacts;
- ◐ techniques for doping;
- ◐ characterization and imaging of nanoscale structures and composition.

Fig. 2 outlines the core steps of technology development for 2-D material integration in the CMOS process flow. With hundreds of 2-D materials currently being isolated or synthesized, selecting a few materials from this growing library becomes an important integration decision. Material selection can be done by benchmarking against current silicon technology, as proposed by Agarwal *et al.* [69], or can be done based on application-specific requirements, with TFETs being the most attractive example [70]–[72]. Another integration option is to select based on the stability of the material in ambient and process availability of high-quality large-area materials. Irrespective of how to select them, a few materials have already attracted special attention, such as graphene, MoS_2, WS_2, WSe_2, hBN, and black phosphorus (BP).

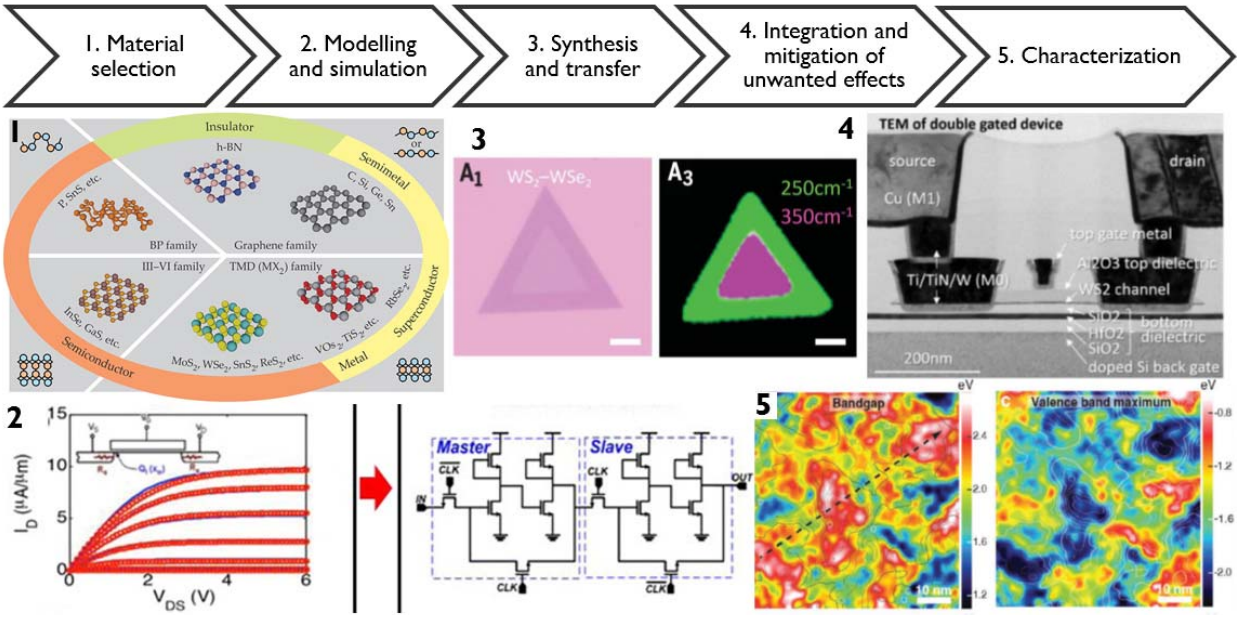

Fig. 2. Roadmap for integration. Required steps for 2-D material to reach product stage. Adapted with permission from [19], [46], [53], and [61].

Modeling and simulation are the key elements for device and circuit design and fabrication and will be the focus of Section VII. Modeling is essential to understand device functionality, especially the impact of contact barriers, nonidealities, and possible defects on the transistor functionality [61], [73]–[77]. Important advances are being made in terms of fundamental material and device understanding [78]–[80]. Besides the important design guidelines that it generates, simulation tools are also essential ingredients if widespread circuit design with 2-D materials is the objective.

Synthesis and transfer, as discussed in detail in Section II, are challenging steps, which aim to achieve materials with a high crystalline quality, controlled thickness at the atomic scale, and integration with arbitrary substrates. Encouraging results from the growth of large single crystals and precise heterostructures [53] were demonstrated. When 300-mm integration is the goal, two main routes for transfer emerge: wafer-to-wafer transfer on complete 300-mm blankets [19] or die-to-wafer positioning of small crystals [81].

The integration core step includes not only upscaling successful lab-scale processes to industry-compatible 300-mm platforms but also mitigating of unwanted effects arising from the substrates, encapsulating materials, or device processing. Some works have explored the mitigation of unintentional doping and strain for both graphene and TMDCs [44]–[46]. Linked to integration is also the precise modulation of the electrical properties of the devices, such as threshold voltage (V_{TH}) and polarity. The precise control of V_{TH} of different devices is critical for correct circuit operation, and while great efforts have been made in the direction of doping, a standard is yet to emerge [82]–[85]. Furthermore, while some materials present either n-type or p-type conduction, others combine both, opening interesting routes for doping-free devices and optimized circuit design, as will be discussed in depth in Section VI [27], [86], [87].

For most of the processing steps, characterization techniques are essential to assure yield and reliability. While the current 2-D material characterization allows probing several properties, wafer-scale characterization techniques are still not matured. The core techniques used to probe 2-D material quality are Raman spectroscopy, photoluminescence, and atomic force microscopy [88]–[90]. Techniques to understand interface properties are not fully developed and are essential for achieving reliable and stable transistors [46], [91], [92]. In-line metrology will surely need additional techniques in order to fully probe the reduced dimensions and specific properties of 2-D materials. Importantly, the development of a standardized characterization toolkit capable of measuring from material quality to electrical characteristics, including interface properties, is still pending.

In conclusion, in order to realize the full potential of 2-D materials as boosters in VLSI systems, several technological developments are still necessarily spanning from a better quality of the grown material to the development of an efficient transfer technique to the upscaling of processes to 300-mm platforms. However, the recent progresses shown in the understanding of the properties of 2-D materials and the demonstration of novel devices keep the research field vibrant and appealing to industries and universities. We now review the state of the art for 2-D electronics based on TMDCs and graphene providing insights into the most recent developments in the field.

IV. State of the Art for Experimental Devices and Circuits

Since the first demonstration of a monolayer (1L) MoS_2 transistor with high mobility and high ON/OFF current ratios in 2011 by Radisavljevic *et al.* [7], the field of 2-D electronics has gained worldwide traction with a constant increase in the number of publications and a growing interest of

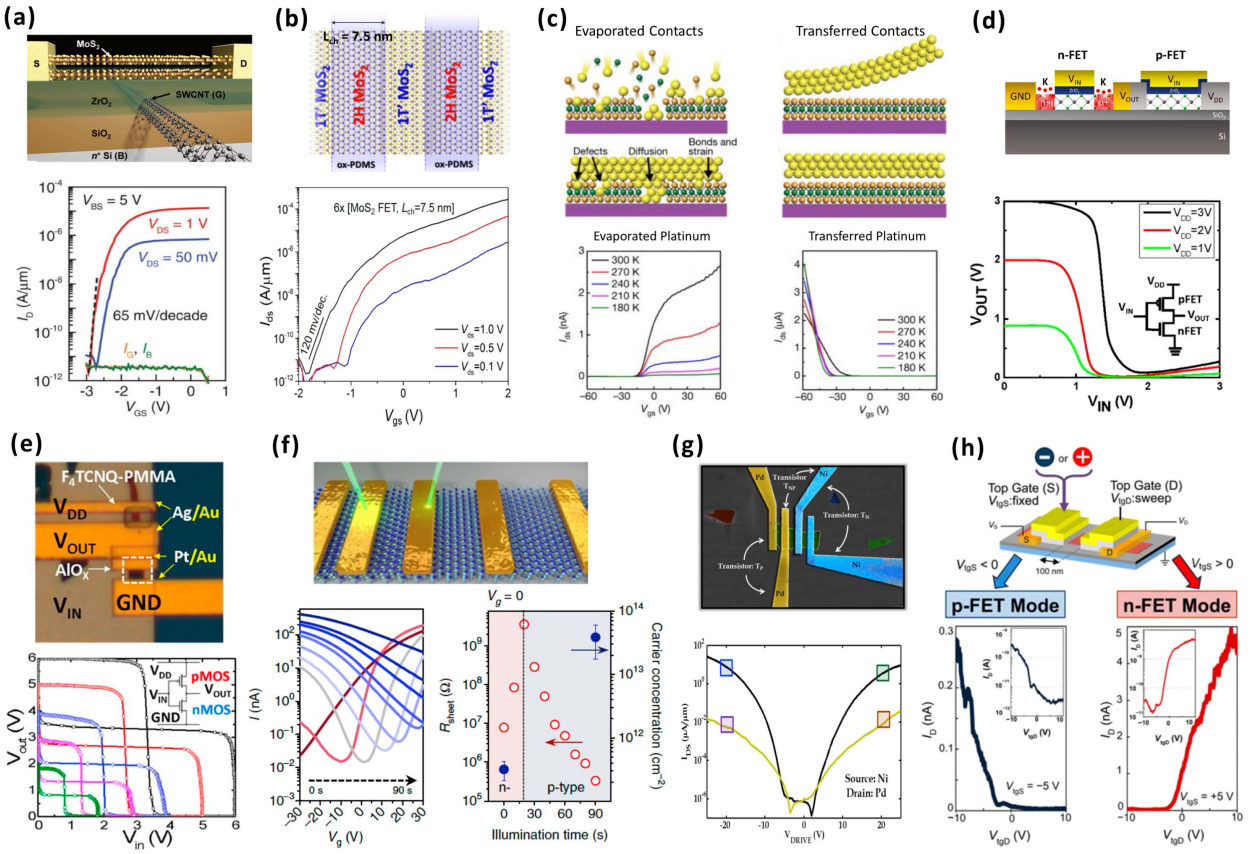

Fig. 3. 2-D-TMDCs electronics. (a) Schematic and transfer characteristics of a MoS_2 device gated by a single carbon nanotube. Adapted with permission from [93]. (b) Ultra-scaled MoS_2 devices fabricated with lithium-induced change to the metallic phase. Adapted with permission from [94]. (c) Comparison between the transfer characteristics of a MoS_2 device with evaporated and transferred platinum contacts. It is shown how p-type conduction can be achieved on MoS_2. Adapted with permission from [95]. (d) Demonstration of a high-gain complementary inverter realized with chemically doped WSe_2. Adapted with permission from [10]. (e) Chemical doping and different metal contacts, providing better carrier injection for electrons and holes, are used to demonstrate logic gates on WSe_2. Adapted with permission from [9] (f) Light-induced defects on $MoTe_2$ cause p-type doping of the 2-D semiconductor, allowing for the development of complementary logic. Adapted with permission from [96]. (g) Ambipolar characteristics of WSe_2 device. Adapted with permission from [97]. (h) Ambipolarity and polarity control demonstrated on exfoliated $MoTe_2$. Adapted with permission from [98].

the research community. Among the several semiconducting materials belonging to the TMDCs family, and introduced in Section II, the most appealing for electronic application have been the molybdenum (MoS_2, $MoTe_2$, and $MoSe_2$) and tungsten compounds (WSe_2 and WS_2). These semiconducting materials are stable in the air; even in their monolayer form, they are easily exfoliated from commercially available bulk crystal and are also grown with high quality in a large area, as shown in Section II. Several major results presented in this review have been achieved using mechanical exfoliation, which despite being a nonscalable approach, provides high-quality flakes that are used to gain insights into the properties of these materials and assess their potential for electronic applications. Fig. 3 summarizes a few of the most noticeable experimental results of the last years.

The most known TMDC material, MoS_2, has proven to be a viable solution for the realization of nMOS transistors [7], [8], [24], [99], [100] and ultrascaled devices that have been recently demonstrated [93], [94], [101] [see Fig. 3(a) and (b)]. In Fig. 3(a), a single carbon nanotube was used to gate a transistor with MoS_2 semiconducting channel, proving the superior electrostatic control achievable thanks to the ultrathin MoS_2 [93]. In Fig. 3(b), the devices with gate length below 10 nm were realized by inducing a change to the metallic phase of the MoS_2, with a lithium solution. This process also allows for a reduced contact resistance thanks to the metallic MoS_2 forming a seamless contact scheme with the 3-D metal [102]. To date, the largest circuit reported on 2-D MoS_2 is a 1-bit microprocessor composed of 115 transistors [103] and other small circuits that have also been previously demonstrated [8], [24], [104]. However, due to considerable difficulties in achieving the p-type behavior in MoS_2 [105], these circuits all adopt a noncomplementary nMOS logic that is not power-efficient. It has recently been demonstrated how p-type conduction can be achieved on MoS_2 by transferring metal contacts on top of the 2-D material, rather than evaporating it [95] [see Fig. 3(c)]. Using this innovative technique, it has been possible to show an almost linear relationship between the work function of the contact metal and the height of the Schottky barrier created, and

p-type conduction has been achieved with high work function metals (such as gold and platinum). Being able to develop both n- and p-type devices on the same semiconducting material is extremely important in order to achieve complementary operation of logic gates and circuits. Conventional CMOS uses ion implantation to physically dope silicon creating low-resistance ohmic contacts and irreversibly setting the polarity of the fabricated device (n- or p-type) according to the dopant atoms used [arsenic (As) for electron and phosphorus (P) for hole doping]. Since a reliable physical doping technique for 2-D materials is still lacking, chemical doping techniques have been explored to both reduce contact resistance (thus achieving higher ON-current) and to achieve complementary behavior [9], [10], [106]–[109]. These techniques are often tailored to the specific material used, in order to dope it against its natural carrier concentration (i.e., n-type doping for WSe_2 and p-type doping for MoS_2 and WS_2). The growth conditions also determine the natural carrier concentration of the materials, and it is important to develop techniques that allow the growth of high-quality, intrinsic materials in order to precisely tune the specific doping processes. Using WSe_2 as a semiconducting material, complementary operations of inverters and other small logic gates have recently been shown [see Fig. 3(d) and (e)] [9], [10]. However, chemical doping is often nonscalable, nonstable, and noncompatible with conventional CMOS fabrication. An innovative doping strategy has recently been proposed where a strong light source is used to locally create defects in $MoTe_2$ semiconducting channels, which upon oxidation, induce p-type doping [96] [see Fig. 3(f)]. This technique has allowed the realization of photovoltaic cells and bipolar-junction-transistor (BJT) arrays [96]. The possibility of using two different 2-D semiconductors to separately develop n- and p-type transistors has been explored using MoS_2 to fabricate nMOS device and monolithically integrate WSe_2 p-type devices on top, demonstrating complementary logic gates [26]. This paper shows the potential of 2-D materials to be used in combination with CMOS for 3-D monolithic integration. An alternative to the use of either chemical or physical doping is the exploitation of the ambipolar behavior, which refers to the capability of a semiconductor to conduct both charge carriers, and has been shown on several 2-D semiconductors, such as WSe_2, $MoTe_2$, WS_2, and $MoSe_2$ [97], [110]–[113] [see Fig. 3(f) and (g)]. A more comprehensive discussion on the opportunity to use the ambipolar behavior to realize doping-free and polarity-controllable devices is presented in Section VI. Other 2-D materials that are being explored include the members of the TMDCs family, such as $HfSe_2$ and $ZrSe_2$, which are appealing since their native oxides HfO_2 and ZrO_2 are CMOS compatible [114] and also BP. BP, in particular, has recently drawn considerable interest thanks to its high carrier mobility, ambipolar nature, and lower semiconducting bandgap compared with TMDCs [25], [86], [115]–[117]. However, BP is nonstable in ambient condition and only a few minutes of air exposure results in a complete oxidation of the semiconducting layer, making it challenging to integrate into a conventional VLSI fabrication flow [118]. While TMDCs and BP have been extensively studied for the fabrication of novel electronic devices, graphene, due to its semimetallic nature and high carrier mobility [119], is mainly considered to be integrated into VLSI systems for interconnect scaling [120], [121]. Monolayer graphene is explored as a diffusion barrier and capping layer to extend scaling of conventional copper (Cu) interconnects [120], [122], while multilayer graphene, in the form of nanoribbons, is looked at for entirely replacing Cu interconnects [120], [123]. One of the major challenges is the development of a technique that would allow to grow high-quality graphene at BEOL-compatible temperatures (i.e., 450 °C). Recently, a low-temperature process to grow graphene has been demonstrated, and upon doping with $FeCl_3$ graphene, nanoribbons of 20-nm width have shown lower resistivity than copper. It is expected that by improving the fabrication process and the doping technique, multilayer graphene interconnects could provide at least 4× smaller circuits delay compared with conventional Cu interconnects [123]. Graphene-based interconnects are also considered for future fully 2-D systems [124] and flexible electronics [125]–[127].

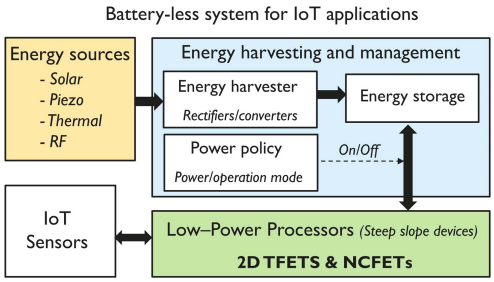

Fig. 4. Overview of self-sustainable energy harvesting system using low-power device alternatives. Adapted with permission from [128].

Following this general overview, we focus on the experimental results of two classes of devices: TFETs and NC-FETs for low-power applications and polarity-controllable FETs for doping-free circuits.

V. Devices for Low-Power Applications

In order to scale the supply voltage in the future technology nodes and provide more energy-efficient systems, several alternatives based on low-power devices are currently being explored. These devices are targeted to reduce the supply voltage to less than 0.5 V by reducing the subthreshold swing below 60 mV/decade. Besides the benefit in power consumption for VLSI systems, low-power devices could enable the realization of power-efficient processors powered by energy harvesters for the Internet-of-Things (IoT) applications [129]–[131] as well as low-voltage static random access memories (SRAMs) [130]. Fig. 4 shows a schematic of a self-sustainable (batteryless) energy harvesting system, which uses an ambient energy source, such as solar, piezo, or thermal to power a processor based on 2-D TFETs or ferroelectric FETs, also known as NCFETs [128]. NC-FETs are also being explored for energy-efficient nonvolatile computing, which is attractive for IoT applications [131]–[133]. This section

focuses on TFETs and NCFETs, as several promising demonstrations of these classes of devices has been shown using 2-D materials.

A. Tunnel FETs

TFETs are one of the candidates to replace conventional CMOS for future technology nodes due to their low supply voltage (V_{DD}) requirement and steep subthreshold slope (SS) at room temperature. The capability to achieve an SS lower than the thermionic limit of 60 mV/decade is enabled by the different conduction mechanism used in these devices. In fact, current flows in a TFET thanks to quantum mechanical tunneling of carriers from the valence band maximum of one material to the conduction band minimum of the other material, while in conventional MOSFETs, conduction is dominated by drift–diffusion mechanisms [140]. In recent years, much research has focused on realizing TFETs with semiconductors from group IV and group III–V. It has been shown that materials with a direct bandgap, such as III–V compounds, can provide higher ON-currents with lower supply voltage compared with indirect bandgap materials. This is because indirect bandgap materials require additional energy to compensate the mismatch in momentum when tunneling from the conduction band to the valence band [141]. Moreover, the III–V materials have low bandgaps and high electron mobilities, which are ideal for TFET performances. A good figure of merit to measure the TFET current performance is the I_{60} current, which is the maximum current value up to which the SS is less than 60 mV/decade [142]. In order for TFETs to compete with CMOS technology, the minimum required I_{60} current is 10 μA/μm and an ON-current of at least 100 μA/μm [141]. However, experimental demonstrations are still far away in reaching these goals. The main reason is that the III–V materials show a high density of trap states both at the dielectric and at the heterojunction interface, due to lattice mismatch, which degrades the band-to-band tunneling (BTBT) mechanism [143]–[145]. Therefore, the monolayer 2-D materials appear to be an ideal candidate for the realization of vertical heterostructures TFET applications thanks to their atomically thin body, direct bandgap, and self-passivating surfaces, which could result in no dangling bonds at the interfaces. The advantage of using monolayer 2-D materials is evident from simulation studies [146], [147], and however, it has not yet been confirmed by the experiments, which often use few-layer semiconductors [134]–[139].

Most experimental demonstrations with 2-D materials aim at achieving BTBT by forming a vertical heterostructure between a 2-D n-type material, such as MoS_2, WS_2, ReS_2, and $SnSe_2$, and a 2-D p-type material, such as WSe_2, $MoTe_2$, and BP, to create a vertical tunneling heterojunction. Heterostructure stacks, such as MoS_2–WSe_2 [136], [138], [148], [149], MoS_2–$MoTe_2$ [137], $SnSe_2$–WSe_2 [149], $SnSe_2$–$MoTe_2$, MoS_2–BP [84], [139], [150], have all shown to exhibit BTBT. Fig. 5 displays a summary of the state of the art for 2-D TFETs. Fig. 5(a) shows a MoS_2–BP heterostructure TFET fabricated using an electrolyte gating with a steep subthreshold of 55 mV/decade as shown in the I_D–V_G characteristics [134]. Fig. 5(b) shows an example of a 3-D–2-D-based tunneling approach where germanium (Ge) is stacked with MoS_2 to form a TFET. The I_D–V_G characteristics of Ge–MoS_2 [135] are shown with an average SS of $\sim$31 mV/decade, using electrolyte gating. This SS is the lowest reported on TFETs to date. The advantage of using a bulk material is that they can be easily doped (not yet possible with 2-D materials, as discussed in Section IV) to provide a lower band offset. This, combined with a 2-D material, can lower scattering and provide improved electrostatics, thus leading to more efficient tunneling [151]. However, as previously mentioned, great care needs to be taken when dealing with the 3-D–2-D interface in order to minimize the trap states at the surface. In Fig. 5(c), a MoS_2–WSe_2 TFET is fabricated with two separate gates, enabling the individual modulation of the n- (MoS_2) and p-type (WSe_2) materials [136]. The device also shows SS less than 60 mV/decade. Fig. 5(d) displays a MoS_2–$MoTe_2$ TFET that also follows the previous approach of having an isolated bottom gate that modulates $MoTe_2$ and not MoS_2. The I_D–V_G characteristics shows a temperature-dependent BTBT current, which occurs due to the recombination/generation currents present at higher temperatures [137]. The devices in Fig. 5(a) and (b) follow a complete top/bottom gate configuration approach, where both the n- and p-type materials are modulated with the same gate potential. However, a major drawback is that this device architecture can hinder the possibility of creating a broken band alignment for tunneling if the materials are not doped enough. Moreover, the Schottky contacts are also modulated simultaneously with the heterostructure, which can degrade the steep switching in the device [137]. The isolated gate approach shown in the devices in Fig. 5(c) and (d) has the advantage of modulating the carrier concentration of the individual n- and p-type materials when neither of the materials is highly doped. However, this configuration is more complicated to fabricate, as it requires two gates per transistor, which is not ideal in an integration point of view. Fig. 5(e) shows a MoS_2–WSe_2 heterostructure FET that shows the phenomena of negative differential transconductance (NDT) in the I_D–V_G characteristics [152]. A similar behavior is also shown by a MoS_2–BP heterostructure FET [see Fig 5(f)]. The NDT phenomena can be exploited to create devices that support multivalued logic (MVL), and MVL inverters have been demonstrated with 2-D TFETs [138], [139], [153]. Thanks to the higher number of logic states and higher data storage density, MVL logic is considered to be a promising alternative to traditional binary logic.

Despite the large amount of experimental work on 2-D TFETs, not many devices have shown a steep SS of less than 60 mV/decade. This is possibly due to several factors, such as the presence of Schottky contacts at the metal–semiconductor heterojunction [137], [154], the high density of interface traps at the semiconductor–oxide interface, and the presence of defects and grain boundaries in the 2-D materials. Further experimental work is needed to improve the performances of 2-D TFETs and enable their integration in VLSI systems.

B. Negative Capacitance FET

NCFETs have recently shown promising performances for steep switching application. Unlike TFETs that obtain the

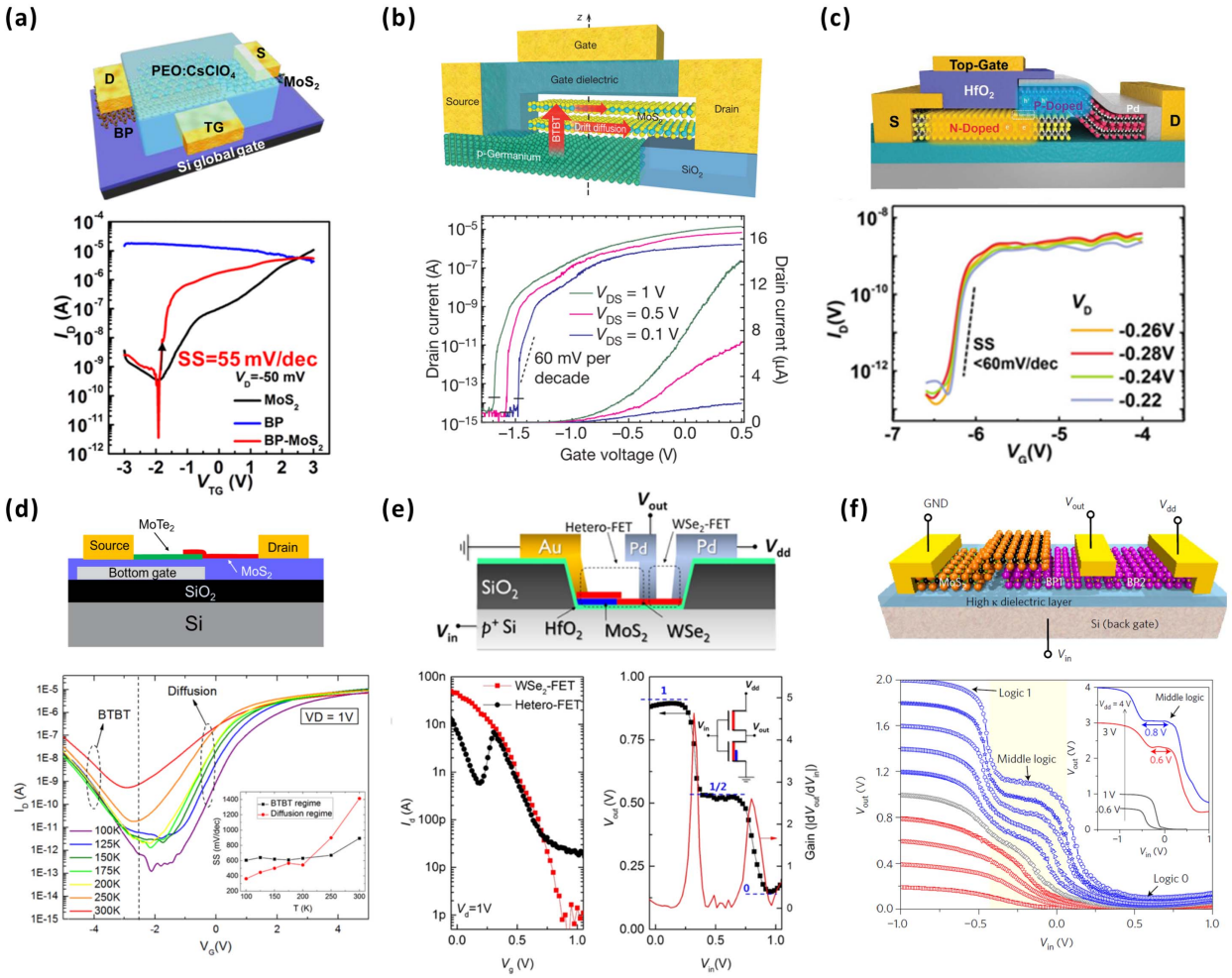

Fig. 5. Experimental results of 2-D TFETs. (a) Device schematic and I_D–V_G curve of a MoS_2–BP TFET with electrolyte gating. Adapted with permission from [134]. (b) Device schematic and transfer characteristics of a Ge–MoS_2 TFET with electrolyte gating. Adapted with permission from [135]. (c) Schematic cross section and I_D–V_G of a MoS_2–WSe_2 TFET with an isolated gate device. Adapted with permission from [136]. (d) Schematic cross section and transfer characteristics of MoS_2–$MoTe_2$ with an isolated bottom gate. Adapted with permission from [137]. (e) Device cross section and I_D–V_G curve of a MoS_2–WSe_2 heterostructure FET showing NDT and MVL operation. Adapted with permission from [138]. (f) Device schematic and transfer characteristics of a MoS_2–BP heterostructure FET showing the NDT behavior for MVL applications. Adapted with permission from [139].

steep switching through BTBT, NCFETs still use a conventional drift–diffusion conduction mechanism, paired with a ferroelectric gate dielectric. The steep switching is enabled by the phenomena of negative capacitance that arises from the transient response of the ferroelectric dielectric while switching its polarization. A ferroelectric material has two polarized states, which can be altered from one state to another with an external applied bias [159]. When the polarization state is switched, the charge-to-voltage variation becomes negative (i.e., $dQ/dV < 0$). This negative value of dQ/dV corresponds to a negative differential capacitance and, when inputted in the equation of SS, results in a subthreshold swing of less than 60 mV/decade [160], [161]. The phenomena of negative capacitance could act as a performance booster for any CMOS platform, even conventional silicon FinFETs, by improving both the SS and the overdrive voltage [162]. However, 2-D materials are attractive for NCFETs because, thanks to their atomically thin body and high mobility, they can respond to a change in polarization more rapidly than a bulk semiconductor.

Several works have focused on the integration of ferroelectric materials in Si MOSFETs and FinFETs to achieve steep slope performance, and CMOS compatible hafnium-oxide-based ferroelectric materials have been demonstrated by doping hafnium oxide (HfO_2) with materials, such as Al, Zr, and Si. The 2-D-based NCFETS using Al- and Zr-doped HfO_2 and other ferroelectrics have been shown to have steep switching characteristics, as discussed in the following [165]–[167]. Moreover, there has been considerable interest in the recent demonstration of an NCFET using a 2-D semiconductor (MoS_2), as well as a 2-D ferroelectric oxide $CuInP_2S_6$ (CIPS) [168]. A considerable and yet unsolved issue with NCFET is the large hysteresis that arises from the ferroelectric material while shifting the polarization state [159].

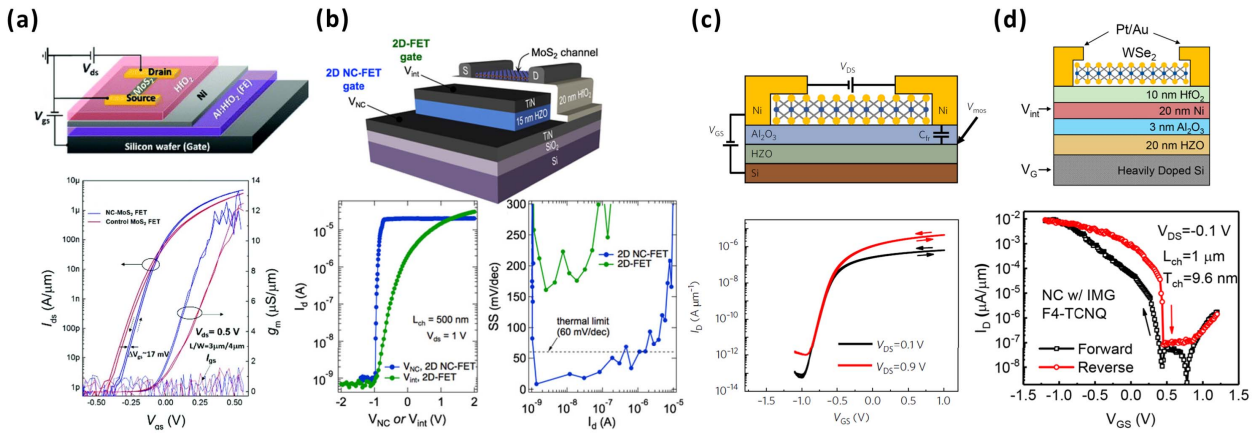

Fig. 6. Experimental studies result in 2-D NCFET based on different 2-D materials and ferroelectric gate-stacks, respectively. (a) Structure schematic and I_D–V_G curve of the MoS_2-NCFET with ferroelectric Al:HfO_2 layer. Adapted with permission from [155]. (b) Structure schematic and I_D–V_G and SS curves of the MoS_2-NCFET with ferroelectric HZO layer. Adapted with permission from [156]. (c) Schematic cross section and I_D–V_G characteristics of the MoS_2-NCFET with ferroelectric HZO without an IMG layer. Adapted with permission from [157]. (d) Schematic cross section and transfer characteristics of the WSe_2-NCFET with ferroelectric HZO layer. Adapted with permission from [158].

TABLE I
STATISTICAL TABLE OF EXPERIMENTAL RESULTS ON 2-D NCFETS

No.	2D Material	FE Material	Type	L_{ch}	V_d	I_{60}	I_{ON}	lowest SS	ref
2	MoS_2	HZO	MFMIS	500 nm	1 V	5 μA	5 μA	6.07 mV/dec	[157]
3	MoS_2	Al:HfO2	MFMIS	3 μm	0.5 V	500 pA	13 μA	57 mV/dec	[156]
4	MoS_2	P(VDF-TrFE)	MFIS	80 nm	0.5 V	10 nA	100 μA	24.2 mV/dec	[164]
5	MoS_2	HZO	MFMIS	1 μm	0.5 V	100 pA	10 μA	37.6 mV/dec	[165]
6	MoS_2	HZO	MFIS	2 μm	0.5 V	N/A	510 μA	52.3 mV/dec	[158]
7	WSe_2	HZO	MFMIS	1 μm	0.1 V	200 pA	10 nA	14.4 mV/dec	[159]

Hysteresis could be reduced by capacitance matching between the ferroelectric layer and the dielectric layer. This complicated process aims at achieving a single energy minimum in the energy landscape of the resulting capacitor, thus reducing or eliminating hysteresis, which originates from the presence of two energy minimum [169], [170]. Design guidelines for NCFETs should thus include specifications for the tolerance range of hysteresis, as addressed in [171]. However, in order to achieve a steeper SS, most of the NCFETs reported in the literature are fabricated with an internal metal gate (IMG), placed in between the ferroelectric and dielectric layers, which makes capacitance matching impossible to obtain and enhances the hysteretic behavior [172].

Fig. 6 displays several 2-D NCFETs fabricated with and without an IMG architecture. Fig. 6(a) show a schematic cross section of a MoS_2 NCFET using Al:HfO_2 dielectric with a Ni IMG layer [155]. The I_D–V_G curve shows a low hysteresis with a slight improvement in SS of 57mV/decade compared with when only gating it with regular HfO_2. Fig. 6(b) shows a schematic cross section of a MoS_2 NCFET using hafnium–zirconium oxide (HZO) with a TiN IMG layer [156]. The I_D–V_G curve displays a very steep SS with a minimum of 6.07 mV/decade when compared with the regular MoS_2 FET. However, a very large hysteresis is also observed for this device. Fig. 6(c) shows a MoS_2 NCFET with HZO as ferroelectric without an IMG layer [157]. The I_D–V_G curve has very small hysteresis, however, with the tradeoff of a larger SS of 52.3 mV/decade. For this device, the drain ON-current level, I_{ON}, of 510 μA/μm is among the highest values for the state-of-the-art steep-slope FETs reported so far [162]. A p-type NCFET using WSe_2 was also realized, as shown in Fig. 6(d), using HZO ferroelectric with an IMG layer [158]. The device dimensions and their performances in terms of SS and ON-current are summarized in Table I, which also includes other notable examples. The devices are separated into two types: metal–ferroelectric–metal–insulator–semiconductor (MFMIS), the devices that contain an IMG layer, and metal–ferroelectric–insulator–semiconductor (MFIS), devices without an IMG layer. The devices have shown to obtain a steep SS below 60 mV/decade and have shown more promise compared with its TFET counterpart. All the reports used exfoliated flakes with a majority of the work done using MoS_2 and different ferroelectric materials.

Apart from improving performances of CMOS devices, NCFETs have other potential applications such as to realize nonvolatile flip-flops for IoT applications, provided that the polarization of the ferroelectric layer is maintained in the absence of gate voltage [132]. As mentioned earlier, the hysteresis created by the introduction of the ferroelectric material is detrimental to purely logic applications, but if properly

controlled could improve the noise margin on SRAMs [131]–[133]. Moreover, the possibility of dynamically tuning the hysteresis to the zero-gate-voltage region will create novel memory-logic interchangeable circuits for energy harvesting processor and in-memory computing [128]. As a final remark, it is worth mentioning that NCFETs offer extensive dynamic voltage–frequency scaling (DVFS) with a wide range of power-performance options [173], [174]. This feature can be applied to low-voltage near-threshold computing, which is an active area of research with attractive energy efficiency [174], [175].

VI. Polarity-Controllable Doping-Free Devices and Logic Gates on WSe_2

Physical doping, through ion-implantation, of the 2-D material has not proven to be successful due to the extreme thinness of the 2-D semiconductors, with ions just implanting in the substrate. The possibility of introducing dopant atoms [such as rhenium (Re) or niobium (Nb) for MoS_2] during the growth of the 2-D material has been reported but lacks selectivity and does not allow for any control of the doping profile [176]–[180]. Several chemical and molecular doping techniques have been developed and have been addressed in Section IV, but are often nonstable and non-CMOS compatible, thus not allowing the integration of chemically doped 2-D devices in the BEOL fabrication of VLSI circuits [9], [10], [106]. A device concept that would not rely on any physical doping and use undoped materials would be of great interest in this regard. When no physical or chemical doping is introduced (i.e., an undoped material is used), contact to a 2-D semiconductor usually results in the creation of a Schottky barrier at the source and drain contacts. The height of the Schottky barrier determines the conduction properties of the device, as undoped materials are, for the most part, able to conduct both charge carriers (i.e., electrons and holes). However, it is challenging to control the OFF state of a purely ambipolar device when using a standard gate configuration, as we cannot selectively suppress the conduction of a specific type of charge carriers [97], [181]. In order to control the polarity of the transistor and achieve either n- or p-type behavior, a separate gating of different channel regions is introduced, which we refer to as a double-independent-gate (DIG) structure [181]. A second gate is added, named polarity gate (PG), which induces electrostatic doping at the contact interfaces, effectively modulating the height of the Schottky barrier and blocking the injection either of electrons or holes. It is then possible to dynamically reconfigure the device polarity at run time, by reversing the bias applied to the PG. A conventional gate, named control gate (CG), acts in the central region of the channel and controls the ON/OFF state of the device. The possibility to dynamically flip the polarity at a run time enhances the switching property of the devices, enabling a doping-free, highly flexible design for logic circuits [182], [183]. Differently, from the TFETs and NCFETs, DIG-FETs do not inherently provide a way to reduce the SS below the limit of 60 mV/decade, although steep switching has been demonstrated on Si FinFETs with a DIG structure by increasing the V_{DS} bias and achieving weak-impact ionization of charge carriers [184]. Moreover, the application of ferroelectric oxide to a DIG-FET structure could be foreseen in future research.

As mentioned in Section IV, ambipolar behavior has been demonstrated on several 2-D materials (such as WSe_2, $MoTe_2$, $MoSe_2$, and BP), with WSe_2 showing high mobility and high current densities for both charge carriers [97], [185]–[188]. Recent progress in the demonstration of 2-D polarity-controllable doping-free devices and circuits has been made using WSe_2 and is summarized in Fig. 7 [27]. A schematic cross section of a single device presented in Fig. 7(a), highlighting the position of the PG and CG as well as the semiconducting channel. The devices are fabricated experimentally on exfoliated WSe_2, and the demonstration of polarity control is shown in Fig. 7(b). The inset shows a schematic of the band profile at the source contact for two opposite biases of the PG. When the PG is biased at 0 V or below, holes are favorably injected in the channel, and the device behaves as a p-type transistor. Conversely, the transistor is programmed to function as an n-type device when the PG is biased at 3 V and above. In both cases, the CG is able to turn on and off the transistor when swept between 0 and 2 V. A standard-cell library has been demonstrated with doping-free polarity-controllable WSe_2 FETs, including inverters, NAND, NOR, XOR, and MAJ gates [see Fig. 7(c) and (d)]. The DIG structure results in a more expressive switching function of the fabricated devices, which act as comparison driven switches (i.e., the device is conducting when both PG and CG are controlled by the same logic value). Thanks to the higher expressivity of the single device, it is possible to realize compact two-input XOR gates using only four transistors (not counting the inverters needed to generate the negate signals), while in CMOS, eight transistors would be necessary. The peculiar switching properties of the devices also enable the fabrication of three-input XOR and three-input MAJ gates using only four transistors and replacing the V_{DD} and GND terminals with logic inputs [27], [183]. The possibility of realizing highly compact XOR and MAJ gates has been explored in the synthesis of arithmetic circuits, as will be discussed in Section VII. The challenges that need to be addressed to enable the use of polarity-controllable devices in VLSI systems include achieving a symmetric behavior of the n- and p-type branches by tuning the Schottky barrier at contacts, reach the p-type behavior without the need to apply negative gate voltages (to ensure cascadability), and operate both gate terminals with the same voltage bias.

The experimental results presented in Sections IV–VI show the potential of 2-D semiconductors for several applications, but simulations are essential to better evaluate the strength and weakness of different devices. In Section VII, we will focus on the most recent simulation results for 2-D devices and circuits.

VII. Performances Projection at Scaled Device Dimensions

The need for modeling and simulation to assess the performances of devices and circuits at scaled gate dimensions has already been highlighted in Section III as one of the critical steps in the roadmap. It is crucial to rely on accurate simulations to understand the scaling possibilities for different

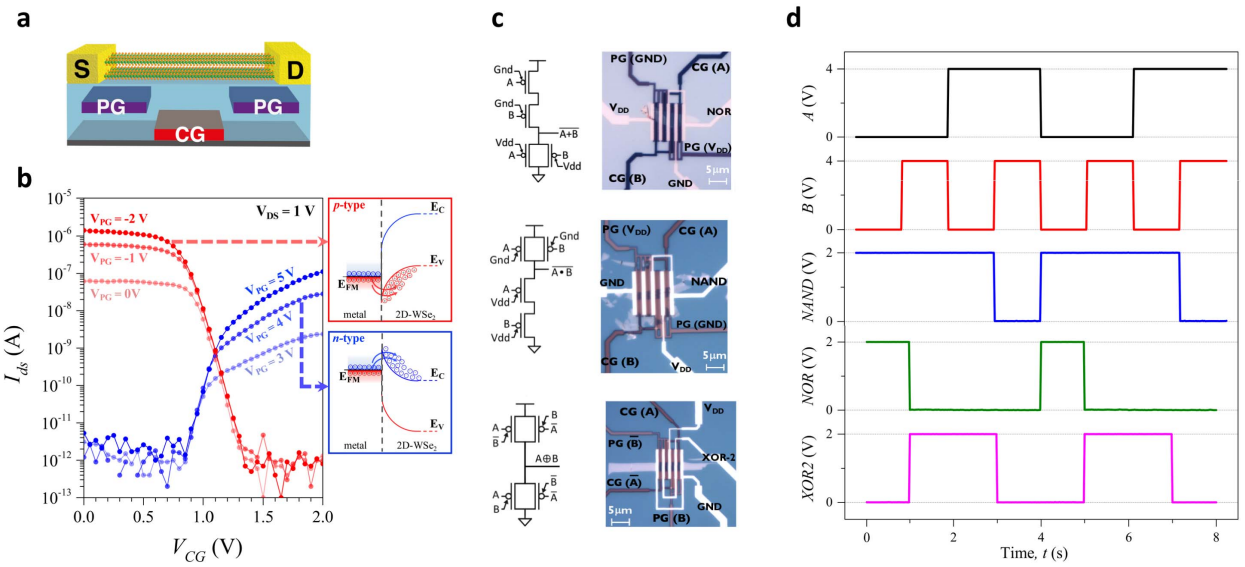

Fig. 7. Polarity-controllable devices and circuits. (a) Schematic cross section of a single polarity-controllable device, highlighting the presence of the PG acting at the contact interface and the CG placed in the central region of the channel. (b) Transfer characteristics demonstrating the polarity-controllable behavior. Insets: schematic of the band-bending at the contacts for n- and p-type operation. (c) Optical micrograph and circuit schematic of the fabricated NAND, NOR, and 2-input XOR gates. (d) Quasi-static measurements of the doping-free logic gates, demonstrating proper operation. Adapted with permission from [27].

classes of devices, compare their performances, and assess the circuit-level metrics. Simulations can also provide guidance and insights into improving the fabrication process (e.g., which metal provides the lowest contact resistance or which oxide lowers the phonon scattering). Scaled device characteristics for 2-D materials have mainly been studied using *ab initio* methods, where the band structure extracted from density functional theory (DFT) calculations [192] is used within a nonequilibrium Green's function (NEGF) formalism to derive the current–voltage characteristics of a device [193]. These simulations require a high computational cost, which increases tremendously when several conduction and valence bands are considered in the Hamiltonian and when scattering is introduced in the simulations [194]. They are also only suitable for single scaled-devices simulations. In order to reduce the computational cost and extend the simulations to circuit level, several compact models have been proposed that are able to reproduce the results of NEGF simulations or experimental results for both doped-FETs and TFETs [61], [73]–[77], [195]. Using these compact models, circuit simulations have shown that 2-D materials could theoretically outperform conventional Si-FinFETs and meet ITRS performance and power-delay requirements [61], [196]–[199]. Fig. 8 summarizes some of the main simulation results both at the device and circuit level for the three main classes of devices presented in this paper (i.e., conventional doped 2-D FETs, 2-D TFETs, and doping-free 2-D FETs). We excluded considerations on NC-FETs, as simulation results on scaled devices and circuit perspectives are still lacking for 2-D materials.

A. Doped 2-D FETs

For 2-D-doped FETs, it was found that a double-gated structure, like the one presented in Fig. 8(a), provides better electrostatic control on the channel, particularly when using a few-layer 2-D material. Work from Cao *et al.* [11] and Szabó *et al.* [194] have focused on understanding the impact of charge and phonon scattering on the device performances [see Fig. 8(b)] and have shown that even at ultrascaled dimensions ($L_G = 8$ nm), scattering can reduce the ON-current considerably. As mentioned in Section III, the material choice can be guided by several factors, such as intrinsic device performances, fabrication simplicity, or stability of the 2-D materials. In this context, several simulations have been performed to assess which 2-D material can provide the best device performances [11], [12], [14], [69], [189], [198] [see Fig. 8(c)]. Thanks to the possibility of low-temperature integration (see Section II), the performance projection of monolithically integrated 2-D-FETs has been studied [see Fig. 8(d)] [69]. Simulations including parasitic capacitances and wire loads have shown how devices based on WS_2 could be able to provide lower energy-delay-product (EDP) than conventional Fin-FETs in future technology nodes [69]. Moreover, a 32-bit commercial processor core has been implemented with 5-nm design rules to assess the benefits of 2-D transistors on a large-scale design [196]. It was found that 2-D-FETs can provide $\sim 2\times$ better EDP with respect to conventional Si Fin-FETs, provided that a contact resistivity $<6 \times 10^{-8}\ \Omega \cdot \mu\text{m}^2$ can be achieved [196].

B. Two-Dimensional TFETs

The schematic of a scaled TFET exploiting band-to-band vertical tunneling between the p- and n-type semiconductors is shown in Fig. 8(e), with a schematic of the band levels and effective masses [147]. As shown in Fig. 8(f), the transfer characteristics of the scaled devices appear promising reaching

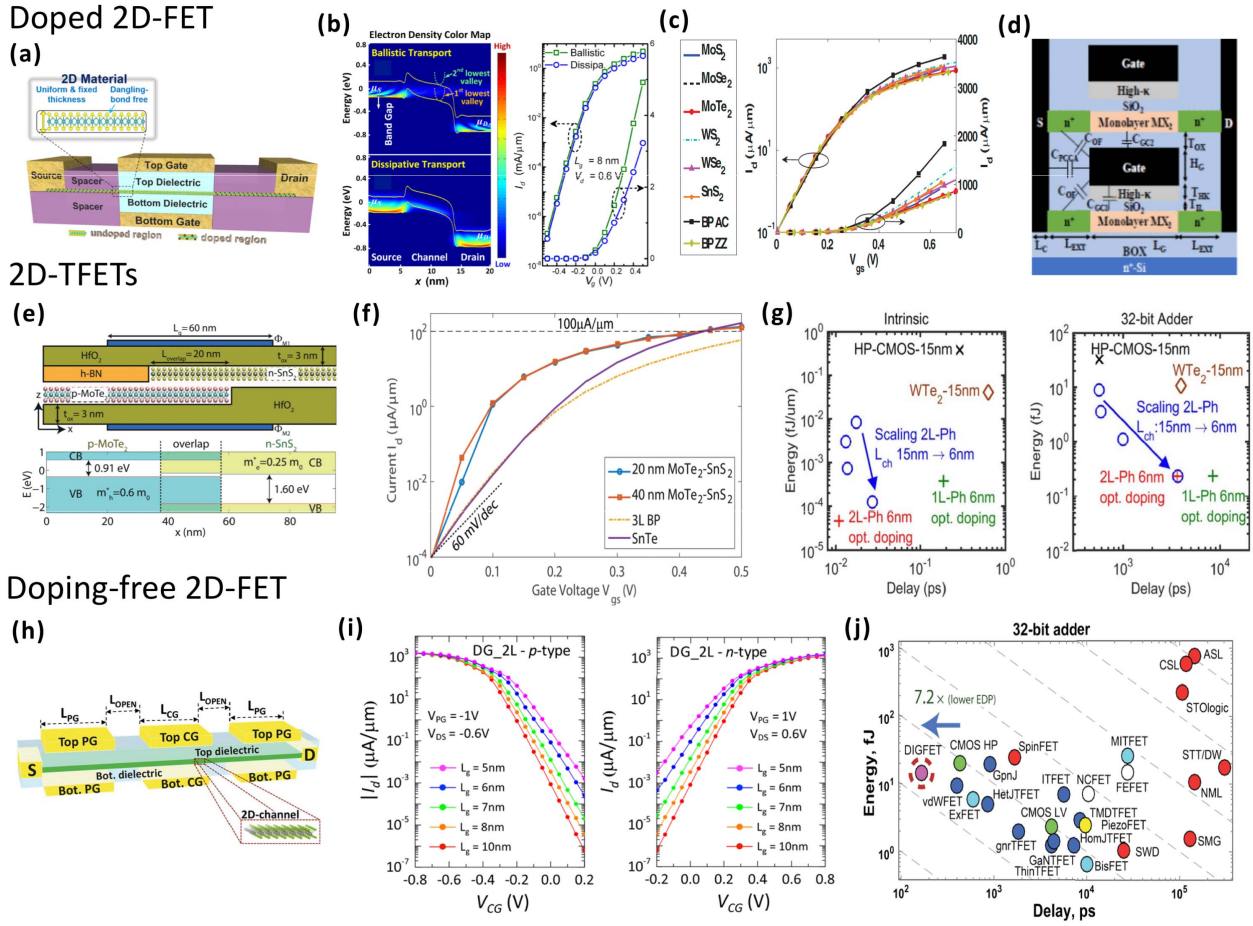

Fig. 8. Device and circuits performances at scaled gate lengths. (a) Schematic of a double-gate FET with doped contacts. Adapted with permission from [11]. (b) Electron density color map and transfer characteristics of the scaled device in (a), showing the effect of scattering on the performances of the device. Adapted with permission from [11]. (c) Comparison of transfer characteristics for several 2-D TMDCs and BP. Adapted with permission from [189]. (d) Schematic of a monolithically integrated device with MX_2 materials, which is benchmarked against conventional Si-FinFETs. Adapted with permission from [69]. (e) Schematic cross section of a scaled TFET device, showing the band alignment between the 2-D semiconductors. Adapted with permission from [147]. (f) Transfer characteristics of the device in (e), showing steep-switching and relatively high ON-current. Adapted with permission from [147]. (g) Study of EDP improvements both at the device and circuit level for ultrascaled BP-TFETs. Adapted with permission from [70]. (h) Three-dimensional schematic of the simulated polarity-controllable FET. (i) Transfer characteristics for the device in (h), showing the feasibility of polarity-control down to 5-nm gate lengths. Scaling of the channel length results in an increased SS, as also demonstrated for conventional doped 2-D FETs in [11]. Adapted with permission from [190]. (j) EDP projection for a doping-free 32-bit adder realized with polarity-controllable 2-D FETs. The use of polarity-controllable 2-D FETs enables a ~7× reduction in EDP compared with scaled high-power CMOS. Adapted with permission from [191].

ON-currents greater than 100 μA/μm, having I_{60} of around 1 μA/μm and operating at $V_{DD} = 0.5$ V. These simulations, although promising, are purely ballistic and not include any effect arising from scattering, traps, and contact resistance. Other works have also investigated different geometries and materials [200]–[203]. As mentioned in Section V-A, BP is a material that has attracted considerable interest for TFETs applications and its performances at scaled gate lengths have been studied [70] and compared with HP CMOS as in the beyond-CMOS benchmark [204]. In this case, no heterostructure is used, and the BTBT takes place between the heavily p-doped source and the heavily n-doped drain through an intrinsic region (i.e., p-i-n structure). Fig. 8(g) shows the switching energy versus delay, a metric usually referred to as EDP, for the intrinsic-scaled BP device and for a 32-bit adder realized with 2-D-BP TFETs. It is demonstrated that thanks to the lower bandgap, two-layer BP with asymmetric optimized doping provides the most improvement in EDP. However, it can be seen in Fig. 8(g) that the improvements in EDP for the 32-bit adder are not as significant as the ones promised by the intrinsic EDP. This is caused by the presence of interconnects and parasitic capacitances that in the sub-10-nm regime, play a critical role.

C. Doping-Free 2-D FETs

Using a scaled double-gated structure [see Fig. 8(h)], the performances of doping-free polarity-controllable devices have been assessed by Resta *et al.* [190], using ballistic NEGF simulations. It is shown how a reduction in the semiconducting

bandgap of the MX_2 material can lead to higher ON-currents (due to improved tunneling at the contacts) while maintaining sufficient electrostatic control over the channel to switch OFF the device [see Fig. 8(i)]. For a bandgap energy of 0.8 eV, I_{ON} can reach 1.5 μA/μm while keeping I_{OFF} well below 10^{-2} μA/μm down to $L_G = 5$ nm. It should be noted that due to the presence of the additional PG, the device is inherently longer than conventional CMOS, and in the simulations, L_G refers to the length of each gated segments, either PG or CG. The simulated transfer characteristics for the 10-nm devices were used to simulate the behavior of a 32-bit adder, which is compared with other technologies of beyond-CMOS benchmark [191], [204]. Thanks to the design possibilities enabled by polarity-controllable devices at the circuit level, e.g., compact realization of XOR and MAJ gates, it was shown a $\sim 7\times$ reduction in EDP when compared with HP-scaled CMOS [see Fig. 8(j)] [191].

VIII. Conclusion and Perspective

This paper provided an overview of the recent advances in the field of 2-D electronics. We focused on three different aspects that are equally relevant for the evaluation of novel materials and novel devices considering material synthesis, experimental demonstrations, and projections of device performances. We looked closely at novel device concepts that have been boosted by the properties of 2-D materials, such as TFETs and NCFETs, and also provided an in-depth discussion on the possibility of realizing doping-free 2-D circuits thanks to polarity-controllable devices. For each topic, we highlighted the main achievements and evaluated the challenges that remain to be addressed in order to integrate the 2-D materials into VLSI systems. This integration can be fruitful by using 2-D materials alongside the conventional silicon CMOS, where we could envision 2-D-TMDCs circuits being integrated into the BEOL and graphene nanoribbons used for interconnects. A truly 3-D nanosystem could be enabled by the low-temperature fabrication process required by the 2-D materials leading to dense 3-D monolithic VLSI systems, integrating memory, sensors, and electronics on the same chip [205]. Moreover, the foldable and flexible electronic system could also greatly benefit from the thinness and large area availability of 2-D materials, enabling more compact and portable wearable systems.

Acknowledgment

The authors would like to thank C. Huyghebaert and F. Catthoor for their valuable input and stimulating discussions.

References

[1] P. R. Wallace, "The band theory of graphite," *Phys. Rev.*, vol. 71, no. 9, p. 622, 1947.

[2] J. A. Wilson and A. Yoffe, "The transition metal dichalcogenides discussion and interpretation of the observed optical, electrical and structural properties," *Adv. Phys.*, vol. 18, no. 73, pp. 193–335, 1969.

[3] K. S. Novoselov *et al.*, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, no. 5696, pp. 666–669, 2004.

[4] D. Jariwala, V. K. Sangwan, L. J. Lauhon, T. J. Marks, and M. C. Hersam, "Emerging device applications for semiconducting two-dimensional transition metal dichalcogenides," *ACS Nano*, vol. 8, no. 2, pp. 1102–1120, 2014.

[5] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, "Electronics and optoelectronics of two-dimensional transition metal dichalcogenides," *Nature Nanotechnol.*, vol. 7, no. 11, p. 699, Nov. 2012.

[6] G. Fiori *et al.*, and L. Colombo, "Electronics based on two-dimensional materials," *Nature Nanotechnol.*, vol. 9, no. 10, pp. 768–779, 2014.

[7] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS_2 transistors," *Nature Nanotechnol.*, vol. 6, no. 3, pp. 147–150, 2011.

[8] H. Wang *et al.*, "Integrated circuits based on bilayer MoS_2 transistors," *Nano Lett.*, vol. 12, no. 9, pp. 4674–4680, 2012.

[9] L. Yu *et al.*, "High-performance WSe_2 complementary metal oxide semiconductor technology and integrated circuits," *Nano Lett.*, vol. 15, no. 8, pp. 4928–4934, Jul. 2015.

[10] M. Tosun *et al.*, "High-gain inverters based on WSe_2 complementary field-effect transistors," *ACS Nano*, vol. 8, no. 5, pp. 4948–4953, 2014.

[11] W. Cao, J. Kang, D. Sarkar, W. Liu, and K. Banerjee, "2D semiconductor FETs—Projections and design for sub-10 nm VLSI," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3459–3469, Nov. 2015.

[12] V. Mishra, S. Smith, K. Ganapathi, and S. Salahuddin, "Dependence of intrinsic performance of transition metal dichalcogenide transistors on materials and number of layers at the 5 nm channel-length limit," in *IEDM Tech. Dig.*, Dec. 2013, pp. 5–6.

[13] Y. Yoon, K. Ganapathi, and S. Salahuddin, "How good can monolayer MoS_2 transistors be?" *Nano Lett.*, vol. 11, no. 9, pp. 3768–3773, 2011.

[14] L. Liu, S. Bala Kumar, Y. Ouyang, and J. Guo, "Performance limits of monolayer transition metal dichalcogenide transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 3042–3047, Sep. 2011.

[15] K. Kang *et al.*, "High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity," *Nature*, vol. 520, no. 7549, pp. 656–660, 2015.

[16] K. Verguts *et al.*, "Growth of millimeter-sized graphene single crystals on $Al_2O_3(0001)$/Pt(111) template wafers using chemical vapor deposition," *ECS J. Solid State Sci. Technol.*, vol. 7, no. 12, pp. M195–M200, 2018.

[17] J. Zhou *et al.*, "A library of atomically thin metal chalcogenides," *Nature*, vol. 556, no. 7701, pp. 355–359, 2018.

[18] H. Yu *et al.*, "Wafer-scale growth and transfer of highly-oriented monolayer MoS_2 continuous films," *ACS Nano*, vol. 11, no. 12, pp. 12001–12007, 2017.

[19] C. Huyghebaert *et al.*, "2D materials: Roadmap to CMOS integration," in *IEDM Tech. Dig.*, Dec. 2018, pp. 22.1.1–22.1.4.

[20] K. Kang *et al.*, "Layer-by-layer assembly of two-dimensional materials into wafer-scale heterostructures," *Nature*, vol. 550, pp. 229–233, Oct. 2017.

[21] H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, and A. Javey, "High-performance single layered WSe_2 p-FETs with chemically doped contacts," *Nano Lett.*, vol. 12, no. 7, pp. 3788–3792, 2012.

[22] A. K. Geim and I. V. Grigorieva, "Van der Waals heterostructures," *Nature*, vol. 499, pp. 419–425, Jul. 2013.

[23] D. Ovchinnikov, A. Allain, Y.-S. Huang, D. Dumcenco, and A. Kis, "Electrical transport properties of single-layer WS_2," *ACS Nano*, vol. 8, no. 8, pp. 8174–8181, 2014.

[24] B. Radisavljevic, M. B. Whitwick, and A. Kis, "Integrated circuits and logic operations based on single-layer MoS_2," *ACS Nano*, vol. 5, no. 12, pp. 9934–9938, 2011.

[25] W. Zhu *et al.*, "Flexible black phosphorus ambipolar transistors, circuits and AM demodulator," *Nano Lett.*, vol. 15, no. 3, pp. 1883–1890, Feb. 2015.

[26] A. B. Sachid *et al.*, "Monolithic 3D CMOS using layered semiconductors," *Adv. Mater.*, vol. 28, no. 13, pp. 2547–2554, 2016.

[27] G. V. Resta *et al.*, "Doping-free complementary logic gates enabled by two-dimensional polarity-controllable transistors," *ACS Nano*, vol. 12, no. 7, pp. 7039–7047, 2018.

[28] K. K. H. Smithe, C. D. English, S. V. Suryavanshi, and E. Pop, "Intrinsic electrical transport and performance projections of synthetic monolayer MoS_2 devices," *2D Mater.*, vol. 4, no. 1, 2017, Art. no. 011009.

[29] K. Verguts *et al.*, "Controlling water intercalation is key to a direct graphene transfer," *ACS Appl. Mater. Interfaces*, vol. 9, no. 42, pp. 37484–37492, Oct. 2017.

[30] L. Banszerus *et al.*, "Ultrahigh-mobility graphene devices from chemical vapor deposition on reusable copper," *Sci. Adv.*, vol. 1, no. 6, 2015, Art. no. e1500222.

[31] Z. Xu, H. Tian, A. Khanaki, R. Zheng, M. Suja, and J. Liu, "Large-area growth of multi-layer hexagonal boron nitride on polished cobalt foils by plasma-assisted molecular beam epitaxy," *Sci. Rep.*, vol. 7, Feb. 2017, Art. no. 43100.

[32] W. Chen *et al.*, "Oxygen-assisted chemical vapor deposition growth of large single-crystal and high-quality monolayer MoS_2," *J. Amer. Chem. Soc.*, vol. 137, no. 50, pp. 15632–15635, 2015.

[33] D. Chiappe *et al.*, "Layer-controlled epitaxy of 2D semiconductors: Bridging nanoscale phenomena to wafer-scale uniformity," *Nanotechnology*, vol. 29, no. 42, Aug. 2018, Art. no. 425602.

[34] N. Choudhary, J. Park, J. Y. Hwang, and W. Choi, "Growth of large-scale and thickness-modulated MoS_2 nanosheets," *ACS Appl. Mater. Interfaces*, vol. 6, no. 23, pp. 21215–21222, 2014.

[35] C.-S. Lee *et al.*, "Fabrication of metal/graphene hybrid interconnects by direct graphene growth and their integration properties," *Adv. Electron. Mater.*, vol. 4, no. 6, 2018, Art. no. 1700624.

[36] T. Schram *et al.*, "WS_2 transistors on 300 mm wafers with BEOL compatibility," in *Proc. IEEE 47th Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2017, pp. 212–215.

[37] R. Yue *et al.*, "Nucleation and growth of WSe_2: Enabling large grain transition metal dichalcogenides," *2D Mater.*, vol. 4, no. 4, 2017, Art. no. 045019.

[38] W. Wan *et al.*, "Temperature-related morphological evolution of MoS_2 domains on graphene and electron transfer within heterostructures," *Small*, vol. 13, no. 15, 2017, Art. no. 1603549.

[39] W. H. Chae, J. D. Cain, E. D. Hanson, A. A. Murthy, and V. P. Dravid, "Substrate-induced strain and charge doping in CVD-grown monolayer MoS_2," *Appl. Phys. Lett.*, vol. 111, no. 14, 2017, Art. no. 143106.

[40] X. Li *et al.*, "Transfer of large-area graphene films for high-performance transparent conductive electrodes," *Nano Lett.*, vol. 9, no. 12, pp. 4359–4363, 2009.

[41] A. Gurarslan *et al.*, "Surface-energy-assisted perfect transfer of centimeter-scale monolayer and few-layer MoS_2 films onto arbitrary substrates," *ACS Nano*, vol. 8, no. 11, pp. 11522–11528, 2014.

[42] J. Shim *et al.*, "Water-gated charge doping of graphene induced by mica substrates," *Nano Lett.*, vol. 12, no. 2, pp. 648–654, 2012.

[43] V. V. Afanas'ev *et al.*, "(Invited) internal photoemission of electrons from 2-dimensional semiconductors," *ECS Trans.*, vol. 80, no. 1, pp. 191–201, 2017.

[44] A. Leonhardt, D. Chiappe, I. Asselberghs, C. Huyghebaert, I. Radu, and S. De Gendt, "Improving MOCVD MoS_2 electrical performance: Impact of minimized water and air exposure conditions," *IEEE Electron Device Lett.*, vol. 38, no. 11, pp. 1606–1609, Nov. 2017.

[45] L. Banszerus *et al.*, "Identifying suitable substrates for high-quality graphene-based heterostructures," *2D Mater.*, vol. 4, no. 2, 2017, Art. no. 025030.

[46] B. G. Shin *et al.*, "Indirect bandgap puddles in monolayer MoS_2 by substrate-induced local strain," *Adv. Mater.*, vol. 28, no. 42, pp. 9378–9384, 2016.

[47] C. Lee *et al.*, "Comparison of trapped charges and hysteresis behavior in hBN encapsulated single MoS_2 flake based field effect transistors on SiO_2 and hBN substrates," *Nanotechnology*, vol. 29, no. 33, 2018, Art. no. 335202.

[48] K. Novoselov, A. Mishchenko, A. Carvalho, and A. H. C. Neto, "2D materials and van der Waals heterostructures," *Science*, vol. 353, no. 6298, p. aac9439, 2016.

[49] J. H. Yu *et al.*, "Vertical heterostructure of two-dimensional MoS_2 and WSe_2 with vertically aligned layers," *Nano Lett.*, vol. 15, no. 2, pp. 1031–1035, 2015.

[50] Y. Gong *et al.*, "Vertical and in-plane heterostructures from WS_2/MoS_2 monolayers," *Nature Mater.*, vol. 13, no. 12, pp. 1135–1142, 2014.

[51] T. Yang *et al.*, "Van der Waals epitaxial growth and optoelectronics of large-scale WSe_2/SnS_2 vertical bilayer p-n junctions," *Nature Commun.*, vol. 8, no. 1, p. 1906, 2017.

[52] Y. Qian, H. Van Ngoc, and D. J. Kang, "Growth of graphene/h-BN heterostructures on recyclable pt foils by one-batch chemical vapor deposition," *Sci. Rep.*, vol. 7, no. 1, 2017, Art. no. 17083.

[53] Z. Zhang, P. Chen, X. Duan, K. Zang, J. Luo, and X. Duan, "Robust epitaxial growth of two-dimensional heterostructures, multiheterostructures, and superlattices," *Science*, vol. 357, pp. 788–792, Aug. 2017.

[54] P. K. Sahoo, S. Memaran, Y. Xin, L. Balicas, and H. R. Gutiérrez, "One-pot growth of two-dimensional lateral heterostructures via sequential edge-epitaxy," *Nature*, vol. 553, pp. 63–67, Jan. 2018.

[55] L. Tao *et al.*, "Deterministic and etching-free transfer of large-scale 2D layered materials for constructing interlayer coupled van der Waals heterostructures," *Adv. Mater. Technol.*, vol. 3, no. 5, 2018, Art. no. 1700282.

[56] S. Boandoh *et al.*, "Wafer-scale van der Waals heterostructures with ultraclean interfaces via the aid of viscoelastic polymer," *ACS Appl. Mater. Interfaces*, vol. 11, no. 1, pp. 1579–1586, 2019.

[57] D. Unuchek, A. Ciarrocchi, A. Avsar, K. Watanabe, T. Taniguchi, and A. Kis, "Room-temperature electrical control of exciton flux in a van der Waals heterostructure," *Nature*, vol. 560, no. 7718, pp. 340–344, 2018.

[58] E. V. Calman, M. M. Fogler, L. V. Butov, S. Hu, A. Mishchenko, and A. K. Geim, "Indirect excitons in van der Waals heterostructures at room temperature," *Nature Commun.*, vol. 9, no. 1, 2018, Art. no. 1895.

[59] P. Alonso-González *et al.*, "Acoustic terahertz graphene plasmons revealed by photocurrent nanoscopy," *Nature Nanotechnol.*, vol. 12, pp. 31–35, Oct. 2016.

[60] B. Yao *et al.*, "Broadband gate-tunable terahertz plasmons in graphene heterostructures," *Nature Photon.*, vol. 12, no. 1, pp. 22–28, 2018.

[61] L. Yu *et al.*, "Design, modeling, and fabrication of chemical vapor deposition grown MoS_2 circuits with E-mode FETs for large-area electronics," *Nano Lett.*, vol. 16, no. 10, pp. 6349–6356, 2016.

[62] W. Zhu, S. Park, M. N. Yogeesh, and D. Akinwande, "Advancements in 2D flexible nanoelectronics: From material perspectives to RF applications," *Flexible Printed Electron.*, vol. 2, no. 4, 2017, Art. no. 043001.

[63] X. Zhou *et al.*, "2D layered material-based van der Waals heterostructures for optoelectronics," *Adv. Funct. Mater.*, vol. 28, no. 14, 2018, Art. no. 1706587.

[64] E. Pomerantseva and Y. Gogotsi, "Two-dimensional heterostructures for energy storage," *Nature Energy*, vol. 2, Jun. 2017, Art. no. 17089.

[65] S. Yang, C. Jiang, and S.-H. Wei, "Gas sensing in 2D materials," *Appl. Phys. Rev.*, vol. 4, p. 021304, Apr. 2017.

[66] A. C. Ferrari *et al.*, "Science and technology roadmap for graphene, related two-dimensional crystals, and hybrid systems," *Nanoscale*, vol. 7, no. 11, pp. 4598–4810, Sep. 2015.

[67] N. Briggs *et al.* (Aug. 2018). "A roadmap for electronic grade 2-dimensional materials." [Online]. Available: https://arxiv.org/abs/1808.10514

[68] *International Roadmap for Devices and Systems: 2017 Edition*, IRDS, 2018.

[69] T. Agarwal *et al.*, "Benchmarking of monolithic 3D integrated MX_2 FETs with Si FinFETs," in *IEDM Tech. Dig.*, 2017, pp. 5–7.

[70] T. A. Ameen, H. Ilatikhameneh, G. Klimeck, and R. Rahman, "Few-layer phosphorene: An ideal 2D material for tunnel transistors," *Sci. Rep.*, vol. 6, Jun. 2016, Art. no. 28515.

[71] E. G. Marin, D. Marian, G. Iannaccone, and G. Fiori, "First principles investigation of tunnel FETs based on nanoribbons from topological two-dimensional materials," *Nanoscale*, vol. 9, pp. 19390–19397, Nov. 2017.

[72] G. H. Shin, B. Koo, H. Park, Y. Woo, J. E. Lee, and S.-Y. Choi, "Vertical-tunnel field-effect transistor based on a silicon–MoS_2 Three-dimensional–two-dimensional heterostructure," *ACS Appl. Mater. Interfaces*, vol. 10, no. 46, pp. 40212–40218, 2018.

[73] D. Jiménez, "Drift-diffusion model for single layer transition metal dichalcogenide field-effect transistors," *Appl. Phys. Lett.*, vol. 101, no. 24, 2012, Art. no. 243501.

[74] W. Cao, J. Kang, W. Liu, and K. Banerjee, "A compact current–voltage model for 2D semiconductor based field-effect transistors considering interface traps, mobility degradation, and inefficient doping effect," *IEEE Trans. Electron Devices*, vol. 61, no. 12, pp. 4282–4290, Dec. 2014.

[75] L. Wang *et al.*, "A unified surface potential based physical compact model for both unipolar and ambipolar 2D-FET: Experimental verification and circuit demonstration," in *IEDM Tech. Dig.*, Dec. 2017, pp. 4–31.

[76] C. Yadav, P. Rastogi, T. Zimmer, and Y. S. Chauhan, "Charge-based modeling of transition metal dichalcogenide transistors including ambipolar, trapping, and negative capacitance effects," *IEEE Trans. Electron Devices*, vol. 65, no. 10, pp. 4202–4208, Oct. 2018.

[77] B. Das and S. Mahapatra, "An atom-to-circuit modeling approach to all-2D metal–insulator–semiconductor field-effect transistors," *NPJ 2D Mater. Appl.*, vol. 2, no. 1, 2018, Art. no. 28.

[78] Y. Y. Illarionov *et al.*, "The role of charge trapping in MoS_2/SiO_2 and MoS_2/hBN field-effect transistors," *2D Mater.*, vol. 3, no. 3, 2016, Art. no. 035004.

[79] G. Arutchelvan *et al.*, "From the metal to the channel: A study of carrier injection through the metal/2D MoS_2 interface," *Nanoscale*, vol. 9, no. 30, pp. 10869–10879, 2017.

[80] B. Stampfer *et al.*, "Characterization of single defects in ultra-scaled MoS_2 field-effect transistors," *ACS Nano*, vol. 12, no. 6, pp. 5368–5375, 2018.

[81] A. Castellanos-Gomez *et al.*, "Deterministic transfer of two-dimensional materials by all-dry viscoelastic stamping," *2D Mater.*, vol. 1, no. 1, 2014, Art. no. 011002.

[82] K. Xu, Y. Wang, Y. Zhao, and Y. Chai, "Modulation doping of transition metal dichalocogenides/oxides heterostructure," *J. Mater. Chem. C*, vol. 5, no. 2, pp. 376–381, 2016.

[83] S.-S. Chee *et al.*, "Sulfur vacancy-induced reversible doping of transition metal disulfides via hydrazine treatment," *Nanoscale*, vol. 9, pp. 9333–9339, Mar. 2017.

[84] M. Liu *et al.*, "Temperature-triggered sulfur vacancy evolution in monolayer MoS2/graphene heterostructures," *Small*, vol. 13, no. 40, 2017, Art. no. 1602967.

[85] C. J. L. de la Rosa *et al.*, "Relation between film thickness and surface doping of MoS_2 based field effect transistors," *APL Mater.*, vol. 6, no. 5, May 2018, Art. no. 058301.

[86] D. Li, M. Chen, Q. Zong, and Z. Zhang, "Floating-gate manipulated graphene-black phosphorus heterojunction for nonvolatile ambipolar Schottky junction memories, memory inverter circuits, and logic rectifiers," *Nano Lett.*, vol. 17, no. 10, pp. 6353–6359, 2017.

[87] Z. Wang *et al.*, "The ambipolar transport behavior of WSe_2 transistors and its analogue circuits," *NPG Asia Mater.*, vol. 10, no. 8, pp. 703–712, 2018.

[88] N. Colthup, *Introduction to Infrared and Raman Spectroscopy*. Amsterdam, The Netherlands: Elsevier, 2012.

[89] A. Splendiani *et al.*, "Emerging photoluminescence in monolayer MoS_2," *Nano Lett.*, vol. 10, no. 4, pp. 1271–1275, Mar. 2010.

[90] G. Binnig, C. F. Quate, and C. Gerber, "Atomic force microscope," *Phys. Rev. Lett.*, vol. 56, no. 9, p. 930, Mar. 1986.

[91] A. Gaur *et al.*, "Demonstration of 2e12 cm^{-2} eV^{-1} 2D-oxide interface trap density on back-gated MoS_2 flake devices with 2.5 nm EOT," *Microelectron. Eng.*, vol. 178, pp. 145–149, Jun. 2017.

[92] X. Liu and M. C. Hersam, "Interface characterization and control of 2D materials and heterostructures," *Adv. Mater.*, vol. 30, no. 39, 2018, Art. no. 1801586.

[93] S. B. Desai *et al.*, "MoS_2 transistors with 1-nanometer gate lengths," *Science*, vol. 354, no. 6308, pp. 99–102, 2016.

[94] A. Nourbakhsh *et al.*, "MoS_2 field-effect transistor with sub-10 nm channel length," *Nano Lett.*, vol. 16, no. 12, pp. 7798–7806, 2016.

[95] Y. Liu *et al.*, "Approaching the Schottky–Mott limit in van der Waals metal–semiconductor junctions," *Nature*, vol. 557, pp. 696–700, May 2018.

[96] S.-Y. Seo *et al.*, "Writing monolithic integrated circuits on a two-dimensional semiconductor with a scanning light probe," *Nature Electron.*, vol. 1, no. 9, pp. 512–517, 2018.

[97] S. Das and J. Appenzeller, "WSe_2 field effect transistors with enhanced ambipolar characteristics," *Appl. Phys. Lett.*, vol. 103, no. 10, Sep. 2013, Art. no. 103501.

[98] S. Nakaharai, M. Yamamoto, K. Ueno, Y.-F. Lin, S.-L. Li, and K. Tsukagoshi, "Electrostatically reversible polarity of Ambipolar α-$MoTe_2$ transistors," *ACS Nano*, vol. 9, no. 6, pp. 5976–5983, 2015.

[99] L. Yang *et al.*, "High-performance MoS_2 field-effect transistors enabled by chloride doping: Record low contact resistance (0.5 $k\Omega{\cdot}\mu m$) and record high drain current (460 $\mu A/\mu m$)," in *IEEE Dig. Tech. Papers Symp. VLSI Technol. (VLSI-Technol.)*, Jun. 2014, pp. 1–2.

[100] S. Das, H.-Y. Chen, A. V. Penumatcha, and J. Appenzeller, "High performance multilayer MoS_2 transistors with scandium contacts," *Nano Lett.*, vol. 13, no. 1, pp. 100–105, 2012.

[101] K.-S. Li *et al.*, "MoS_2 U-shape MOSFET with 10 nm channel length and poly-Si source/drain serving as seed for full wafer CVD MoS_2 availability," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2016, pp. 1–2.

[102] A. Allain, J. Kang, K. Banerjee, and A. Kis, "Electrical contacts to two-dimensional semiconductors," *Nature Mater.*, vol. 14, no. 12, pp. 1195–1205, 2015.

[103] S. Wachter, D. K. Polyushkin, O. Bethge, and T. Mueller, "A microprocessor based on a two-dimensional semiconductor," *Nature Commun.*, vol. 8, p. 14948, Apr. 2017.

[104] H. Wang *et al.*, "Large-scale 2D electronics based on single-layer MoS_2 grown by chemical vapor deposition," in *IEDM Tech. Dig.*, Dec. 2012, pp. 4–6.

[105] C. Gong, L. Colombo, R. M. Wallace, and K. Cho, "The unusual mechanism of partial Fermi level pinning at metal–MoS_2 interfaces," *Nano Lett.*, vol. 14, no. 4, pp. 1714–1720, 2014.

[106] L. Yang *et al.*, "Chloride molecular doping technique on 2D materials: WS_2 and MoS_2," *Nano Lett.*, vol. 14, no. 11, pp. 6275–6280, 2014.

[107] H. M. Khalil, M. F. Khan, J. Eom, and H. Noh, "Highly stable and tunable chemical doping of multilayer WS_2 field effect transistor: Reduction in contact resistance," *ACS Appl. Mater. Interfaces*, vol. 7, no. 42, pp. 23589–23596, 2015.

[108] D. Xiang *et al.*, "Surface transfer doping induced effective modulation on ambipolar characteristics of few-layer black phosphorus," *Nature Commun.*, vol. 6, p. 6485, Mar. 2015.

[109] H.-L. Tang *et al.*, "Multilayer Graphene–WSe_2 heterostructures for WSe_2 transistors," *ACS Nano*, vol. 11, no. 12, pp. 12817–12823, 2017.

[110] S. Das, M. Dubey, and A. Roelofs, "High gain, low noise, fully complementary logic inverter based on bi-layer WSe_2 field effect transistors," *Appl. Phys. Lett.*, vol. 105, no. 8, 2014, Art. no. 083511.

[111] J.-K. Huang *et al.*, "Large-area synthesis of highly crystalline WSe_2 monolayers and device applications," *ACS Nano*, vol. 8, no. 1, pp. 923–930, 2014.

[112] N. R. Pradhan *et al.*, "Ambipolar molybdenum diselenide field-effect transistors: Field-effect and Hall mobilities," *ACS Nano*, vol. 8, no. 8, pp. 7923–7929, 2014.

[113] Y.-F. Lin *et al.*, "Ambipolar $MoTe_2$ transistors and their applications in logic circuits," *Adv. Mater.*, vol. 26, no. 20, pp. 3263–3269, May 2014.

[114] M. J. Mleczko *et al.*, "$HfSe_2$ and $ZrSe_2$: Two-dimensional semiconductors with native high-κ oxides," *Sci. Adv.*, vol. 3, no. 8, 2017, Art. no. e1700481.

[115] L. Li *et al.*, "Black phosphorus field-effect transistors," *Nature Nanotechnol.*, vol. 9, no. 5, pp. 372–377, 2014.

[116] F. Xia, H. Wang, and Y. Jia, "Rediscovering black phosphorus as an anisotropic layered material for optoelectronics and electronics," *Nature Commun.*, vol. 5, pp. 4458-1–4458-6, Jul. 2014.

[117] M. C. Robbins and S. J. Koester, "Black Phosphorus p- and n-MOSFETs with electrostatically doped contacts," *IEEE Electron Device Lett.*, vol. 38, no. 2, pp. 285–288, Feb. 2017.

[118] Y. Huang *et al.*, "Interaction of black phosphorus with oxygen and water," *Chem. Mater.*, vol. 28, no. 22, pp. 8330–8339, 2016.

[119] K. S. Novoselov *et al.*, "Two-dimensional gas of massless dirac fermions in graphene," *Nature*, vol. 438, no. 7065, pp. 197–200, Nov. 2005.

[120] L. Li and H.-S. P. Wong, "Integrating graphene into future generations of interconnect wires," in *IEDM Tech. Dig.*, Dec. 2018, pp. 5.5.1–5.5.4.

[121] W.-S. Zhao *et al.*, "Vertical graphene nanoribbon interconnects at the end of the roadmap," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2632–2637, Jun. 2018.

[122] L. Li, Z. Zhu, T. Wang, J. A. Currivan-Incorvia, A. Yoon, and H.-S. P. Wong, "BEOL compatible graphene/Cu with improved electromigration lifetime for future interconnects," in *IEDM Tech. Dig.*, Dec. 2016, pp. 5–9.

[123] J. Jiang, J. H. Chu, and K. Banerjee, "CMOS-compatible doped-multilayer-graphene interconnects for next-generation VLSI," in *IEDM Tech. Dig.*, Dec. 2018, pp. 5–34.

[124] T. Roy *et al.*, "Field-effect transistors built from all two-dimensional material components," *ACS Nano*, vol. 8, no. 6, pp. 6259–6264, 2014.

[125] Z. Chen, W. Ren, L. Gao, B. Liu, S. Pei, and H.-M. Cheng, "Three-dimensional flexible and conductive interconnected graphene networks grown by chemical vapour deposition," *Nature Mater.*, vol. 10, no. 6, pp. 424–428, 2011.

[126] R.-H. Kim *et al.*, "Stretchable, transparent graphene interconnects for arrays of microscale inorganic light emitting diodes on rubber substrates," *Nano Lett.*, vol. 11, no. 9, pp. 3881–3886, Sep. 2011.

[127] K. S. Novoselov, V. I. Fal'ko, L. Colombo, P. R. Gellert, M. G. Schwab, and K. Kim, "A roadmap for graphene," *Nature*, vol. 490, p. 192, Oct. 2012.

[128] X. Li, K. Ma, S. George, J. Sampson, and V. Narayanan, "Enabling Internet-of-Things with opportunities brought by emerging devices, circuits and architectures," in *VLSI-SoC: System-on-Chip in the Nanoscale Era—Design, Verification and Reliability*. Cham, Switzerland: Springer, 2017, pp. 1–23.

[129] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.

[130] M. Alioto, *Enabling the Internet of Things: From Integrated Circuits to Integrated Systems*. New York, NY, USA: Springer-Verlag, 2017.

[131] X. Li, K. Ma, S. George, J. Sampson, and V. Narayanan, "Enabling Internet-of-Things with opportunities brought by emerging devices, circuits and architectures," in *Proc. IFIP/IEEE Int. Conf. Very Large Scale Integr.-Syst. Chip*. Cham, Switzerland: Springer, 2016, pp. 1–23.

[132] X. Li *et al.*, "Advancing nonvolatile computing with nonvolatile NCFET latches and flip-flops," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 11, pp. 2907–2919, Nov. 2017.

[133] X. Li *et al.*, "Enabling energy-efficient nonvolatile computing with negative capacitance FET," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3452–3458, Aug. 2017.

[134] X. Liu *et al.*, "Modulation of quantum tunneling via a vertical two-dimensional black phosphorus and molybdenum disulfide p–n junction," *ACS Nano*, vol. 11, no. 9, pp. 9143–9150, Sep. 2017.

[135] D. Sarkar *et al.*, "A subthermionic tunnel field-effect transistor with an atomically thin channel," *Nature*, vol. 526, pp. 91–95, Sep. 2015.

[136] Z. Guo *et al.*, "Independent band modulation in 2D van der Waals heterostructures via a novel device architecture," *Adv. Sci.*, vol. 5, no. 9, Sep. 2018, Art. no. 1800237.

[137] Y. Balaji *et al.*, "Tunneling transistors based on MoS_2/$MoTe_2$ van der Waals heterostructures," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 1048–1055, 2018.

[138] A. Nourbakhsh, A. Zubair, M. S. Dresselhaus, and T. Palacios, "Transport properties of a MoS_2/WSe_2 heterojunction transistor and its potential for application," *Nano Lett.*, vol. 16, no. 2, pp. 1359–1366, Feb. 2016.

[139] M. Huang, S. Li, Z. Zhang, X. Xiong, X. Li, and Y. Wu, "Multifunctional high-performance van der Waals heterostructures," *Nature Nanotechnol.*, vol. 12, pp. 1148–1154, Oct. 2017.

[140] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, 2011.

[141] A. S. Verhulst *et al.*, "Perspective of tunnel-FET for future low-power technology nodes," in *IEDM Tech. Dig.*, Dec. 2015, pp. 30.2.1–30.2.4.

[142] W. G. Vandenberghe *et al.*, "Figure of merit for and identification of sub-60 mV/decade devices," *Appl. Phys. Lett.*, vol. 102, no. 1, Jan. 2013, Art. no. 013510.

[143] Y. Qiu, R. Wang, Q. Huang, and R. Huang, "A comparative study on the impacts of interface traps on tunneling FET and MOSFET," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1284–1291, May 2014.

[144] R. N. Sajjad, W. Chern, J. L. Hoyt, and D. A. Antoniadis, "Trap assisted tunneling and its effect on subthreshold swing of tunnel FETs," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4380–4387, Nov. 2016.

[145] Q. Smets *et al.*, "Calibration of bulk trap-assisted tunneling and Shockley–Read–Hall currents and impact on InGaAs tunnel-FETs," *IEEE Trans. Electron Devices*, vol. 64, no. 9, pp. 3622–3626, Sep. 2017.

[146] Á. Szabó, S. J. Koester, and M. Luisier, "*Ab-initio* simulation of van der Waals $MoTe_2$–SnS_2 heterotunneling FETs for low-power electronics," *IEEE Electron Device Lett.*, vol. 36, no. 5, pp. 514–516, May 2015.

[147] Á. Szabó, C. Klinkert, D. Campi, C. Stieger, N. Marzari, and M. Luisier, "*Ab initio* simulation of band-to-band tunneling FETs with single- and few-layer 2-D materials as channels," *IEEE Trans. Electron Devices*, vol. 65, no. 10, pp. 4180–4187, Oct. 2018.

[148] M.-H. Doan *et al.*, "Charge transport in MoS_2/WSe_2 van der Waals heterostructure with tunable inversion layer," *ACS Nano*, vol. 11, no. 4, pp. 3832–3840, Apr. 2017.

[149] T. Roy, M. Tosun, M. Hettick, G. H. Ahn, C. Hu, and A. Javey, "2D-2D tunneling field-effect transistors using WSe_2/$SnSe_2$ heterostructures," *Appl. Phys. Lett.*, vol. 108, no. 8, Feb. 2016, Art. no. 083111.

[150] R. Zhou, V. Ostwal, and J. Appenzeller, "Vertical versus lateral two-dimensional heterostructures: On the topic of atomically abrupt p/n-junctions," *Nano Lett.*, vol. 17, no. 8, pp. 4787–4792, Aug. 2017.

[151] W. Cao, J. Kang, and K. Banerjee, "(Invited) 2D/3D tunnel-FET: Toward green transistors and sensors," *ECS Trans.*, vol. 77, no. 5, pp. 185–189, Apr. 2017.

[152] A. Nourbakhsh, A. Zubair, M. S. Dresselhaus, and T. Palacios, "Transport properties of a MoS_2/WSe_2 heterojunction transistor and its potential for application," *Nano Lett.*, vol. 16, no. 2, pp. 1359–1366, Feb. 2016.

[153] J. Shim *et al.*, "Phosphorene/rhenium disulfide heterojunction-based negative differential resistance device for multi-valued logic," *Nature Commun.*, vol. 7, no. 1, Dec. 2016, Art. no. 13413.

[154] Y. Du, L. Yang, H. Liu, and P. D. Ye, "Contact research strategy for emerging molybdenum disulfide and other two-dimensional field-effect transistors," *APL Mater.*, vol. 2, no. 9, Sep. 2014, Art. no. 092510.

[155] A. Nourbakhsh, A. Zubair, S. Joglekar, M. Dresselhaus, and T. Palacios, "Subthreshold swing improvement in MoS_2 transistors by the negative-capacitance effect in a ferroelectric Al-doped-HfO_2/HfO_2 gate dielectric stack," *Nanoscale*, vol. 9, pp. 6122–6127, Apr. 2017.

[156] F. A. McGuire, Y.-C. Lin, K. Price, G. B. Rayner, S. Khandelwal, S. Salahuddin, and A. D. Franklin, "Sustained sub-60 mV/decade switching via the negative capacitance effect in MoS_2 transistors," *Nano Lett.*, vol. 17, no. 8, pp. 4801–4806, 2017.

[157] M. Si *et al.*, "Steep-slope hysteresis-free negative capacitance MoS_2 transistors," *Nature Nanotechnol.*, vol. 13, pp. 24–28, Jan. 2018.

[158] M. Si, C. Jiang, W. Chung, Y. Du, M. A. Alam, and P. D. Ye, "Steep-slope WSe_2 negative capacitance field-effect transistor," *Nano Lett.*, vol. 18, no. 6, pp. 3682–3687, May 2018.

[159] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, pp. 405–410, 2008.

[160] V. V. Zhirnov and R. K. Cavin, "Negative capacitance to the rescue?" *Nature Nanotechnol.*, vol. 3, no. 2, pp. 77–78, Feb. 2008.

[161] T. N. Theis and P. M. Solomon, "It's time to reinvent the transistor!" *Science*, vol. 327, pp. 1600–1601, Mar. 2010.

[162] A. M. Ionescu, "Negative capacitance gives a positive boost," *Nature Nanotechnol.*, vol. 13, no. 1, pp. 7–8, 2018.

[163] X. Wang *et al.*, "Two-dimensional negative capacitance transistor with polyvinylidene fluoride-based ferroelectric polymer gating," *NPJ 2D Mater. Appl.*, vol. 1, no. 1, 2017, Art. no. 38.

[164] M. Si *et al.*, "Sub-60 mV/dec ferroelectric HZO MoS_2 negative capacitance field-effect transistor with internal metal gate: The role of parasitic capacitance," in *IEDM Tech. Dig.*, vol. 6, Dec. 2017, pp. 23.5.1–23.5.4.

[165] E. Ko, H. Lee, Y. Goh, S. Jeon, and C. Shin, "Sub-60-mV/decade negative capacitance finfet with sub-10-nm hafnium-based ferroelectric capacitor," *IEEE J. Electron Devices Soc.*, vol. 5, no. 5, pp. 306–309, Sep. 2017.

[166] M. H. Lee *et al.*, "Negative capacitance FETs with steep switching by ferroelectric Hf-based oxide," in *Proc. Int. Symp. VLSI Technol., Syst. Appl. (VLSI-TSA)*, Apr. 2017, vol. 35, no. 2, pp. 6–7.

[167] A. Sharma and K. Roy, "Design space exploration of hysteresis-free $HfZrO_x$-based negative capacitance FETs," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1165–1167, Aug. 2017.

[168] M. Si, P. Y. Liao, G. Qiu, Y. Duan, and P. D. Ye, "Ferroelectric field-effect transistors based on MoS_2 and $CuInP_2S_6$ two-dimensional van der Waals heterostructure," *ACS Nano*, vol. 12, no. 7, pp. 6700–6705, 2018.

[169] J. Jo and C. Shin, "Negative capacitance field effect transistor with hysteresis-free sub-60-mV/decade switching," *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 245–248, Mar. 2016.

[170] A. Saeidi, F. Jazaeri, F. Bellando, I. Stolichnov, C. C. Enz, and A. M. Ionescu, "Negative capacitance field effect transistors; capacitance matching and non-hysteretic operation," in *Proc. Eur. Solid-State Device Res. Conf.*, 2017, pp. 78–81.

[171] X. Li *et al.*, "Emerging steep-slope devices and circuits: Opportunities and challenges," in *Beyond-CMOS Technologies for Next Generation Computer Design*. Cham, Switzerland: Springer, 2019, pp. 195–230.

[172] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Physical insights on negative capacitance transistors in nonhysteresis and hysteresis regimes: MFMIS versus MFIS structures," *IEEE Trans. Electron Devices*, vol. 65, no. 3, pp. 867–873, Mar. 2018.

[173] J.-S. Yuan, J. Lin, Q. Alasad, and S. Taheri, "Ultra-low-power design and hardware security using emerging technologies for Internet of Things," *Electronics*, vol. 6, no. 3, p. 67, 2017.

[174] S. K. Samal, S. Khandelwal, A. I. Khan, S. Salahuddin, C. Hu, and S. K. Lim, "Full chip power benefits with negative capacitance FETs," in *Proc. IEEE/ACM Int. Symp. Low Power Electron. Design (ISLPED)*, Jul. 2017, pp. 1–6.

[175] M. Alioto, "Near-threshold digital circuits for nearly-minimum energy processing," in *Enabling the Internet of Things*. Cham, Switzerland: Springer, 2017, pp. 95–148.

[176] K. K. Tiong, P. C. Liao, C.-H. Ho, and Y.-S. Huang, "Growth and characterization of rhenium-doped MoS_2 single crystals," *J. Cryst. Growth*, vol. 205, no. 4, pp. 543–547, 1999.

[177] T. Hallam *et al.*, "Rhenium-doped MoS_2 films," *Appl. Phys. Lett.*, vol. 111, no. 20, 2017, Art. no. 203101.

[178] J. Suh *et al.*, "Doping against the native propensity of MoS_2: Degenerate hole doping by cation substitution," *Nano Lett.*, vol. 14, no. 12, pp. 6976–6982, 2014.

[179] K. Dolui, I. Rungger, C. Das Pemmaraju, and S. Sanvito, "Possible doping strategies for MoS_2 monolayers: An *ab initio* study," *Phys. Rev. B, Condens. Matter*, vol. 88, no. 7, 2013, Art. no. 075420.
[180] M. R. Laskar *et al.*, "p-type doping of MoS_2 thin films using Nb," *Appl. Phys. Lett.*, vol. 104, no. 9, 2014, Art. no. 092104.
[181] G. V. Resta *et al.*, "Polarity control in WSe_2 double-gate transistors," *Sci. Rep.*, vol. 6, Jul. 2016, Art. no. 29448.
[182] P.-E. Gaillardon, L. Amaru, J. Zhang, and G. De Micheli, "Advanced system on a chip design based on controllable-polarity FETs," in *Proc. Conf. Design, Autom. Test Eur.*, 2014, p. 235.
[183] G. V. Resta, P.-E. Gaillardon, and G. De Micheli, "Functionality-enhanced devices: From transistors to circuit-level opportunities," in *Beyond-CMOS Technologies for Next Generation Computer Design*. Cham, Switzerland: Springer, 2019, pp. 21–42.
[184] J. Zhang, M. De Marchi, P.-E. Gaillardon, and G. De Micheli, "A Schottky-barrier silicon FinFET with 6.0 mV/dec Subthreshold Slope over 5 decades of current," in *IEDM Tech. Dig.*, Dec. 2014, pp. 13.4.1–13.4.4.
[185] W. Liu, J. Kang, D. Sarkar, Y. Khatami, D. Jena, and K. Banerjee, "Role of metal contacts in designing high-performance monolayer n-type WSe_2 field effect transistors," *Nano Lett.*, vol. 13, no. 5, pp. 1983–1990, 2013.
[186] V. Podzorov, M. Gershenson, C. Kloc, R. Zeis, and E. Bucher, "High-mobility field-effect transistors based on transition metal dichalcogenides," *Appl. Phys. Lett.*, vol. 84, no. 17, pp. 3301–3303, 2004.
[187] H. C. P. Movva *et al.*, "High-mobility holes in dual-gated WSe_2 field-effect transistors," *ACS Nano*, vol. 9, no. 10, pp. 10402–10410, 2015.
[188] H.-J. Chuang *et al.*, "anek, and Z. Zhou, "High mobility WSe_2 p- and n-type field-effect transistors contacted by highly doped graphene for low-resistance contacts," *Nano Lett.*, vol. 14, no. 6, pp. 3594–3601, 2014.
[189] M. Luisier *et al.*, "First-principles simulations of 2-D semiconductor devices: Mobility, I-V characteristics, and contact resistance," in *IEDM Tech. Dig.*, Dec. 2016, pp. 4–5.
[190] G. V. Resta *et al.*, "Scaling trends and performance evaluation of 2-dimensional polarity-controllable FETs," *Sci. Rep.*, vol. 7, Mar. 2017, Art. no. 45556.
[191] G. V. Resta *et al.*, "Towards high-performance polarity-controllable FETs with 2D materials," in *Proc. Design, Autom. Test Eur. Conf. Exhib. (DATE)*, Mar. 2018, pp. 637–641.
[192] T. Björkman, A. Gulans, A. V. Krasheninnikov, and R. M. Nieminen, "van der waals bonding in layered compounds from advanced density-functional first-principles calculations," *Phys. Rev. Lett.*, vol. 108, no. 23, 2012, Art. no. 235502.
[193] S. Datta, "Nanoscale device modeling: The Green's function method," *Superlattices Microstruct.*, vol. 28, no. 4, pp. 253–278, 2000.
[194] Á. Szabó, R. Rhyner, and M. Luisier, "Ab initio simulation of single- and few-layer MoS_2 transistors: Effect of electron-phonon scattering," *Phys. Rev. B, Condens. Matter*, vol. 92, no. 3, 2015, Art. no. 035435.
[195] R. B. Salazar, H. Ilatikhameneh, R. Rahman, G. Klimeck, and J. Appenzeller, "A predictive analytic model for high-performance tunneling field-effect transistors approaching non-equilibrium Green's function simulations," *J. Appl. Phys.*, vol. 118, no. 16, 2015, Art. no. 164305.
[196] C.-S. Lee, B. Cline, S. Sinha, G. Yeric, and H.-S. P. Wong, "32-bit processor core at 5-nm technology: Analysis of transistor and interconnect impact on VLSI system performance," in *IEDM Tech. Dig.*, Dec. 2016, pp. 28.3.1–28.3.4.
[197] S. V. Suryavanshi and E. Pop, "S2DS: Physics-based compact model for circuit simulation of two-dimensional semiconductor devices including non-idealities," *J. Appl. Phys.*, vol. 120, no. 22, p. 224503, 2016.
[198] T. K. Agarwal *et al.*, "Material-device-circuit co-optimization of 2D material based FETs for ultra-scaled technology nodes," *Sci. Rep.*, vol. 7, no. 1, 2017, Art. no. 5016.
[199] L. Wang *et al.*, "A surface potential based compact model for two-dimensional field effect transistors with disorders induced transition behaviors," *J. Appl. Phys.*, vol. 124, no. 3, 2018, Art. no. 034302.
[200] M. O. Li, D. Esseni, J. J. Nahas, D. Jena, and H. G. Xing, "Two-dimensional heterojunction interlayer tunneling field effect transistors (Thin-TFETs)," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 200–207, May 2015.
[201] H. Ilatikhameneh, Y. Tan, B. Novakovic, G. Klimeck, R. Rahman, and J. Appenzeller, "Tunnel field-effect transistors in 2-D transition metal dichalcogenide materials," *IEEE J. Explor. Solid-State Computat.*, vol. 1, no. 1, pp. 12–18, Dec. 2015.
[202] H. Ilatikhameneh, F. W. Chen, R. Rahman, and G. Klimeck, "Electrically doped 2D material tunnel transistor," in *Proc. IEEE Int. Workshop Comput. Electron. (IWCE)*, Sep. 2015, pp. 1–3.
[203] H. Ilatikhameneh, G. Klimeck, and R. Rahman, "Can homojunction tunnel FETs scale below 10 nm?" *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 115–118, Jan. 2016.
[204] D. E. Nikonov and I. A. Young, "Benchmarking of beyond-CMOS exploratory devices for logic integrated circuits," *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 1, no. 1, pp. 3–11, Dec. 2015.
[205] M. Shulaker *et al.*, "Three-dimensional integration of nanotechnologies for computing and data storage on a single chip," *Nature*, vol. 547, pp. 74–78, Jul. 2017.

Giovanni V. Resta (S'17) received the B.Sc. degree in electronic engineering from the University of Pisa, Pisa, Italy, in 2011, and the joint M.Sc. degree in nanotechnologies (information and communication technologies) from the Politecnico di Torino, Turin, Italy, Grenoble INP, Grenoble, France, and the Swiss Federal Institute of Technology Lausanne (EPFL), Lausanne, Switzerland, in 2015. He is currently working toward the Ph.D. degree in microtechnologies at the Integrated System Laboratory (LSI), EPFL.

His current research interests include 2-D materials for novel electronic devices and beyond-CMOS technologies.

Alessandra Leonhardt received the B.S. degree in computer engineering from the Federal University of Rio Grande do Sul, Porto Alegre, Brazil, in 2014, and the M.S. degree in electrical engineering from the University of Campinas, Campinas, Brazil, in 2016. She is currently working toward the Ph.D. degree at the Chemistry Department, Katholieke Universiteit Leuven in collaboration with imec, Leuven, Belgium.

She is involved in experimental studies in transfer and doping and physical and electrical characterization of 2-D materials.

Yashwanth Balaji received the B.E. degree in electronics and instrumentation engineering from Anna University, Chennai, India, in 2013, and the M.Sc. degree in nanoscience and nanotechnology from Katholieke Universiteit Leuven, Leuven, Belgium, in 2015. He is currently working toward the Ph.D. degree at the Department of Electrical Engineering, Katholieke Universiteit Leuven in collaboration with imec, Leuven, Belgium, with a focus on 2-D materials-based heterostructures for electronic applications.

Stefan De Gendt (SM'12) received the M.S. and Ph.D. degrees in science from the University of Antwerp, Antwerp, Belgium, in 1989 and 1996, respectively.

Since 1996, he has been with imec, Leuven, Belgium, where he is currently the Scientific Director responsible for exploratory materials and processes. Since 2003, he has also been a part-time full Professor with Katholieke Universiteit Leuven, Leuven. He has coauthored more than 800 publications (journal and proceedings) and holds several patents in semiconductor relevant fields. His current research interests include semiconductor cleaning and passivation, thin-film low- and high-*k* dielectrics and photoresists, and 2-D materials, including processing and characterization.

Pierre-Emmanuel Gaillardon (S'10–M'11–SM'16) received the Degree in electrical engineering from CPE-Lyon, Villeurbanne, France, in 2008, the M.Sc. degree in electrical engineering from INSA, Lyon, France, in 2008, and the Ph.D. degree in electrical engineering from CEA-LETI, Grenoble, France, and the University of Lyon, Lyon, France, in 2011.

He was a Research Associate with the Laboratory of Integrated Systems (Prof. G. De Micheli), Swiss Federal Institute of Technology Lausanne (EPFL), Lausanne, Switzerland, and a Visiting Research Associate with Stanford University, Palo Alto, CA, USA. He was a Research Assistant with CEA-LETI. He is currently an Assistant Professor with the Electrical and Computer Engineering Department, The University of Utah, Salt Lake City, UT, USA, where he is also an Adjunct Assistant Professor with the School of Computing and leads the Laboratory for NanoIntegrated Systems. His current research interests include the development of novel computing systems exploiting emerging device technologies and novel EDA techniques.

Dr. Gaillardon was a recipient of the C-Innov 2011 Best Thesis Award, the Nanoarch 2012 Best Paper Award, the BSF 2017 Prof. Pazy Memorial Research Award, the 2017 NSF CAREER Award, and the 2018 IEEE CEDA Pederson Award. He is an Associate Editor of the IEEE TRANSACTIONS ON NANOTECHNOLOGY. He has been serving as a TPC Member of many conferences, including the DATE 2015–2019, the DAC 2016–2018, and the Nanoarch 2012–2017, and is a Reviewer for several journals and funding agencies. He served as the Topic Co-Chair—Emerging Technologies for Future Memories—for the DATE 2017–2019.

Giovanni De Micheli (F'94) received the Degree in Nuclear Engineering from the Politecnico di Milano, Milan, Italy, in 1979, and the M.S. and Ph.D. degrees in electrical engineering and computer science from the University of California at Berkeley, Berkeley, CA, USA, 1980 and 1983, respectively.

He was a Professor of Electrical Engineering with Stanford University, Stanford, CA, USA. He is currently a Professor and the Director of the Institute of Electrical Engineering, Swiss Federal Institute of Technology Lausanne (EPFL), Lausanne, Switzerland. His current research interests include several aspects of design technologies for integrated circuits and systems, such as synthesis for emerging technologies, networks on chips, and 3-D integration.

Prof. De Micheli is a Fellow of the Association for Computing Machinery (ACM), a member of the Academia Europaea, and an International Honorary Member of the American Academy of Arts and Sciences. He was a recipient of the 2016 IEEE/CS Harry Goode Award for seminal contributions to design and design tools of networks on chips, the 2016 EDAA Lifetime Achievement Award, the 2012 IEEE/CAS Mac Van Valkenburg Award for his contributions to theory, practice, and experimentation in design methods and tools, the 2003 IEEE Emanuel Piore Award for his contributions to computer-aided synthesis of digital systems, and the D. Pederson Award for the best paper in the IEEE TRANSACTION ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUIT AND SYSTEMS (TCAD/ICAS) in 1987 and 2018.