

A 57-74GHz Tail-Switching Injection-Locked Frequency Tripler in 28nm CMOS

Lorenzo Iotti, *Member, IEEE*, Greg LaCaille, *Student Member, IEEE*, Ali M. Niknejad, *Fellow, IEEE*

Abstract—This paper presents a wideband injection-locked frequency tripler for mm-wave LO generation. Conventional class-C injection is combined with class-D tail switching, achieving significant extension of the locking range. Theoretical insights on the effectiveness of the proposed technique are provided. A 28nm CMOS prototype achieves 57-74GHz operation with 11mW power consumption, without the need of tuning or calibration.

Index Terms—mm-wave, frequency tripler, frequency multiplier, injection-locking, ILO, dual injection, tail switching

I. INTRODUCTION

High-speed mm-wave wireless links for next-generation mobile access and backhaul mandate strict phase noise requirements for Local Oscillator (LO) circuits [1]. These specifications are beyond what is commonly attainable with CMOS fundamental-frequency oscillators, due to the low quality factor (Q) of capacitive components at mm-waves. Therefore, the oscillator often runs at a subharmonic frequency, and the high-frequency LO reference is generated through a frequency multiplier [1], [2]. Injection-locked frequency multipliers (ILFM) are popular in mm-wave CMOS LO generation due to their high power efficiency [2]–[6]. However, they typically suffer from narrowband operation, due to the limited locking range (LR) of injection-locked oscillators (ILO) [4].

Several techniques have been proposed to extend the locking range of ILFM. In [3], $\sim 13\%$ LR is achieved by lowering the tank's Q, although this reduces output swing and power efficiency. Tail current modulation for LR extension is proposed in [2]; however, the measured locking range is only 480 MHz at 60GHz carrier ($<1\%$). In [4], a transformer (XFMR) is introduced in the ILO tank, increasing the LR to $\sim 17\%$. Combining this technique with a XFMR-boost of the injection current, 76% LR is obtained in [6]; however, this introduces high variations of output power across the frequency range. Finally, the ILFM operation range can be extended beyond the LR by adding tuning elements to the ILO tank [2], [4], [5]. However, tunable capacitors degrade the output swing due to limited component Q, and require calibration loops that add complexity and power overhead [7].

In this paper, we propose an injection-locked frequency tripler (ILFT) achieving 26% operation range with no tuning elements. The ILFT, shown in Fig. 1, employs two techniques. First, it features a XFMR-coupled load as in [4]. Second,

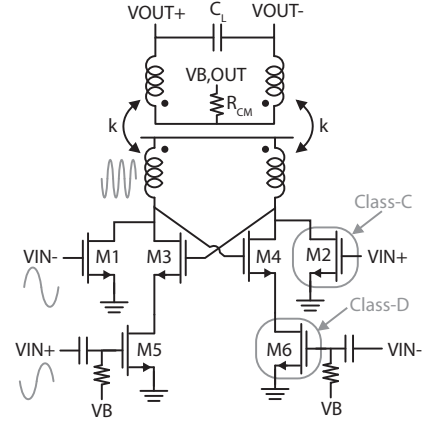


Fig. 1. Schematic of the tail-switching injection-locked frequency tripler.

it combines parallel class-C injection in the ILO tank with series class-D switching on the tail of the cross-coupled pair. In section II it is shown that if the tail transistors are hard-switched, rather than modulated in class-A as in [2], a large LR extension is obtained. An analytical model providing insights on the effectiveness of the proposed technique is developed, and shows good agreement with circuit simulations. Implemented in 28nm CMOS technology, a prototype achieves 57-74GHz operation while consuming only 11 mW.

II. TAIL SWITCHING FOR LOCKING RANGE EXTENSION

The simplified model of a conventional ILFT is shown in Fig. 2.a. Transistor M2 is biased in class-C to maximize 3rd-harmonic generation. Current and voltage phasors at 3ω , where ω is the injection angular frequency, are shown in Fig. 2.b. When the ILO works off-resonance and the phase of the tank impedance Z_T is non-zero, a phase offset between the injection current I_{inj} , the tank current I_t and the oscillator current I_{osc} is established. When $\angle Z_T$ is high enough that $\alpha=90^\circ$, the system loses lock [8]. As shown in Fig. 2.c, if a phase lag θ (or a phase lead, if $\angle Z_T < 0$) is established between I_{osc} and $-V_T$, a smaller angle $\alpha' < \alpha$ is obtained for the same $\angle Z_T$, so at given frequency offset, the ILO operates further away from the locking edge. As derived in the following, this phase correction effect is achieved in the tail-switching ILFT.

To model the proposed ILFT, an ideal switch controlled by the negative phase of the injection signal is added on the source of M1 as in Fig. 3. Assuming the oscillation swing A_{osc} is within the linearity region of M1, which is often the case at mm-waves, the circuit can be analyzed using a Linear Time-Variant (LTV) model. We assume V_{inj} is real and, since

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Authors are with the University of California, Berkeley, CA, 94704 USA (email: lorenzo.iotti@berkeley.edu, greglac@berkeley.edu, niknejad@berkeley.edu).

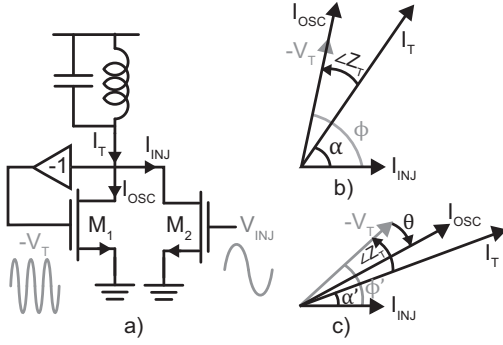


Fig. 2. (a) Simplified model of a conventional injection-locked frequency tripler. (b) Corresponding 3rd-harmonic phasors for I_{osc} in phase with $-V_T$ and (c) in case a delay θ is established between I_{osc} and $-V_T$.

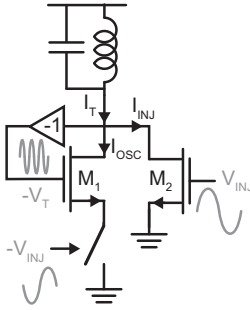


Fig. 3. Simplified model of the proposed tail-switching frequency tripler.

M2 is biased in class-C, its 3rd-harmonic current I_{inj} is in phase with V_{inj} . Assuming the tank's Q is high enough to filter undesired harmonics, the signal on the gate of M1 is $-V_T = A_{osc} \cos(3\omega t + \phi)$, where ϕ is an arbitrary phase shift between $-V_T$ and I_{inj} . The current I_{osc} can be expressed as

$$I_{osc} = [2I_{DC} + g_m A_{osc} \cos(3\omega t + \phi)] \cdot SW(t) \quad (1)$$

where I_{DC} is the DC current flowing in M1, g_m is its transconductance, and $SW(t)$ is a 50%-duty-cycle square wave in phase with $-V_{inj}$, given by

$$SW(t) = \frac{1}{2} \left\{ 1 - \frac{4}{\pi} \sum_{n=0}^{\infty} (-1)^n \frac{1}{2n+1} \cos[(2n+1)\omega t] \right\} \quad (2)$$

Isolating the 3rd-harmonic component of I_{osc} and replacing $g_m = 2I_d/V_{ov} = 4I_{DC}/V_{ov}$, where I_d is the drain current of M1 when the switch is *on*, and V_{ov} is the effective overdrive voltage, yields

$$I_{osc,3} = 2I_{DC} \left[\frac{A_{osc}}{V_{ov}} \cos(3\omega t + \phi) + \frac{2}{3\pi} \cos(3\omega t) \right] \quad (3)$$

The phase of $I_{osc,3}$ is plotted versus ϕ in Fig. 4.a, for different values of A_{osc}/V_{ov} . It can be noticed that $|\angle I_{osc,3}|$ is always lower than $|\phi|$. Therefore, as shown in Fig. 2.c, in the proposed frequency tripler I_{osc} is no longer in phase with $-V_T$, and the tail switching generates a phase correction θ that reduces the phase shift between I_{osc} and I_{inj} . As a result, the locking range is extended. Interestingly, the phase correction effect becomes stronger at low A_{osc}/V_{ov} , i.e. at the edge of the LR.

The magnitude of $I_{osc,3}$, normalized to I_{DC} , is plotted in

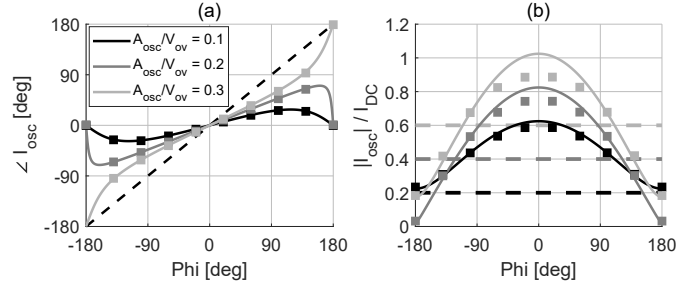


Fig. 4. (a) Phase and (b) magnitude (normalized to I_{DC}) of I_{osc} vs phase of $-V_T$. Comparison between eq. (3) (solid lines), circuit simulations (squares), and conventional ILFT (dashed lines). For a conventional ILFT, $\angle I_{osc} = \phi$ and $|I_{osc}| = g_m A_{osc}$ are assumed. The value of $\angle I_{osc}$ for $\phi = \pm 180^\circ$ (either 0° or $\pm 180^\circ$) is set by which term in eq. (3) has larger amplitude.

Fig. 4.b. Even if the ILO current drops for high phase shifts, the current efficiency is still better than a conventional ILFT for most reasonable values of ϕ . Indeed, switching the ILO DC current increases the 3rd-harmonic component of I_{osc} .

In Fig. 4, results from eq. (3) are compared with circuit simulations, with very good agreement¹. Simulations also show that if switches with resistance $r_{on} \neq 0$ are considered, eq. (3) still holds approximately true, and the phase correction effect becomes slightly stronger when r_{on} grows.

If V_{inj} , instead of $-V_{inj}$, is used to drive the switch in Fig. 3, the $+$ sign in eq. (3) turns into a $-$, and the LR is significantly decreased. However, since harmonics in eq. (2) have alternating sign, the correct choice of the switch control phase depends on the multiplication factor. For an ILFT, opposite-phase control is the optimal choice. Conversely, if the ILO is locked on the fundamental, in-phase tail switching is beneficial. For higher harmonics, the optimal choice depends on the phase relationship between I_{inj} and V_{inj} , which is a function of bias and nonlinear characteristic of M2.

It is worth noticing that if the tail transistor is driven in class-A, instead of being switched, it produces virtually no 3ω component on I_{osc} , and no phase correction is performed. In practical cases, a 3ω harmonic is still created by transistor nonlinearity, leading to the slight LR extension observed in [2].

III. CIRCUIT DESIGN

The schematic of the proposed switched-tail ILFT is shown in Fig. 1. Wide transistors ($60\mu\text{m}/30\text{nm}$) are used for M5/M6 to ensure class-D operation, while the cross-coupled MOS size is $16\mu\text{m}/30\text{nm}$. Transistors M1/M2 are also $60\mu\text{m}/30\text{nm}$ to ensure strong 3rd-harmonic injection. The gates of M5/M6 are AC coupled to the input, to allow independent bias between injection devices and tail switches. A single-turn low-k XFMR ($L_p \approx L_s = 200$ pH, $k = 0.25$) is used as a load, resulting in two advantages. First, XFMR-coupled resonators provide flat phase and magnitude on the tank impedance, which further extends the locking range and ensures wideband operation with high output swing [4], [9]. Moreover, since resistor R_{CM} lowers the common-mode Q of the secondary coil, the XFMR

¹PSS simulation with Cadence Virtuoso. To account for non-square-law devices, in simulations A_{osc} is set to be proportional to $V_{ov} = 2I_d/g_m$, where I_d and g_m are calculated from the DC operation point.

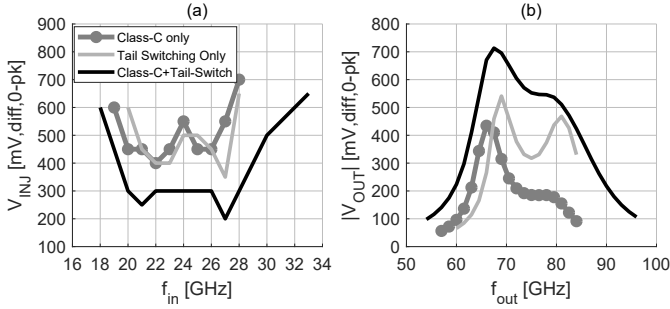


Fig. 5. (a) Simulated minimum differential input swing required to lock the ILFT vs injection frequency and (b) simulated output swing with 600mV,diff,0pk injection swing. Comparison between class-C parallel injection only, class-D tail switching only, and the proposed ILFT. Post-layout simulation results, using same MOS and XFMR size for the three cases. For tail-switching only, transistors M1/M2 are turned off. For class-C injection only, drains of M5/M6 are shorted together, and gate is set to a constant bias; in this case, the ILO DC current is reduced by $\sim 40\%$ compared to the proposed ILFT to achieve significant locking range.

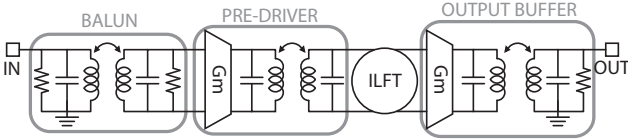


Fig. 6. Schematic of the ILFT test chip.

rejects even harmonics resulting from the mixing between the tail switch square wave and the tank voltage signal at 3ω . Circuit simulations using a realistic EM-simulated XFMR show $>15\text{dB}$ improvement in even-harmonic rejection, which results in $>20\text{dB}$ rejection on all harmonics at the ILFT output.

Fig. 5.a shows the simulated LR versus injection swing. The proposed ILFT is compared with conventional ILFTs employing only class-C parallel injection or only class-D tail injection. The proposed ILFT achieves $\sim 50\%$ LR extension, and higher output swing.

The full schematic of the test chip is shown in Fig. 6. A pre-driver, employing XFMR-coupled load for wideband operation, is added at the ILFT input to ensure sufficient injection swing. A balun is also added at the pre-driver input. Leveraging loaded high-k XFMR-coupled resonators [9], it provides over an octave matching BW with $S_{11} < -10\text{dB}$, and $\sim 1\text{dB}$ power loss. Overall, the simulated balun/pre-driver chain provides $>600\text{mV,diff,0pk}$ swing at the ILFT input over a 35% fractional BW, when driven by $P_{in}=0\text{dBm}$ input power. A high-linearity terminated output buffer, providing 1.5dB simulated power gain and -10dB voltage gain with $>45\%$ 1dB BW, is also added for measurement purposes.

IV. MEASUREMENTS

A prototype, shown in Fig. 7, was fabricated in a 28nm CMOS process. The total area is $1 \times 0.4\text{mm}^2$. The ILFT occupies $180 \times 130 \mu\text{m}^2$ and draws 11 mA from 1V supply, while the pre-driver consumes 6 mW. The chip was wirebonded on a PCB to provide supply and bias, and probes were used for input and output pads. Fig. 8 shows measured S_{11} and S_{22} .

A tone was delivered to the input pad from a E2257D signal

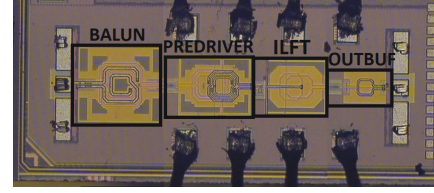


Fig. 7. Test chip microphotograph.

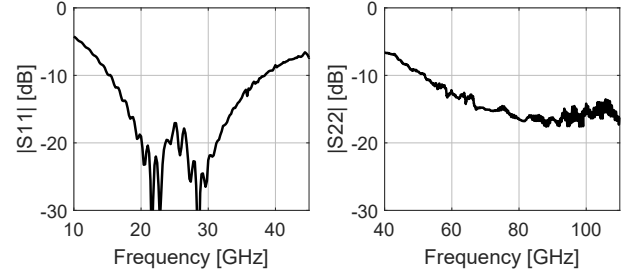


Fig. 8. Measured S_{11} and S_{22} .

generator. Cable losses were measured, and the generator power was adjusted to provide 0dBm power to the chip. To analyze the output spectrum, the signal was downconverted to baseband using an external WR10 mixer, amplified, and fed to a spectrum analyzer. A E2267D signal generator, followed by a x6 frequency multiplier, was used to drive the mixer LO.

The downconverted output spectrum with the input source turned off is shown in Fig. 9.a. A noisy free-running oscillation tone at 4.3 GHz, which corresponds to output frequency $f_{out}=68.7\text{GHz}$, is observed. Fig. 9.b shows the spectrum when a 24GHz tone is fed to the chip. A clean tone at 1 GHz, corresponding to 72GHz f_{out} , is measured, showing correct locking of the ILFT. While sweeping the input frequency f_{in} between 17 and 28GHz, a clean tone at $3f_{in}$, without any spurs due to injection pulling, was observed. The ILFT only loses lock when $P_{in} < -5\text{dBm}$.

Measured phase noise performance of the ILFT at 72GHz f_{out} is reported in Fig. 10. Phase noise spectra of the input (L_{in}) and LO (L_{LO}) signal sources were measured. For an ideal ILFT, output phase noise is $L_{out}=L_{in}+20 \log 3$ [3]. However, since the measurement is performed on the downconverted output, the LO also contributes to the noise spec-

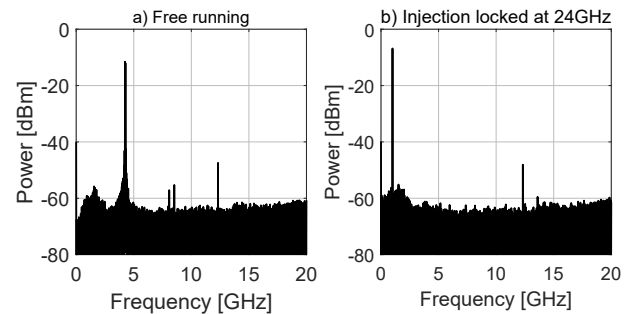


Fig. 9. Measured downconverted output spectrum of the ILFT (a) in free-running mode and (b) when injected by a 24GHz tone. A 73GHz signal is used as mixer LO. The tone at $\sim 12\text{GHz}$ is also observed when the chip is off, and is due to the LO fundamental harmonic leaking through the mixer.

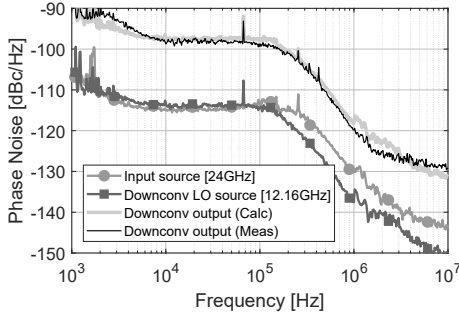


Fig. 10. Measured phase noise spectra of input and LO signal sources, and comparison between the measured phase noise at the ILFT downconverted output and results from eq. (4).

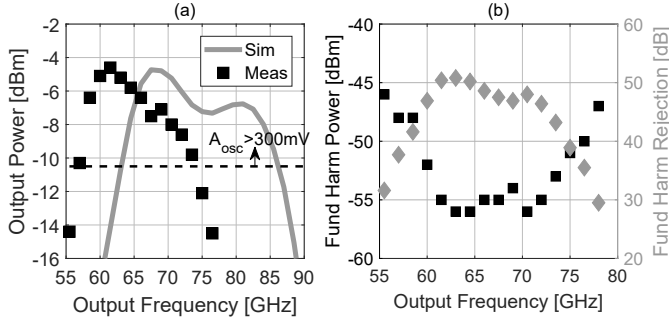


Fig. 11. (a) Measured power at the chip output (after cable loss de-embedding) and comparison with simulations. (b) Measured fundamental-harmonic output power (after cable de-embedding) and corresponding harmonic rejection.

trum. The ideal downconverted phase noise is calculated as

$$L_{out,dn} = 10 \log \left[10^{L_{out}/10} + 10^{(L_{LO} + 20 \log 6)/10} \right] \quad (4)$$

where the $20 \log 6$ factor accounts for the $\times 6$ frequency multiplier on the LO path. As shown in Fig. 10, eq. (4) shows good agreement with measurements, showing that the ILFT introduces negligible phase noise degradation. Several measurements were done over the whole ILFT operation range, showing consistent results.

Output RF power was measured using a DC-120GHz power meter, as shown in Fig. 11.a. Results show good agreement with simulations, minus a $\sim 10\%$ frequency mismatch due to process spread and mm-wave modeling inaccuracy. Considering 10dB voltage loss from the output buffer, the operation range of the ILFT, where $A_{osc} > 300\text{mV}_{diff,0pk}$, is 57-74GHz. Note that as reported above, the ILFT shows a spur-free output spectrum over a much wider range (51-84GHz). Indeed, unlike a conventional ILO, the tail-switching ILFT does not experience injection pulling even at very low A_{osc} swings. Fundamental harmonic power, measured on a spectrum analyzer, is plotted in Fig. 11.b. $>35\text{dB}$ rejection is achieved over the operation range.

Table I reports comparison with state-of-the-art CMOS ILFTs. Thanks to the tail-switching technique, the proposed ILFT covers one of the highest fractional ranges, i.e. $\sim 26\%$, with low power consumption. Although the solution in [4] covers a comparable or superior frequency range, it requires additional calibration loops to tune the ILO tank. Wider frequency ranges are reported for ILFT operating at lower

TABLE I
COMPARISON WITH STATE OF THE ART ILFTs

	This work	[2]	[3]	[4]	[5]	[6]
CMOS Node	28nm	65nm	90nm	40nm	65nm	65nm
VDD [V]	1	1.2	1	1.1	N/A	N/A
Freq Range [GHz]	57-74* (26%)	58-65.4 [‡] (12%)	56.5-64.5 [‡] (13%)	52-66 [‡] (24%)	33.9-48.2 [‡] (35%)	22.8-43.2 [†] (62%)
Freq Range (w/o Tuning)	26%	0.8%	13%	17%	35%	62%
Output Power Variation [dB]	<6	N/A	<10.9	N/A	N/A	>30
Input	Diff	Diff	Quad	Quad	Quad	Diff
Output	Diff	Quad	Quad	Quad	Diff	Diff
P_{DC} [mW]	11	14.4-52.8	23.8	37	16.8	5

* Defined by minimum output swing

[‡] Defined by locking range

[†] Defined by lack of phase noise degradation

frequencies. However, [5] requires four injection phases to generate a differential output, resulting in power and area overhead, while [6] suffers from $>30\text{dB}$ variation in the output power, which calls for power-hungry output buffers and makes the output tone sensitive to noise and interference.

V. CONCLUSIONS

A 57-74GHz ILFT combining conventional class-C injection with class-D tail switching is presented. The proposed technique extends the locking range of injection-locked frequency multipliers, ensuring reliable operation over a wide frequency range without requiring any calibration loops.

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