Evaluation of 1.2 kV SiC MOSFETs in Multilevel Cascaded H-bridge Three-phase Inverter for Medium-voltage Grid Applications

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Abstract: A study is conducted to evaluate 1.2 kV silicon-carbide (SiC) MOSFETs in a cascaded H-bridge (CHB) three-phase inverter for medium-voltage applications. The main purpose of this topology is to remove the need for a bulky 60 Hz transformer normally used to step up the output signal of a voltage source inverter to a medium-voltage level. Using SiC devices (1.2-6.5 kV SiC MOSFETs) which have a high breakdown voltage, enables the system to meet and withstand the medium-voltage stress using only a minimal number of cascaded modules. The SiC-based power electronics when used in the presented topology considerably reduce the complexity usually encountered when Si devices are used to meet the medium-voltage level and power scalability. Simulation and preliminary experimental results on a low-voltage prototype verifies the nine-level CHB topology presented in this study.

Keywords: SiC switching devices, cascaded h-bridge inverter, medium voltage AC grid, energy storage

1 Introduction

The use of power electronic interfaces to integrate renewable sources and battery energy storage systems (BESS) in medium-voltage (MV) grids has garnered attention both in industry and academia. To meet the requirements of MV, paralleling [1], or connecting converter cells in series instead of through power semiconductors is a well-known approach [2-5]. A typical example using a series connection of converter cells is the cascaded H-bridge (CHB) topology. This modular approach can cope with any grid voltage by increasing the number of cascaded modules. However, the circuit structure of a CHB is naturally modular, and the control structure is highly centralized, which makes the overall system more complex. This involves communication of extensive information, complex submodule management, and the need for high-bandwidth links for pulse width modulation (PWM) transmission.

The implementation of a modular control presents certain challenges, namely, coordination schemes and the synchronization of PWM signals. To address these challenges, silicon-carbide (SiC) devices are used to take advantage of higher voltage ratings, resulting in a considerably reduced number of submodules. This in turn lowers the total component count and simplifies the control and management system. Using SiC devices, as shown in Fig. 1 provides higher temperature capability, resulting in relaxed cooling requirements for the BESS interface. The topology of the nine-level three-phase CHB inverter is fixed throughout the evaluation of SiC devices (1.2-6.5 kV). In this study, the nine-level SiC-based three-phase CHB inverter is proposed to achieve the following two goals: i) considerably reduce the number of submodules for the CHB topology, and ii) reduce the complexity of the control algorithms for medium-voltage applications of up to 13.8 kV.

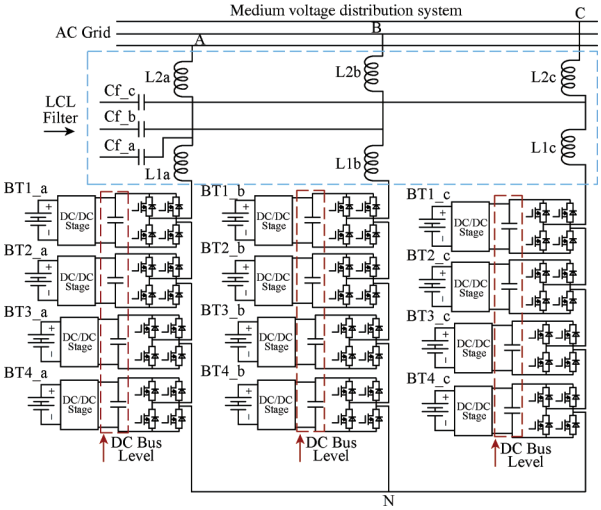

Fig. 1 Nine-level cascaded H-bridge three-phase inverter for a modular battery energy storage system

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The SiC devices are evaluated in a modular nine-level three-phase CHB inverter to take advantage of their beneficial properties such as high-voltage operation, higher thermal conductivity, and higher switching frequency, as shown in Fig. 2 [6-7]. The SiC material has a higher bandgap than Si, enabling SiC power devices to operate at higher junction temperatures. The higher breakdown field of SiC also enables higher voltage blocking capability with practical material thickness. Higher thermal conductivity reduces the thermal resistance to heat dissipation.

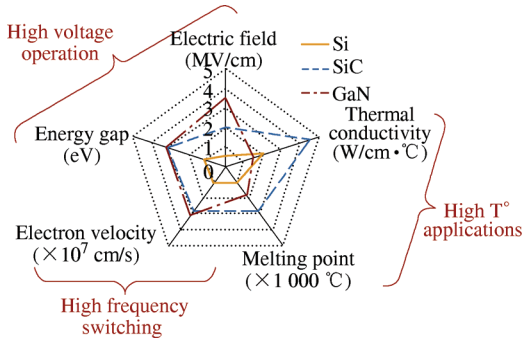

Fig. 2 Wide bandage device benefits

In medium-voltage and high-power applications, the switching frequency can be extended from less than 1 kHz with Si devices to several kHz with SiC devices, enabling higher control bandwidth and potentially reduced filter requirements. In this study, through the use of 1.2 kV SiC MOSFETs, the inverter switching frequency is 8 kHz.

This remainder of the paper is organized as follows: Section 2 provides a description of the topology of the nine-level CHB, and Section 3 presents the DC bus requirement for a design with a minimal number of modules. Section 4 describes the effect of the switching frequency and output filter, Section 5 presents the isolation required for both the gate drivers and signal sensing network for the feedback loop. Section 6 discusses the distributed control and the strategy to balance the battery system state of charge (SOC). Section 7 describes the design principles for developing an MV cabinet for the nine-level CHB used in BESS. Simulation and experimental results are discussed in Section 8. The paper provides a conclusion in Section 9.

2 Topology description

The topology shown in Fig. 1 is specifically selected to integrate the BESS into an AC medium-voltage distribution system. The inverter is the core element of any BESS as it charges and discharges batteries to store or provide power based on application requirements such as frequency control, peak shaving, energy shifting, and voltage control. The optimized number of modules per phase for the inverter to generate a 13.8 kV RMS AC three-phase output voltage is three. As reported in Ref. [8], four modules per phase are selected to add another degree of freedom for fault resiliency purposes. A three-level three-phase CHB inverter uses the lowest number of modules. However, it is not considered for this design, as it requires a DC bus voltage level that is higher than the breakdown voltage (≥10 kV) of SiC MOSFETs considered in this study.

Refs. [9-10] reviewed and compared the most popular power electronic converters for a utility-scale BESS. A three-phase CHB inverter using Si switching devices that turn on and off at a very low switching frequency (i.e., lower than 1 kHz) was reported to be the most suitable topology for BESS. When SiC devices are used in a three-phase CHB inverter, they present the advantage of either significantly improving the converter efficiency or reducing the number of modules per phase, as reported in Ref. [8]. By taking advantage of the breakdown voltage of SiC MOSFETs (i.e., up to 10 kV), the number of modules per phase can be reduced to two for a 13.8 kV medium-voltage application. By applying SiC MOSFETs, the device's maximum feasible switching frequency $f_{sw,dev}$ can be increased. With a reduced number of modules, the optimized switching frequency should be evaluated.

Many energy storage power converters use a bulky 60-Hz step-up transformer like the AEG Power Solutions BESS inverter shown in Fig. 3 [11-12]. To eliminate this transformer, considerable effort has been invested in developing transformer-less converters [9-10]. For a similar purpose, Fig. 1 shows the topology studied to integrate batteries into a 13.8 kV RMS distribution system using SiC MOSFETs as switching devices. With a nine-level CHB three-phase inverter, at least a 3.5 kV DC bus is required for each module for the inverter to generate a 13.8 kV RMS voltage output. A non-isolated DC-DC stage converter as shown in Fig. 4 is used to control intelligently the

current flowing through the batteries and realize SOC balancing. With the DC-DC stage in each module, the CHB ensures a distributed control over each module, allowing the implementation of balancing schemes and inherent protection in each battery pack against over-voltage and over-current. This topology is flexible for the controller to follow a battery technology charging profile. As an example, Fig. 5 shows a lithium battery cell charging profile. For each module, a DC-DC stage follows the control algorithm scheme to regulate the battery current during both charging and discharging of the batteries, as reported in Ref. [8]. For different types of batteries, the controller adaptively follows the respective charging profile.

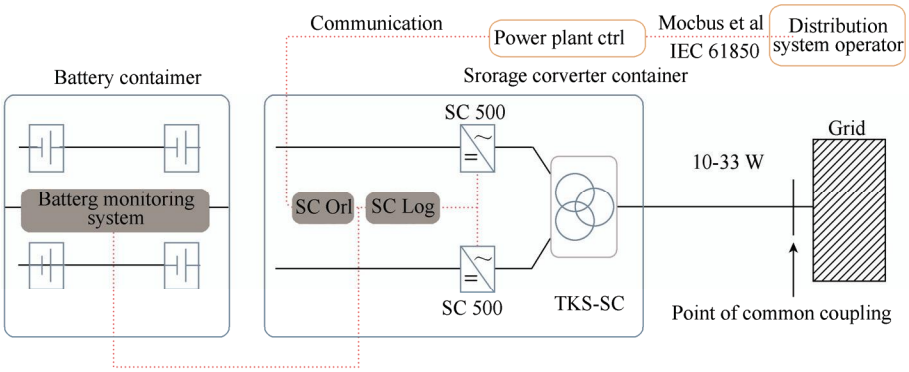

Fig. 3 Typical energy storage system layout [11-12]

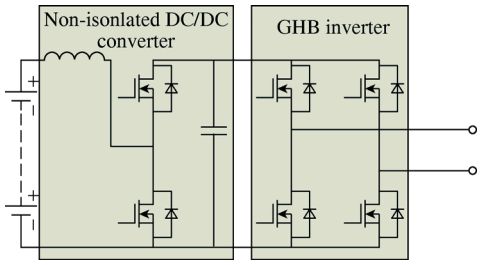

Fig. 4 Non-isolated DC/DC stage converter and CHB

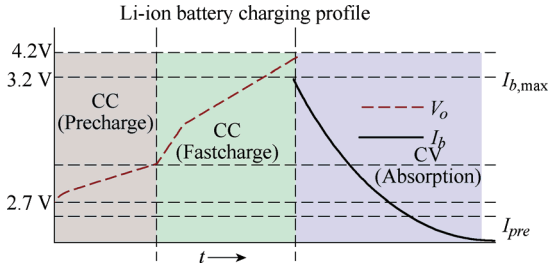

Fig. 5 Cell charging profile [41]

3 Trade-offs between minimizing the number of modules and the DC bus requirement

If 1.2 kV SiC devices are used, the DC bus is controlled and regulated at 720 V. At this DC bus voltage level, hard-switching can cause damaging over-shoot voltages. Soft-switching mechanisms and intelligent gate drivers to mitigate these conditions are recommended (see Refs. [13-18]), specifically, to prevent a possible voltage over-shoot that is higher than the device breakdown voltage. With a 720 V DC bus, at least 22 modules per phase are required for the inverter to generate a 13.8 kV RMS three-phase output. If the number of modules is set to four, such as in Fig. 1, the DC requirement is 3.5 kV. This can be increased to 4.5 kV DC bus of a seven-level CHB inverter when a fault occurs in any cell and causes it to be bypassed. The DC stage converter should be used in each cell to boost battery voltage, regulate the DC bus to a required voltage level, and control the current ripple observed by the batteries. Controlling the current ripple contributes to the reliability of the batteries.

Although reducing the number of modules for a CHB inverter minimizes control complexity, it also creates a trade-off for the DC bus requirement. A minimized number of modules results in a high-voltage DC bus requirement. For a 13.8 kV RMS voltage application, three-, five-, and seven-level CHB inverters require at least 11.3 kV, 7 kV, and 3.5 kV DC buses, respectively. Tab. 1 shows the relationship between the

Tab. 1 Trade-offs between the number of sub-modules per phase and the DC bus voltage level required for CHB to generate 13.8 kV

SiC device/ kV	DC bus voltage/ kV	# of cells per phase	# of switches (PWMs)	# of sensed signals for feedback loop
1.2	0.72	20	360	189
1.7	1.2	12	216	117
3.3	2.0	7	126	72
6.6	3.5	4	72	45
⩾10	7.0	2	36	27

SiC devices, DC bus voltage, number of cells, output voltage, number of PWM signals, and number of sensed signals required for the feedback loop.

If a conventional two-level inverter is used, the DC bus requirement for a 13.8 kV system will be even higher, specifically, approximately 20 kV DC voltage. Boosting the battery bank to 20 kV will result in a less efficient system. If the DC-DC stage is not used, multiple battery banks must be connected in series to reach 20 kV. A BESS application with a MV DC bus presents major technical challenges such as insulation. This type of high DC bus battery bank will create a coupling capacitor with respect to the ground, which will generate arc faults and high noise from capacitive coupling currents, resulting in a complex system. Moreover, a cell diagnostic method should be implemented for a large-scale battery bank[42]. To avoid the noise originating from capacitive coupling currents, lower-voltage battery banks such as the typical 400 V battery banks are used in data centers [19] are a better option. The available standards for safety as described in Refs. [20-23] are also carefully followed throughout the design. A three-phase CHB inverter with a high-power density DC-DC stage is thus the suitable choice.

For the DC-DC stage, many structures exist from which to choose. Synchronous buck/boost converters can be used as simpler versions of the DC-DC stage to regulate the current flowing through the battery with lower ripple. The disadvantage of synchronous buck/boost converters is that their gain ratio is lower. Thus, high-voltage battery banks are still required. The acceptable gain ratio for a synchronous buck boost converter is as much as three times the battery bank input voltage; otherwise, it negatively affects the system's overall efficiency. Different types of bidirectional DC-DC converters with possible higher gains have been considered in various Refs. [24-32]. To achieve a higher efficiency and wide-range of DC bus voltages for the system to be connected to 13.8 kV, a high gain step-up/down DC-DC converter with a wide-range DC bus regulation is recommended in Ref. [8]. For a more compact system that uses fewer switching devices, a current-fed dual active bridge combined with resonant functionality and soft-switching provides a better option to achieve a high step-up/down gain and a considerably reduced ripple in the current flowing into the batteries.

4 Effect of switching frequency on the output filter design

SiC power semiconductors perform much better than conventional Si components in terms of efficiency and reliability. They also provide a higher switching frequency and reduced system size and weight in a variety of applications. A major objective of many applications is to reducing their overall size in order to increase the power density. This can be achieved by: 1) increasing the switching frequency, and 2) reducing losses. However, increasing the switching frequency results in an increase in losses in hard-switched applications. Soft-switching can help mitigate this problem by reducing losses, thus making higher switching frequencies available. Higher switching frequencies in turn lead to smaller passive elements and an increase in filter size.

The challenges with high-voltage SiC MOSFET device switching at a high frequency are the high dv/dt and di/dt. Soft-switching and intelligent gate drivers are critical to limit the severity of dv/dt and di/dt problems. The requirement for switches to be turned on under a zero-voltage switching (ZVS) condition is that the output capacitance C_{oss} of the switch is fully discharged, and the body diode conducts current before the switch is turned on Refs. [46-47]. The dead-time interval between the two switches should be longer than the time required for C_{oss} to be discharged from the dc input voltage to 0 V. The C_{oss} of the selected SiC MOSFET is 1.54 nF. Formula (1) represents the relationship between the dead-time and drain-source current.

$$\Delta t = \frac{2C\Delta V}{i_{dc}} \tag{1}$$

where Δt is the dead-time interval, C_{oss} is the output capacitance, ΔV is the voltage across the output capacitor, and i_{dc} is the switch drain-source current. Since the current envelope for the selected DC/DC converter is half sinusoidal, there are intervals when the current is near zero. The transformer's magnetizing current can also discharge C_{oss}. As long

as the dead-time interval is appropriately set, ZVS during turn-on can be achieved. For bidirectional power flow, either DC-to-AC or AC-to-DC that realizes zero-current switching (ZCS) turn-off of the switches is the most fundamental issue. However, given the fact that the operating principles for both directions are not exactly the same, realizing ZCS requires an adaptive modulation technique. The bidirectional DC/DC stage is designed to realize both soft-switching conditions of ZVS and ZCS.

In addition to the soft-switching mechanism, another important part of the AC/DC converter is the inductance-capacitor-inductance (LCL) filter, which should be designed as a function of the equivalent CHB inverter switching frequency. A value of the converter-side inductor is selected based on a specified ripple current flowing through the switching devices. Then, a value of the grid-side inductance is determined as a percentage ratio of the converter-side inductor. The resonant frequency of the LCL filter should be between 10 times the grid frequency (60 Hz) and half the inverter switching frequency (8 kHz). A capacitance value of the LCL filter is selected based on the condition of reactive power absorbed by the filter. For a CHB inverter, generally the switching frequency of the inverter using a phase-shifted modulation is related to the device switching frequency by $f_{sw,inv} = 2Nf_{sw,dev}$, where N is the number of modules per phase. Knowing the phase-to-phase voltage of the grid enables the total DC voltage of the inverter to be calculated as a function of the modulation index, as shown in the following formula. With a specified operating voltage ($\mathrm{U}.V_B$) of the switching device, the number of modules required per phase can be determined as

$$V_d = \sqrt{\frac{2}{3}}\frac{V_{LL}}{ma} \qquad \text{Thus,} \qquad N = \frac{V_d}{V_B} \tag{2}$$

where V_{LL} is the inverter phase-to-phase voltage, ma is the modulation index, U is the percentage utilization of each switching device in CHB, V_B is the breakdown voltage of the switching device, and V_d is the total DC voltage.

The LCL filter design for a three-phase inverter is described in Refs. [33-37]. The designer specifies an inverter switching frequency ($f_{sw,inv}$), a total DC voltage (V_d), nominal power (P_N), nominal AC voltage (V_{LL}), the maximum allowed current ripple on the inverter-side inductor (Δi), and the maximum allowed harmonic distortion as specified by the power quality IEEE 519 standard. Moreover, when the filter is to be minimized, the basic inductance specified in Refs. [37, 45] for grid-side protection should be satisfied.

For the LCL filter shown in Fig. 1, the filter inductors on the inverter side in all phases are equal, $L_{1a} = L_{1b} = L_{1c}$. The same applies for the grid-side filter inductors, $L_{2a} = L_{2b} = L_{2c}$.

Similarly, the filter capacitors are equal for all phases, $C_{f-a} = C_{f-b} = C_{f-c}$. Fig. 6 shows a per phase equivalent model of the LCL filter, where L_C denotes the inductor on the inverter side, L_G denotes the inductor on the grid side, and CF denotes the filter capacitor. For a 10 kVA system, the design results in the following filter parameters: L_C = 1.5 mH, L_G = 500 μH, and C_F = 1 μF. Calculation of the filter parameters is accomplished in the following steps:

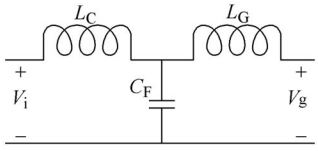

Fig. 6 Per-phase LCL filter model

The inverter-side inductor (L_C) is calculated based on the specified current ripple (Δi) through the following formula.

$$L_C = \frac{V_d}{8\Delta i\ i_{ph}\ f_{sw,inv}} \tag{3}$$

Filter capacitance (C_F) is calculated based on the specified maximum-allowed reactive power absorbed by the filter through the following formula.

$$C_F = \frac{Q_F P_N}{6\pi f_g V_{LL}^2} \tag{4}$$

The grid-side inductor (L_G) is calculated using the following formula based on a specified ripple current on the grid-side inductor (Δi_g) [33].

$$L_G = \frac{1-\Delta i_g}{\Delta i_g\ [1-(L_C C_F\left[2\pi f_{sw,inv}\right]^2)]} \tag{5}$$

5 Isolation requirements for both gate drivers and the sensing network

The PWM signal generated by the digital controller is 0 to 5 V. To turn on and off the SiC

module efficiently and fully, a gate signal from −5 to 20 V is required. The isolated gate driver is required to provide these voltage levels. The ground on the low-voltage digital controller and the high-voltage power ground should be separated by an isolation barrier. As shown in Fig. 7, the driver for the upper switch with S_Up1a at a source connection of the upper MOSFET is separated from the gate driver of the lower switch with S_Ls1a as a source point of the lower MOSFET. The digital ground must be isolated from each MOSFET source. Isolation of the power supply for each gate driver must also be able to isolate the effect of the dv/dt from the primary DC source. In addition, the barrier for both the gate driver and power supply must be able to withstand the highest blocking voltage of the SiC MOSFET. Moreover, for a cascaded structure of the topology in Fig. 1, all the DC buses should be isolated from each other. The isolation within the gate drivers, the power supplies, and the sensing network circuitry must be present and robust to withstand any possible stress derived from faults at high-voltage power areas of the topology. The isolated hall effect LEM sensors are used in this study.

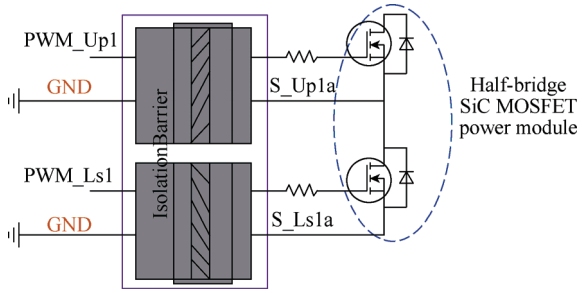

Fig. 7 Isolation barrier required for the gate driver of SiC MOSFETs

The gate driver from Wolfspeed (part # CGD15HB62LP [44]) is used to drive the half-bridge SiC MOSFET power module[43]. The SiC MOSFET power module switches at speeds beyond what is customarily associated with insulated gate bipolar transistor (IGBT)-based modules. Special precautions must be taken to realize the best performance. The interconnection between the gate driver and module must be as short as possible to afford the best switching time and avoid potential device oscillations. Fiber optics provides high transient immunity for the digital signals from the switching dv/dt and di/dt of the MOSFET. Furthermore, great care is required to ensure minimum inductance between the module and DC link capacitors to avoid excessive drain-to-source voltage overshoots. Details on minimizing the effect of parasitics when laying out the circuit into the cabinet will be provided in the next study. Mitigating the dv/dt and di/dt issues using active gating and shoot-through protection in an intelligent gate driver is reported in Refs. [13-17]. In addition, the soft-switching mechanism for high-voltage SiC modules is analyzed in Ref. [18].

Another issue under high switching speeds (i.e., high dv/dt) is the so-called “cross-talk” effect, where the turn-on of one device may increase the potential of the gate of the complementary device. If the gate voltage of the complementary device rises above the threshold voltage, this may trigger a false turn-on and lead to a shoot-through failure. The high-voltage transient (dv/dt) is applied across the Miller capacitance of the bottom device during the top device turn-on. The resulting current causes a voltage drop on the gate and internal resistances of the gate driver, which increases the gate voltage. To avoid a false turn-on of the power device, a negative gate voltage is applied (−5 V) during the off-state[48]. The higher dv/dt and higher gate loop impedance may cause the switching devices to fail. Thus, the switching speed must be reduced. In this design, an inverter switching frequency of 8 kHz is considered. As the inverter undergoes the evaluation process with different switching devices (i.e., SiC MOSFETs from 1.2 to 10 kV), the switching frequency for each voltage level application must be evaluated to optimize the system’s overall performance.

6 Control implementation and SOC balancing

For battery SOC balancing, local distributed controllers for each cell’s DC-DC stage are implemented to monitor closely the battery bank voltages and currents and to regulate the DC bus. Three TI DSPs (TMS320F28335) are used to control each DC-DC stage converter in the respective branches of the inverter, that is, phases A, B, and C. Each DSP receives the DC bus reference voltage (DC V_{ref}) for the outer voltage loop to follow and generate the reference current for the inner current loop of each

cell control. The central (and fourth) DSP is used to execute a three-phase phase-locked-loop, direct-quadrature rotating frame control computation as well as active power and ac current control of the overall three-phase inverter. The central DSP with the feed-forward current controller[8] sends three-phase sine references to the Xilinx Artix-7 FPGA or lattice semiconductor complex programmable logic device (CPLD) from the MachXO2 device family to generate all the phase-shifted PWMs to switch on and off the 12 H-bridge cells of the inverter shown in Fig. 1. Fig. 8 shows the input signals for each control device unit. The DSP for phase A uses the sensed signals in each cell to regulate the DC bus in each cell based on the DC Vref received from the central DSP. This is performed for all four cells in each phase. For example, I_{bat_1A}, V_{bat_1A}, and V_{dc_1A} are the battery current, battery voltage, and DC bus voltage, respectively, in cell 1 of phase A. The sensed signals in cell 1 of phase B are labeled I_{bat_1B}, V_{bat_1B}, and V_{dc_1B}. The sensed signals in cell 1 of phase C are I_{bat_1C}, V_{bat_1C}, and V_{dc_1C}. In Fig. 8, the signals of one cell in each phase are only shown for illustration purposes. These three DSPs receive the same dc bus voltage reference to ensure that all batteries are charged or discharged at the same rate and automatically realize the SOC and dc bus voltage balance control required for the BESS CHB three-phase inverter.

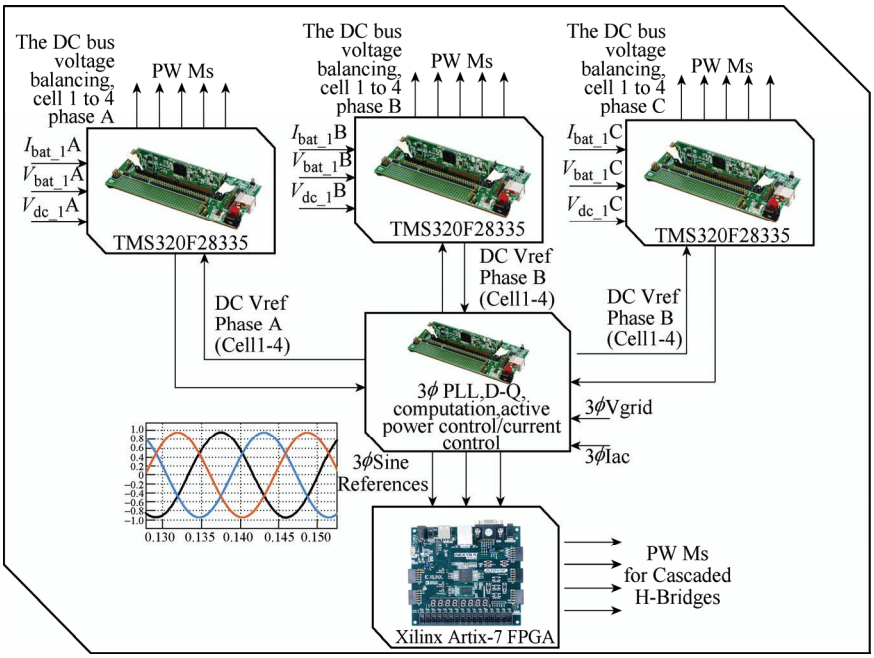

Fig. 8 DSPs and FPGA are used to implement the controls

In addition to an SOC balancing control, the designer must optimize the design for an efficient interface with a high-power density. The high DC link voltages present a challenge for integrating a BESS in a medium-voltage grid. High-voltage battery systems exist for different battery technologies. ABB built a nickel cadmium battery system in Alaska with a DC link voltage of 5 kV[38]. A lithium-ion system with a DC voltage of 5.2 kV was built in Ref. [39]. To find the optimum string voltage, different types of battery systems are considered and handled differently. Moreover, the string voltage of the battery is limited only by the isolation between the components. Safety precautions are necessary for a high-voltage DC bus higher or equal to 400 V[40] to prevent high short-circuit currents and possible arc flash incidents. Different DC-DC converter topologies can be used on the battery side. These converters make a battery management system dispensable because every cell can be operated in its optimum operating point. Another possibility is to connect the batteries in series to a high-voltage battery bank that are connected directly to only one DC-DC converter. The optimal string voltage is not a question of the battery itself. For an optimal design of the overall battery system, knowing the specific requirements of the complete system is necessary, particularly the planned application and system environment.

For batteries connected in series to provide high DC bus voltage, it becomes increasingly complex to build up compact racks with high energy density. A major challenge for setting up of the storage system is based on the fact that specifications for high-voltage applications are not available for different battery technologies. To ensure secure operation of the batteries placed in the shelves at MVs, the dielectric parameters of the components and electric fields should be investigated. Dielectric tests for the batteries and insulation measurements for low-voltage components such as the monitoring system should be verified to realize a secure and reliable operation. To ensure the insulation required for the battery bank and to avoid the complexity of connecting multiple battery banks in series for a DC MV, a 400 V battery bank is selected and boosted to 3.5 kV for a nine-level CHB three-phase inverter to generate the 13.8 kV voltage output. A DC-DC converter with a 9x gain ratio is designed to provide both isolation and monitoring systems for each battery bank, as discussed in Ref. [8].

7 Cabinet-level design considerations at medium voltages

This section describes the design principles for developing an MV cabinet for a nine-level CHB used in BESS. The cabinet level should be carefully designed in terms of insulation and safety for medium-voltage applications. Considerations for both clearance and creepage should be made based on the related standards. The design stages at the cabinet level include the submodule, capacitor bank, EMI, gate drivers, and controllers to ensure an optimized design. Various standards have been reviewed to identify the MV requirements. Creepage, clearance, and material breakdown requirements have been investigated for medium-voltage PCB design according to IPC 2221B, UL840, and IEC 60664-1 standards.

The main assembly units of the two submodules are displayed in Fig. 9. Fig. 1 shows that the inverter consists of 12 submodules, four in each phase. Each submodule is a full-bridge inverter, which is composed of two Cree/Wolfspeed 1.2 kV SiC MOSFET power modules. Each pair of submodules is mounted on a single heat sink for design optimization and to minimize the cost, as shown in Fig. 9.

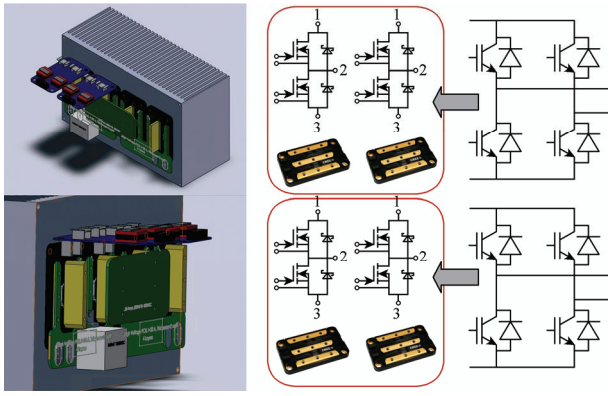

Fig. 9 Schematic for two CHB cells

Additional constraints, including the smoothness of the corners to ensure a low E-field, are imposed in the design. The positive and negative terminals of each submodule are connected to the DC link through a small bus bar. The DC link for each submodule is rated for 840 V and consists of four 3 300 μF/420 V capacitors connected in parallel and series to reduce the equivalent series inductance. Fig. 10 shows the two submodules along with their heat sinks. The gate drives are used to provide the –5 V/20 V gate-source voltage necessary for switching the power MOSFETs. The minimum distance between the gate-source of a power module and that of the gate drivers is ensured by the mounting design to lower the parasitic capacitance.

Fig. 10 Two CHB cells

To guarantee safety and lower parasitics, a 1.2 kV 0.3 μF decoupling capacitor is connected between the drains of the upper MOSFETs and sources of the lower MOSFETs in each submodule. The decoupling capacitor is connected as close as possible to the power modules to enhance parasitic reduction. The two submodules are isolated using alumina ceramic substrate sheets. A power printed circuit board (PCB) is designed and employed as an interface between the two power modules of each submodule, as shown in Fig. 11.

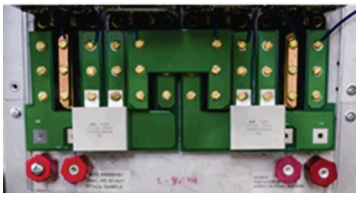

Fig. 11 Hardware design for 2 H-bridges

All 12 submodules in the three-phase design are displayed in Fig. 12. The DC bus in phase B was removed from this figure to provide a clear view of the entire system. As Fig. 10 shown, the four submodules corresponding to each phase are arranged horizontally for easier maintenance and replacement. A total of 48 capacitors comprise the DC link. Paper-based laminations are used between the DC bus layers to reduce the creepage requirements.

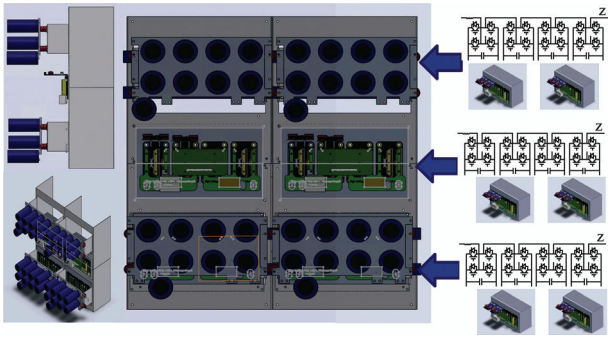

Fig. 12 Cabinet design for the nine-level CHB

8 Simulation and experimental results

Matlab Simulink is used to verify the operation of the nine-level CHB inverter. Fig. 13 presents the simulation results of the inverter output voltage for a 208 V grid line before and after the filter was added. Fig. 14 and Tab. 2 present the fast Fourier transform analytical results of the inverter output voltage after the filter was added. Inverter output voltage total

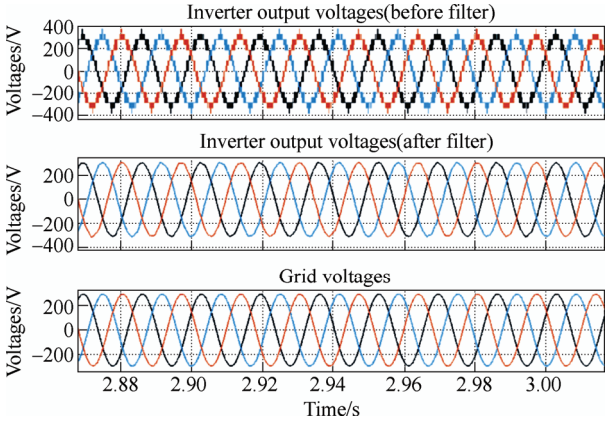

Fig. 13 Simulation results for 208 Vrms, 3Φ

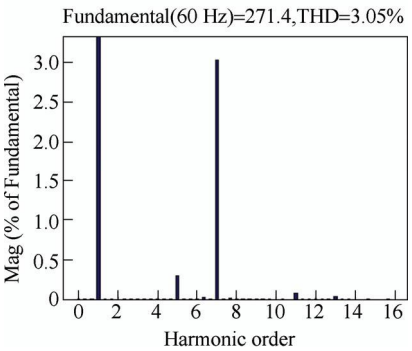

Fig. 14 FFT Analysis at $f_{sw,\,nv}$ = 100 kHz

Tab. 2 Evaluation of the output filter

Filter	Inverter switching frequency $f_{sw,inv}$ / kHz	Rated power/ kVA	Output voltage V_{LL} / V	THD /(%)
LCL	100	10	208	3.05

harmonic distortion (THD) when the inverter was operated at a switching frequency f_{sw} of 100 kHz was 3.05%. Similarly, the passive elements in each DC-DC stage were determined by the switching frequency.

A scaled-down prototype of the topology as illustrated in Fig. 1 was designed and tested. The gate drivers for every module were independently tested, as shown in Fig. 15 and 16. Fig. 16 shows the gate pulse signals (+20 V, −5 V) required to switch the 1.2 kV MOSFETs on and off. The inverter was tested at 208 Vrms, which was a three-phase USA standard of 60 Hz. Fig. 17 shows the preliminary experimental results of the inverter output voltage before the filter was added in phase A. The inverter output voltage after the LCL filter CH3 was added is displayed in Fig. 18. In Fig. 18,

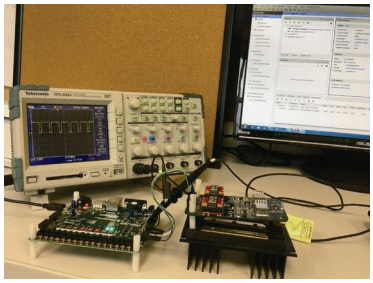

Fig. 15 Xilinx Artix-7 FPGA

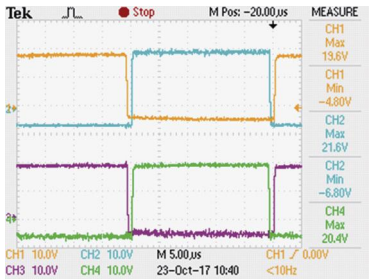

Fig. 16 Gate driver signals for the H-bridge

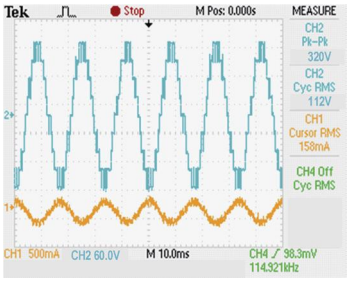

Fig. 17 Output voltage, phase A

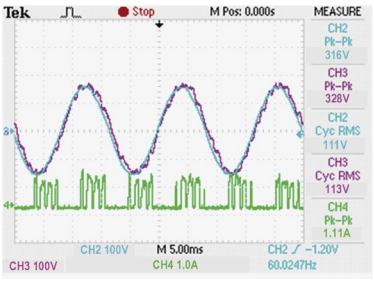

Fig. 18 Phase A, grid-connected test

CH4 shows the current flowing into the H-bridge of one of the cells in phase A when the inverter was operating in discharge mode for the BESS to send power to the grid. The prototype was evaluated at three-phase 208 Vrms (60 Hz).

Fig. 19 shows the cabinet-level implementation including all 12 full H-bridge submodules as well as the contactors, fuses, and circuit breakers, which were all populated in one cabinet. As previously mentioned, the details of the cabinet-level design and implementation ensure a packaging with minimized parasitic effects and cover the insulation requirements of power electronic interfaces in medium-voltage applications. To reach a 3.5 kV output voltage, the DC bus at each submodule should be at least 720 V.

Fig. 19 CHB cabinet-level implementation

Lead acid batteries of 400 V were used to provide the required DC bus. It is worth mentioning that the connection of the batteries provided sufficient insulation to reduce the common mode voltage when using isolated fiberglass to reduce the creepage distance requirement.

The universal control board (UCB) shown in Fig. 20 was designed by the National Center for Reliable Electric Power Transmission (NCREPT). The UCB utilizes interchangeable embedded controllers integrated on daughter cards compatible with industry standard dual in-line memory module connectors. The I/O from each of the embedded controllers is routed using the fabric of a CPLD for increased flexibility. This configuration enables each external I/O port and on-board peripheral to be controlled from any of the embedded devices. Furthermore, a dual-port RAM and communications bus were instantiated in the CPLD, which allows for reliable communication between multiple embedded devices. Finally, this approach allows for common peripheral boards such as the fiber-optic interface, voltage and current sensing, and thermocouple sensing to be standardized, which facilitates the development of a flexible controller/peripheral ecosystem, thus lending itself well to rapid development and prototyping.

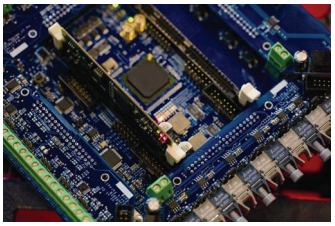

Fig. 20 Universal control board

A differential transceiver was designed to send the PWM signals from the controller to the gate drivers to ensure a reduced electromagnetic interference (EMI) effect on the signals, as shown in Fig. 21. This is a more cost-effective solution as compared with fiber cable and can be accomplished by converting the signals generated by the controller from single-ended to differential. This means each PWM signal is transmitted as a differential pair, which greatly increases noise immunity.

Fig. 21 Eight channel transceivers

Two tests were conducted to evaluate the performances of the SiC MOSFETs for the BESS cabinet-level implementation. Fig. 22 and 23 show the output voltages for the 480 V nine-level and 1 000 V five-level CHBs, respectively.

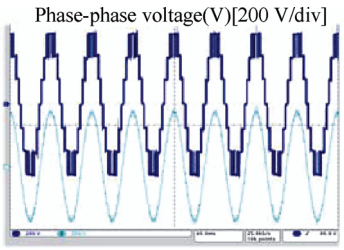

Fig. 22 480-V CHB output voltage

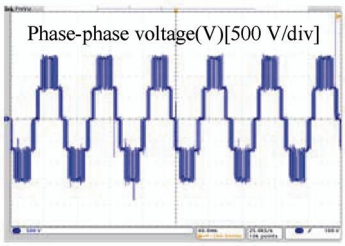

Fig. 23 1-kV CHB output voltage

9 Conclusions

This study conducted a low-voltage verification of a nine-level cascaded H-bridge three-phase inverter proposed for the integration of a BESS into a medium-voltage distribution system. SiC MOSFETs of 1.2 kV were used for a low-voltage prototype up to 3.5 kV. High-voltage SiC MOSFETs of 6.5 kV or 10 kV may be used in nine-level CHB three-phase inverters to interface the BESS to a 13.8 kV line. In this study, a filter for the inverter was analyzed with an 8 kHz inverter switching frequency. The THD in the output three-phase AC signal was verified to be within the specifications of the IEEE 519 standard. Soft-switching mechanisms and intelligent gate drivers were considered to mitigate the high dv/dt and di/dt issues derived from the high switching frequency of high-voltage SiC devices. The design for an MV cabinet for a nine-level CHB used in a BESS was discussed. The cabinet level should be carefully designed with respect to insulation and safety for medium-voltage applications.

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