Evaluation of a Medium-Voltage Grid-Tied Cascaded H-Bridge for Energy Storage Systems Using SiC Switching Devices

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Abstract— **This paper presents the study and evaluation of a medium-voltage grid-tied cascaded H-bridge (CHB) three-phase inverter for battery energy storage systems using SiC devices as an enabling technology. The high breakdown voltage capability of SiC devices provide the advantage to significantly minimize the complexity of the CHB multilevel converter, with less power loss compared to when Silicon (Si) devices are used. The topology in this study has been selected based on high voltage SiC devices. In order to reach 13.8 kV, a nine-level CHB is needed when using 6.5 kV SiC MOSFETs. However, if 10 kV SiC MOSFETs are used, only five-levels of the CHB are required. The controls were developed, simulated and verified through an experimental prototype. The results from the scaled-down prototype proved the controls and the verification of the performance of five-level CHB three-phase inverter. For the system reliability, both open-loop and short-circuit faults are analyzed.**

I. Introduction

For medium-voltage grid-tied battery energy storage systems (BESS), multilevel inverter topologies present significant advantages and increased power ranges compared to conventional topologies. Among the different kinds of multilevel inverters, the cascaded H-bridge (CHB) is suitable for integrating BESS into medium voltage distribution grids [1]. A CHB provides advantages such as scaling up to higher voltages from low voltage battery arrays without the need of a line transformer. Also in the event of faults, the modular structure of the CHB allows a battery pack to be reconfigurable and taken out of inverter. This strategy increases the reliability of the BESS. The CHB structure provides an easy grid connection with minimal filter requirements [2]-[3]. One trade-off of the CHB topology is its highly centralized control structure, thus making the control relatively complex [4]. This is due to the fact that a large amount of information is required to establish coordination between the submodules. The structure of the CHB is comprised of large numbers of modules cascaded in series to reach a medium voltage rating (e.g., 13.8 kV). The use of the wide-bandgap devices provides the advantage of higher blocking voltages. Their application will reduce the number of cells and simplify the system's control scheme. For example, if 1.2 kV SiC MOSFETs are used to integrate the BESS to the 13.8 kV distribution line, it will require a 29-level cascaded H-bridge inverter. Whereas it will only require a nine-level CHB if 6.5 kV SiC MOSFETs are used, and five levels if 10 kV SiC MOSFETs are used. In this paper, a CHB three-phase inverter with the lowest number of cells per-phase is designed and verified through the low-voltage experimental prototype. In addition to the controls, the analysis of a fault detection method is presented.

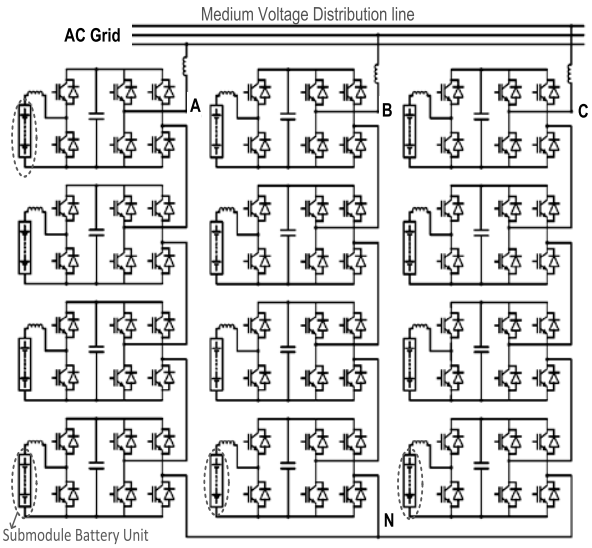

Fig. 1: Nine Level CHB, with integrated high-gain dc/dc converters.

II. Topology Description

Fig. 1 shows the nine-level topology that is studied in this paper. Wide bandgap (WBG) devices, such as SiC MOSFETs, are becoming an enabling technology for medium voltage converters. There has been significant effort put into the evaluation of these systems [5]-[6]. In the work reported in this paper, a SiC five-level CHB is being analyzed as a potential transformerless topology to connect the BESS to the 13.8 kV power line. Its success results in a simplified topology without the complexity that is usually faced when Si power semiconductor devices are used. Generally for a CHB inverter with *n* cells per phase, it produces a staircase voltage per phase with *(2n+1)* levels that are*: (2n) E,(2n-1) E, (2n-2)E,...,(1)E,(0)E,-(1)E,-(2)E,...,-(2n-1)E,-(2n+1) E.*. The output voltage of the cascaded H-bridge is the sum of all cells' individual output voltages. As Fig. 2 shows, the output voltage of a single-phase cascaded H-bridge with *n* cells is the sum of voltages from v_{H1} to v_{Hn}. To reach 13.8 kV in a three-phase 5-level inverter, a 7 kV dc bus voltage is required for each submodule. There are two ways to reach this dc voltage level; either connect multiple battery banks in series or to use lower voltage battery banks with a medium-voltage high-frequency

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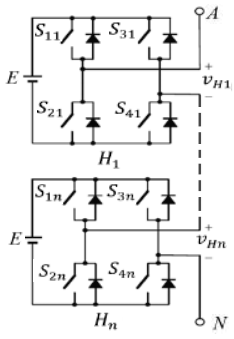

Fig. 2: *n*-Level CHB.

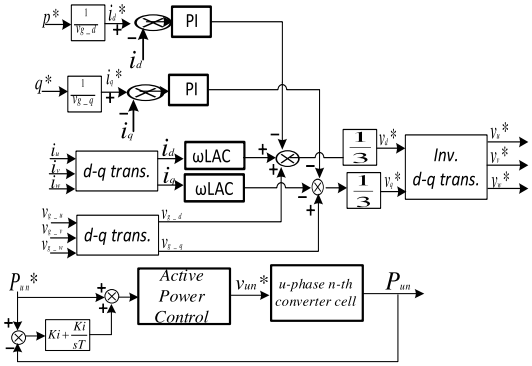

Fig. 3. Decoupled current control and active power control [8].

solid state transformer (SST) converter to boost the battery voltage to the medium dc voltage (7 kV). This paper analyzes the design of the CHB with the assumption that a 7 kV dc bus voltage is provided by either method described above.

III. Operation of The CHB

A. The Control Mechanism

The decoupled current control and voltage feedforward control are used for the CHB three-phase inverter to generate balanced three-phase voltages for both discharging and charging modes, as shown in Fig. 3. The corresponding *dq* reference voltages and currents are also generated to control the power that the inverter supplies during discharging mode, or received during the charging mode [7]-[8]. There are a variety of PWM techniques that have been used with cascaded H-bridge multilevel inverters such as Level-Shifted Pulse Width Modulation (LS-PWM), Phase-Shifted Pulse Width Modulation (PS-PWM), nearest level control (NLC), and selective harmonics elimination. LS-PWM provides lower total harmonic distortion (THD) when it is compared with other modulation techniques. The modulation strategy is key not only for lower THD, but also better voltage balancing. PS-PWM is the most functional and practical to be used with the cascaded H-bridge inverter. That is, when using the PS-PWM with a cascaded H-bridge multilevel inverter for a battery energy storage system, the total losses for submodules is almost equal. Moreover, the state of charge (SOC) for the batteries in CHB suffers from differences between the submodules in the case of LS-PWM. The submodules of dc side of the cascaded H-bridge multilevel inverter should be balanced in one phase, between submodules in one phase, and between phases. Battery voltage balancing within a submodule (series battery connection), submodules voltage balancing for each phase, and voltage balancing between the phases is easier and more practical with PS-PWM.

B. Meduim Voltage Battery Pack

Reaching 13.8 kV with a three-phase CHB with the minimal number of modules-per-cell presents a challenge of high dc bus requirements for each cell. A medium-voltage dc bus is required (approximately 7 kV) if the five-level CHB is used. If batteries are connected in series to reach this voltage, the system reliability will be significantly affected and the cell failure rate increases [9]. The solution to this challenge involves the design of an intelligent battery pack converter performing the dc/dc conversion to boost the battery voltages to the required dc bus voltage level. An intelligent battery pack incorporates a medium-voltage dc/dc converter, battery current limiter, and the built-in balancing control for dc bus voltage of each battery submodule and is shown in Fig.1. To reliably operate the medium-voltage dc/dc converter, the designer has to take into consideration the insulation layer for the battery bank to significantly minimize the capacitive leakage current in the system. In addition there is an isolation concern for voltages of that magnitude. The battery management system should also account for the series connection of batteries. There also needs to be a provision for monitoring the voltage and current for each battery. The batteries do not have to have the exact same charging and discharging ratio. However, it is important to provide for balanced charging of individual battery cells in order to maintain a uniform level of battery maintenance and reliability.

C. Fault Detection

Generally, the types of faults in grid-tied topologies can be classified as either internal or external faults. Internal faults occur within the converter. This could be caused by failures in the semiconductor devices (open/short-circuit switching fault), gate drivers, passive elements, PCBs, or connections. The types of external faults are shown in Fig. 4. This type of fault can happen in the grid, and induce stress inside the power electronics system. External faults also can be divided into two kinds: overvoltage and overcurrent faults. The selectivity of the grid fault protection reduces the negative impact of the faults to smallest grid region by isolating or clearing the fault as fast as possible. It can be achieved by adding more solid-state breakers, circuit breakers and/or fuses with faster tripping time. The overvoltage can be caused by switching or lightning surge transients. The overvoltage may result in damage to one or multiple semiconductor devices. First, the voltage surge could cause the drain-source voltage to exceed the breakdown voltage, resulting in semiconductor device damage or destruction. Secondly, it may cause an oscillation in the gate-source voltage, resulting in a false triggering and potentially leading to an unintentional turn-off event which could casue high overshoot voltages [10]-[13].

The large number of cells in multilevel inverters results in a higher chance for faults to occur, creating a reliability concern

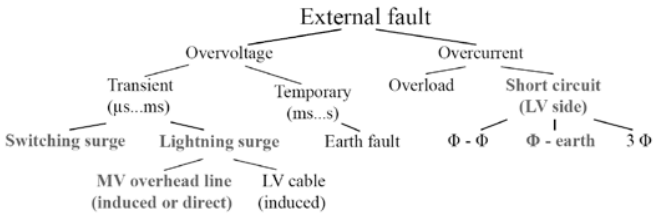

Fig. 4. External fault classification [10]

for the system. In this research there are two basic types of device failures that are considered: either a persistent short- or open-circuit device fault [14]-[15]. Overload in power electronics applications results in a short-circuit switch fault where the load current exceeds the normal operating switch current. Short-circuit switch faults may also occur when the device gate-voltage approaches the saturation voltage. Many methods have been presented to detect this type of fault within a minimum possible time and protect the switch and system from damage. This damage can be relatively expensive to repair in power electronics applications. The most well-known method for short-circuit fault protection is the desaturation protection (DESAT) technique. DESAT techniques have been set with the gate driver circuitry to shut-down the devices within a specified time when faults are detected [16]. The device voltage is measured and compared with a nominal value. In the event of a short-circuit fault, the device should be turned-off as fast as possible to prevent the high current from damaging the device. For example, the detection time and turn-off procedure for ISO5852S gate driver IC from Texas Instrument can take about 2μs [17].

Open-circuit device failures may result from gate driver faults, and wire bond lift [18]. When the number of submodules increases, the possibility of a fault occurrence also increases, and this leads to power electronics reliability issues. In battery energy storage systems, an open-circuit switch fault in the cascaded H-bridge inverter leads to an overall shutdown of the system as a consequence of unbalanced voltage and current.

The open-circuit fault detection technique for CHB described in [19] has been used. This method uses the relationship between the inverter phase currents, cell voltages and PWM signals to identify the faulty submodule and device. The output voltage and current are always measured and compered to expected values. In case of an open-circuit switch fault, the measured cell voltage and phase current are less than the typical values because of the antiparallel diode of the faulty switch.

IV. Simulation and Expermintal Results

To examine the performance of the CHB integrated into a BESS in a 60 Hz distribution system, a MATLAB/Simulink® model was created. The simulation for both grid and inverter voltages, inverter current, and the battery current, during the discharging and charging modes can be shown in Fig. 6 and Fig. 7. The simulation results verified the operability of the chosen topology. The next step is to incrementally test the topology up to medium voltage.

To evaluate the performance of the CHB interfaced to BESS, a 200 V 5-level CHB prototype has been built, as shown in Fig.8 and Fig.9. The dSPACE MicroAutoBox has been used to implement the controls. Lead-acid batteries are used in the experiment. The topology has been verified up to 200 Vpeak. The three-phase PLL is used to enable the synchronization of the inverter with the grid. This synchronization using phase locked loop control (PLL) is verified experimentally, as shown in Fig. 10. The three-phase output voltage of the CHB multilevel inverter before the filter is shown in Fig. 11. Fig. 12 shows the current flowing in the H-bridge, CH1, the grid voltage, CH2, the inverter voltage, CH3, and the battery voltage, CH4, during discharging the batteries to the grid.

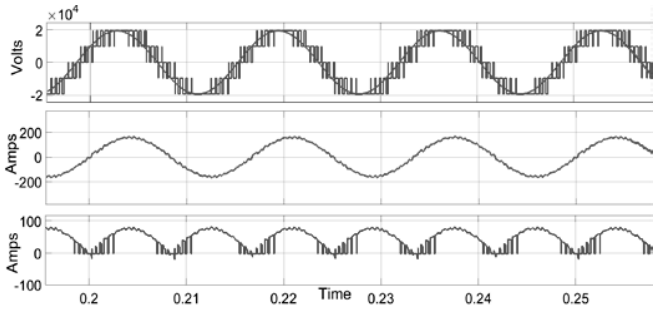

Fig. 6. Grid-inverter voltage current, and battery current during discharging mode.

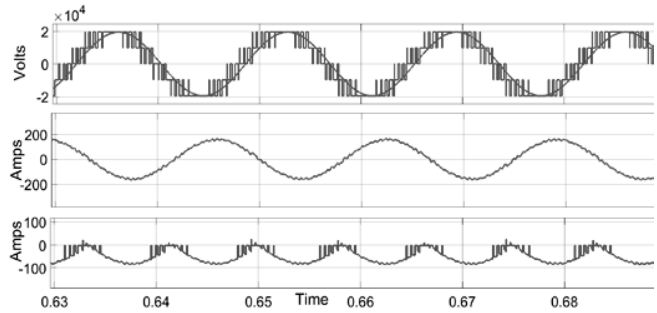

Fig. 7. Grid-inverter voltage current, and battery current during charging mode.

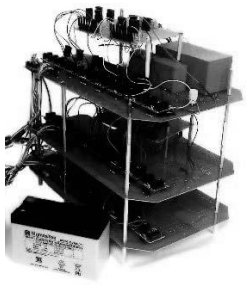

Fig. 8. Five-level CHB Fig.

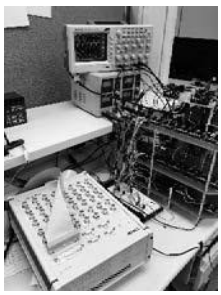

Fig. 9. Low-voltage verification

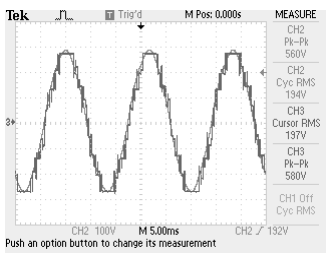

Fig. 10. Grid-Inverter synchronization.

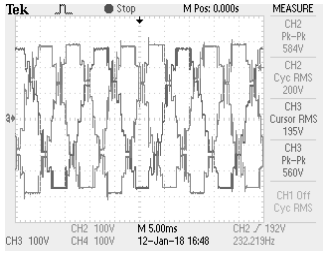

Fig. 11. Unfiltered output voltage

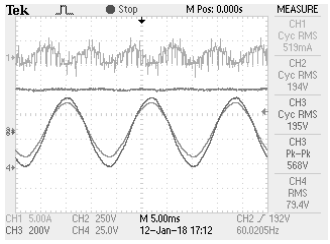

Fig. 12. Discharging mode.

Fig. 13. Detection control signal.

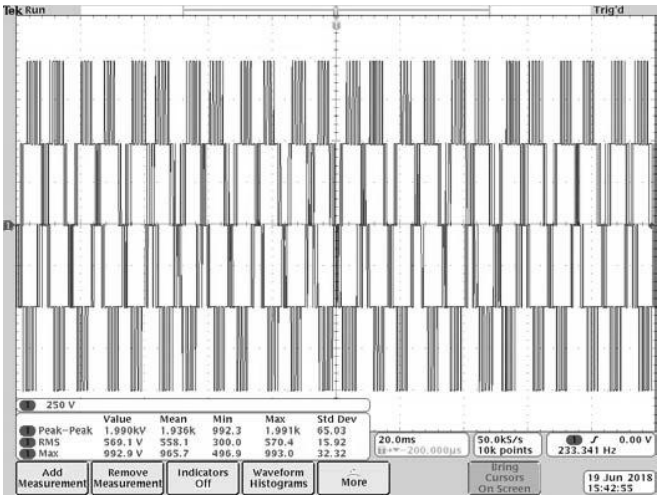

Fig. 14. CHB inverter line-line output voltage.

Another prototype has been built for 5-level CHB with 1 kV as shown in Fig. 13. 1.2 kV SiC power modules part number CAS325M12HM2, and CGD15HB62LP gate drivers from Wolfspeed/Cree have been used. This gate driver provides 20/-5 driving voltage and 14 A gate current. Logic control signal, power supply, and DESAT protection have been activated through the controllers to provide more protection for the circuit. To minimize the negative consequences of the radiated noise that is generated from fast turn-on/off switching events, differential transceiver circuits have been integrated with the gate driver. The effects of the undesired noise can be eliminated by sending the gate driver's signals as differential signals. The control has been implemented with a DSP, TI TMS320F28335. Fig. 14 shows the prototype operating at 1 kV-peak to verify the isolation capability of the gate driver.

V. Conclusions

This work evaluates a multi-level CHB for energy storage system. SiC MOSFETs are used to take advantage of their high-voltage breakdown to minimize the number of modules. The resulting topology, a five-level CHB three-phase inverter was designed and tested up to 200 V. Another prototype is to be investigated up to a medium-voltage without the use of a 60 Hz bulk line transformer. Moreover, an intelligent battery pack converter is proposed to reach the required medium dc bus voltage for each module within the presented topology.

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References

[1] P. Sochor and H. Akagi, "Which is more suitable to a modular multilevel SDBC inverter for utility-scale PV applications, phase-shifted PWM or level-shifted PWM," *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, 2016, pp. 1-7

[2] H. Akagi, "Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC)," in IEEE *Transactions on Power Electronics*, vol. 26, no. 11, pp. 3119-3130, Nov. 2011.

[3] H. Akagi, "Multilevel Converters: Fundamental Circuits and Systems," in *Proceedings of the IEEE* , vol.PP, no.99, pp.1-18 [4] S. Yang, Y. Tang, M. Zagrodnik, G. Amit and P. Wang, "A novel distributed control strategy for modular multilevel converters," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 3234-3240.

[4] L. Baruschka and A. Mertens, "Comparison of cascaded H-Bridge and modular multilevel converters for BESS application," *in Proc. IEEE Energy Convers. Congr. Expo*, Sep. 17–22, 2011, pp. 909–916

[5] S. Madhusoodhanan *et al.*, "Solid-State Transformer and MV Grid Tie Applications Enabled by 15 kV SiC IGBTs and 10 kV SiC MOSFETs Based Multilevel Converters," in *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3343-3360, July-Aug. 2015.

[6] R. Chattopadhyay *et al.*, "Low voltage PV power integration into medium voltage grid using high voltage SiC devices," *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, Hiroshima, 2014, pp. 3225-3232.

[7] L. Maharjan, T. Yamagishi and H. Akagi, "Active-Power Control of Individual Converter Cells for a Battery Energy Storage System Based on a Multilevel Cascade PWM Converter," in *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1099-1107, March 2012

[8] T. Lahlou, S. N. Malik and H. G. Herzog, "Simulation and analysis of control and modulation schemes for a multilevel cascaded H-bridge inverter for use in a battery energy storage system," 2017 18th International Scientific Conference on Electric Power Engineering (EPE), Kouty nad Desnou, 2017, pp. 1-6.

[9] E. Chatzinikolaou and D. J. Rogers, "A Comparison of Grid-Connected Battery Energy Storage System Designs," in *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 6913-6923, Sept. 2017.

[10] J. Burkard and J. Biela, "Protection of hybrid transformers in the distribution grid," 2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe), Karlsruhe, 2016, pp. 1-10.

[11] J. Fisher and D. Brealey, "SolarPro Magazine," Ungrounded PV Power Systems in the NEC: Page 3 of 12. [Online]. Available at: https://solarprofessional.com/articles/design-installation/ungrounded-pv-power-systems-in-the-nec/page/0/2. [Accessed: 18-Apr-2016].

[12] T. Guillod, F. Krismer, R. Färber, C. M. Franck and J. W. Kolar, "Protection of MV/LV solid-state transformers in the distribution grid," IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society, Yokohama, 2015, pp. 003531-003538.

[13] J. Carr, Zhenyuan Wang, S. Bhattacharya and D. Patel, "Transient overvoltage rating and BIL of the transformerless intelligent power substation," 2013 IEEE Power & Energy Society General Meeting, Vancouver, BC, 2013, pp. 1-5.

[14] J. Wang, H. Ma and Z. Bai, "A Submodule Fault Ride-Through Strategy for Modular Multilevel Converters With Nearest Level Modulation," in *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1597-1608, Feb. 2018.

[15] J. He, N. A. O. Demerdash, N. Weise and R. Katebi, "A Fast On-Line Diagnostic Method for Open-Circuit Switch Faults in SiC-MOSFET-Based T-Type Multilevel Inverters," in *IEEE Transactions on Industry Applications*, vol. 53, no. 3, pp. 2948-2958, May-June 2017

[16] H. Zhao and L. Cheng, "Open-circuit faults diagnosis in back-to-back converters of DF wind turbine," in *IET Renewable Power Generation*, vol. 11, no. 4, pp. 417-424, 3 15 2017

[17] Texas Instruments, "ISO5852S High-CMTI 2.5-A and 5-A Reinforced Isolated IGBT, MOSFET Gate Driver With Split Outputs and Active Protection Features," ISO5852S datasheet, Aug. 2015 [Revised January 2017].

[18] C. Brunson, L. Empringham, L. De Lillo, P. Wheeler and J. Clare, "Open-Circuit Fault Detection and Diagnosis in Matrix Converters," in *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2840-2847, May 20

[19] H. Mhiesan *et al.*, "A Method for Open-Circuit Faults Detecting, Identifying, and Isolating in Cascaded H-Bridge Multilevel Inverters," *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Charlotte, NC, USA, 2018, pp. 1-5.