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Sliding mode duty cycle control with current balancing algorithm for an interleaved buck converter-based PV source simulator

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Abstract: Photovoltaic (PV) source simulators are widely used to evaluate the performance of solar inverters and study their grid integration issues in the laboratory settings. Most of the commercial PV simulators are designed based on the programmable dc power supply platform. Owing to bulky output capacitors, the dynamic response and the bandwidth of these PV simulators are significantly limited, which, therefore, cannot meet the requirements to test advanced features of the solar inverters. In this study, a cost-effective high bandwidth PV simulator is proposed. A three-phase interleaved buck converter is utilised as the power stage and a novel sliding mode duty-cycle controller with auto current balancing algorithm is proposed to ensure the accurate and fast reference tracking along with phase current balancing. Both simulation and experimental studies are carried out to validate the feasibility and effectiveness of the proposed PV source simulator.

1 Introduction

In recent years, the solar energy conversion systems have been widely deployed due to their levelised cost of electricity reduction. A sustained amount of research effort has gone into the development of highly efficient, cost-effective, smart solar inverters, which further accelerates their deployment. Testing medium and high-power solar inverters using physical photovoltaic (PV) arrays along with direct solar irradiance are costly, bulky and highly dependent on weather conditions. As an alternative, PV source simulators, which can emulate the dynamic electric behaviour of PV arrays, are widely adopted to evaluate the performance of the solar inverters and study their grid integration issues in the laboratory settings.

A PV source simulator is a power conditioning system, which is designed to mimic the static and dynamic responses of actual solar cells or arrays [1, 2]. As shown in Fig. 1, a PV source simulator usually consists of three major subsystems including a reference generator, a power stage and a controller [3]. The reference generator is mainly designed to generate the current and/or voltage reference for the power stage. The current versus voltage (I–V) reference curve can be obtained through either analogue approach, e.g. pilot solar cells or model-based approach, e.g. digital reference generators.

Both linear and switching mode power converters can be utilised as the power stages in the PV simulator. The linear power stage was very popular over a long time due to their fast dynamic response [4]. However, they are limited to the low-power applications, due to their low efficiency. In high-power applications, the efficient switching mode power converters are more attractive. Various switching mode power stages have been designed for PV simulators, e.g. single-phase buck converter [5], three-phase voltage and current source rectifier [6], half and/or full-bridge converters [7, 8], resonant dc–dc converter [9] etc. There are various commercial PV simulators available on the market and most of them are programmable dc power supplies. Owing to the bulky output capacitors, the dynamic response and the bandwidth of these PV simulators are significantly limited, which, therefore, cannot meet the requirements to test of advanced inverter control algorithms, e.g. the ripple-based maximum power point tracking (MPPT).

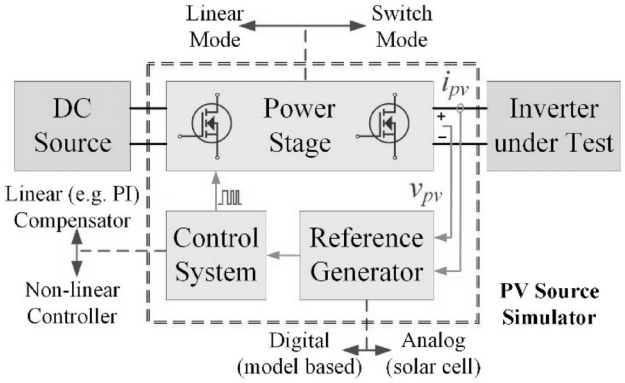

Fig. 1 *Overall block diagram of a PV source simulator*

The control system, which regulates the output of the power stage, has crucial effects on the performance of the PV simulator. A well-designed controller can ensure a fast dynamic response, short transient period etc. Tons of control methods have been designed [10] for switch mode power stages, among which the linear compensators, e.g. the proportional–integral (PI) controller, are the most commonly used. Since the design of PI controller is based on classic converter small-signal averaged models, its dynamic performance is only guaranteed around a certain equilibrium point and the system response will degrade with parametric variations. As shown in Fig. 1, the output of a PV source simulator is connected to a solar inverter under test. The operating point variation and the control mode transition of the solar inverter lead to the variation of the equivalent load impedance, which will degrade the performance of the PV simulator, if controlled by linear compensators. In addition, single-phase grid-connected solar inverters usually inject double-line frequency ac ripple back to the source. It will be challenging for linear controllers to reproduce this ripple at the output of the PV simulator.

To overcome these drawbacks, i.e. ensure robustness against the parameter variations, fast dynamic response and large signal stability, sliding mode controllers (SMCs) have been proposed and implemented for various switch mode power converters. SMC has many distinctive advantages such as the robustness against the parametric variations and external disturbances. In this paper, a novel sliding mode duty-cycle controller (SMDC) [11, 12] is proposed to regulate the output voltage of a three-phase interleaved buck converter, which serves as the power stage, leading to a highly efficient, low-cost PV simulator. Most importantly, it has high control bandwidth.

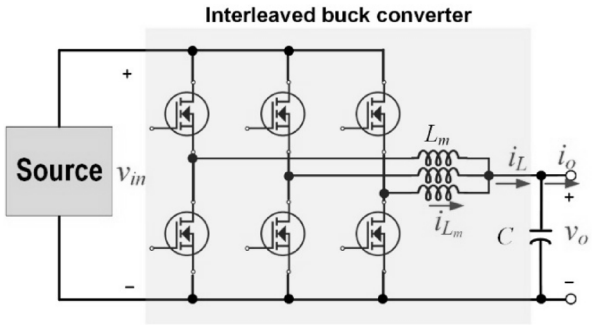

Fig. 2 *Circuit diagram of a three-phase interleaved buck converter*

To design a multi-phase converter, it is critical to balance the phase currents while maintaining total current ripple considerably low. An insignificant amount of variation in some critical phase components may cause unbalanced phase currents [13], which may further lead to unbalanced loss distribution and introduce unequal stress over various phase components. To enforce phase currents' balancing, a lot of research work has been done over the last few years to achieve appropriate current or power sharing among the converters operated in parallel [14–18]. The phase current information, which is usually obtained using current sensors, is critical to the current sharing performance. Several current-sensorless approaches have been proposed [19, 20], which, however, are sensitive to parameters of the critical components in each phase and also difficult to implement. In addition, phase current information can be reconstructed from the measured dc-link current [21]. In this paper, different from all the existing approach, differential-mode (DM) phase current information is utilised instead of using the value of actual phase current, such that the robustness to measurement errors can be significantly enhanced. Then, based on DM phase current information, a novel current balancing algorithm (CBA) is proposed to adjust the duty cycle generated by SMDC for each phase, such that balanced phase currents can be enforced.

2 Modelling and control strategy for the interleaved buck converter

In this section, the mathematical model of a generic interleaved buck converter is first presented, followed by a brief description for the PI compensator. After that, the design procedure of the proposed SMDC controller is presented. The key parameters selection approach is also discussed.

The schematic representation of a three-phase interleaved buck converter is shown in Fig. 2. The major advantage of the interleaved buck converter is the capability to reduce the output current ripple. The total output current is divided by m, which is the number of phases, to lower current stress of semiconductor devices and system conduction losses. As the ripple currents cancelled out with each other, it allows larger ripple current in each individual phase or smaller inductor size [20, 23]. This behaviour allows the controller to be designed with a fast transient response, which is desired by PV simulators. The mathematical model of a general m-phase interleaved buck converter can be expressed as

$$\begin{cases} \dfrac{\mathrm{d}i_{\mathrm{L}_k}}{\mathrm{d}t} = \dfrac{1}{L}(v_{\mathrm{in}}d_k - v_{\mathrm{o}}) \\ \dfrac{\mathrm{d}v_{\mathrm{o}}}{\mathrm{d}t} = \dfrac{1}{C}\left(\sum\limits_{k=1}^{m} i_{L_k} - \dfrac{v_{\mathrm{o}}}{R}\right) \end{cases} \tag{1}$$

where $k = 1, 2, \ldots, m$, V_{o} is the output voltage, v_{in} is the input voltage, R is the load resistance and d_k stands for the duty cycle applied to the phase k. Theoretically, due to the mismatch of the phase impedance, d_k shall be different from each other. However, in the practical application, one common duty cycle is shared among all the paralleling phases and phase-shifting pulse-width modulation (PWM) is usually utilised to generate gate signals. Therefore, in the following sections, to simplify the analysis, a single-phase buck converter model is utilised for the derivation to obtain the common duty cycle.

2.1 Conventional PI compensator design

Conventional PI compensators, designed using the converter small-signal averaged model, are commonly used to control the buck converter. The small-signal model of the converter is briefly derived as follows. Consider small perturbations in the state variables due to small disturbances in the input voltage and duty cycle

$$\begin{cases} v_{\mathrm{in}} = V_{\mathrm{in}} + \tilde{v}_{\mathrm{in}} \\ d = D + \tilde{d} \\ v_{\mathrm{o}} = V_{\mathrm{o}} + \tilde{v}_{\mathrm{o}} \\ i_L = I_L + \tilde{i}_L \end{cases} \tag{2}$$

where V_{in}, D, V_{o} and I_{L} are the average values of v_{in}, d, v_{o} and i_{L}, respectively. Substitute (2) into (1), the dynamic model of the buck converter becomes

$$\begin{cases} \dfrac{\mathrm{d}\tilde{i}_L}{\mathrm{d}t} = \dfrac{1}{L}\left[\tilde{v}_{\mathrm{in}}D + V_{\mathrm{in}}\tilde{d} - \tilde{v}_{\mathrm{o}}\right] \\ \dfrac{\mathrm{d}\tilde{v}_{\mathrm{o}}}{\mathrm{d}t} = \dfrac{1}{C}\left(\tilde{i}_L - \dfrac{\tilde{v}_{\mathrm{o}}}{R}\right) \end{cases} \tag{3}$$

Since $\tilde{i}_{\mathrm{o}} = \tilde{v}_{\mathrm{o}}/R$ following the transfer function of the buck converter system can be obtained

$$H(s) = \frac{\tilde{i}_{\mathrm{o}}}{\tilde{d}} = \frac{(V_{\mathrm{in}}/RLC)}{s^2 + (s/RC) + (1/LC)} \tag{4}$$

which is the open-loop transfer function of the buck converter system. On the basis of the system parameters given in Table 1, the frequency response of the open-loop transfer function can be obtained. Since the uncompensated system frequency response has a large crossover frequency and very limited phase margin, a PI compensator is designed to increase low-frequency loop gain and the closed-loop transfer function can be obtained as

$$C(s) = \frac{\mathrm{PI}(s) \times H(s)}{1 + \mathrm{PI}(s) \times H(s)} \tag{5}$$

where PI(s) is the transfer function of the PI compensator, PI(s) = $k_{\mathrm{p}} + k_{\mathrm{i}}/s$, k_{p} and k_{i} are PI gains. Using the closed-loop transfer function, it is possible to choose values for k_{p} and k_{i}, such that the designed compensator achieves 2 kHz crossover frequency, which will be sufficiently lower than the switching frequency 10 kHz. In this work, the PI gains are chosen as $k_{\mathrm{p}} = 0.015$ and $k_{\mathrm{i}} = 12$.

2.2 Sliding mode duty-ratio controller design

In this work, to improve the dynamic performance and also the robustness against the parametric variations, an SMDC is proposed, which will ensure the output voltage of the buck

Table 1 System parameters

Parameters	Values
input voltage (V_{in})	800 V
inductor (L)	8 mH
capacitor (C)	4 mF
load resistance (R)	20 Ω
switching frequency (f_s)	10 kHz

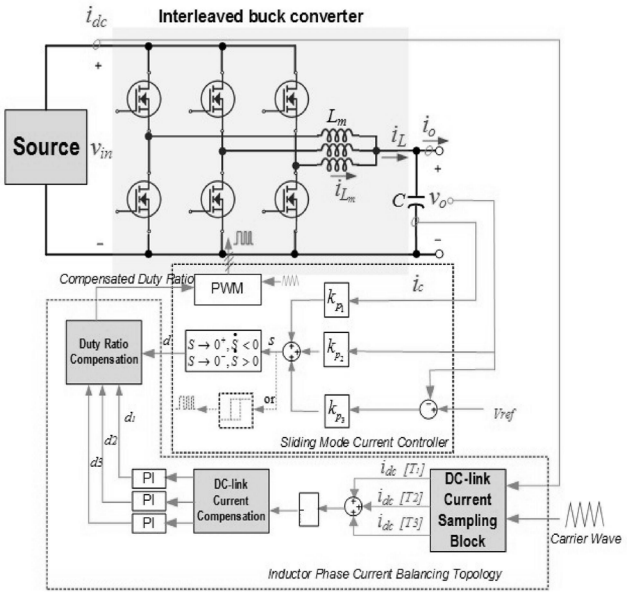

Fig. 3 *Overall block diagram of the SMDC with phase CBA*

converter accurately track the voltage reference generated by the digital reference generator. In addition, the proposed SMDC considers an additional integral term of voltage tracking error in control computation to reduce the steady-state error of the system. In this work, the control variable x can be expressed in the following form:

$$x = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} v_{\mathrm{ref}} - \beta v_{\mathrm{o}} \\ \dfrac{\mathrm{d}(v_{\mathrm{ref}} - \beta v_{\mathrm{o}})}{\mathrm{d}t} \\ \displaystyle\int (v_{\mathrm{ref}} - \beta v_{\mathrm{o}})\mathrm{d}t \end{bmatrix} \tag{6}$$

where β is the voltage sensing scaling factor, v_{ref} and v_{o} are reference and actual converter output voltages, respectively. Substituting the state-space model of the buck converter into (6) yields

$$\dot{x} = \begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & -\dfrac{1}{RC} & 0 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} 0 \\ -\dfrac{\beta v_{\mathrm{i}}}{LC} \\ 0 \end{bmatrix} u + \begin{bmatrix} 0 \\ \dfrac{\beta v_{\mathrm{o}}}{LC} \\ 0 \end{bmatrix} \tag{7}$$

In the proposed SMDC, the sliding surface is defined as

$$s = \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3 = J^{\mathrm{T}} x = 0 \tag{8}$$

where $J^{\mathrm{T}} = [\alpha_1 \ \alpha_2 \ \alpha_3]$ and α_1, α_2 and α_3 are positive coefficients. The switching control law is designed as

$$u = \begin{cases} 1, & \text{when } s > 0 \\ 0, & \text{when } s < 0 \end{cases} \tag{9}$$

To ensure controller stability and convergence to the sliding surface, the existence condition, i.e. $\dot{V} = s\dot{s} < 0$, should be always satisfied by using the proposed switching control law (9). Combining (7) and (8), it is straightforward to obtain $\dot{s}$ as

$$\dot{s} = \alpha_1 \dot{x}_1 + \alpha_2 \dot{x}_2 + \alpha_3 \dot{x}_3 = J^{\mathrm{T}} \dot{x} \tag{10}$$

Then, the following two conditions can be derived by substituting (9) into (10) to ensure $s\dot{s} < 0$:

(i) if $s >$, u will be equal to 1, and $\dot{s} < 0$, which yields

$$-\alpha_1 \frac{\beta i_{\mathrm{c}}}{C} + \alpha_2 \frac{\beta i_{\mathrm{c}}}{RC^2} + \alpha_3 (v_{\mathrm{ref}} - \beta v_{\mathrm{o}}) - \alpha_2 \frac{\beta v_{\mathrm{i}}}{LC} + \alpha_2 \frac{\beta v_{\mathrm{o}}}{LC} < 0 \tag{11}$$

(ii) if $s < 0$, u will be equal to 0, and $\dot{s} > 0$, which yields

$$-\alpha_1 \frac{\beta i_{\mathrm{c}}}{C} + \alpha_2 \frac{\beta i_{\mathrm{c}}}{RC^2} + \alpha_3 (v_{\mathrm{ref}} - \beta v_{\mathrm{o}}) + \alpha_2 \frac{\beta v_{\mathrm{o}}}{LC} > 0 \tag{12}$$

Combining (11) and (12) yield the translated existence condition

$$0 < -\beta L \left(\frac{\alpha_1}{\alpha_2} - \frac{1}{RC} \right) i_{\mathrm{c}} + LC \frac{\alpha_3}{\alpha_2} (v_{\mathrm{ref}} - \beta v_{\mathrm{o}}) + \beta v_{\mathrm{o}} < \beta v_{\mathrm{i}} \tag{13}$$

Finally, the mapping of the equivalent control function onto the duty cycle can be expressed as

$$d = \frac{-k_{p_1} i_{\mathrm{c}} + k_{p_2} (v_{\mathrm{ref}} - \beta v_{\mathrm{o}}) + k_{p_3} v_{\mathrm{o}}}{\beta v_{\mathrm{i}}} \tag{14}$$

where $k_{\mathrm{p_1}} = \beta L \left(\dfrac{\alpha_1}{\alpha_2} - \dfrac{1}{RC} \right)$, $k_{\mathrm{p_2}} = LC(\alpha_3/\alpha_2)$ and $k_{\mathrm{p_3}} = \beta$. According to the desired dynamic response or settling time, which is usually selected as 5τ (τ is the time constant). In this work, $k_{\mathrm{p1}} = 1.2425$, $k_{\mathrm{p2}} = 5$ and $k_{\mathrm{p3}} = 0.263$. The overall block diagram of the proposed SMDC is shown later in Fig. 3.

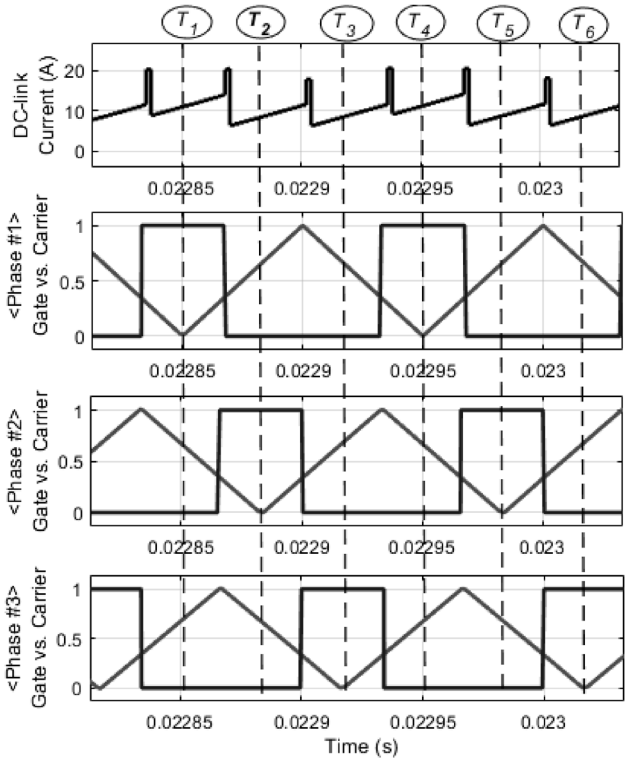

Fig. 4 *Illustration of the synchronised dc-link current sensing*

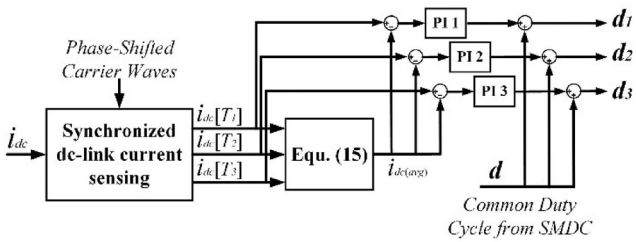

Fig. 5 *Block diagram of the proposed CBA algorithm*

3 Proposed CBA

In a multi-phase converter, equal current sharing among all the interleaved phases is anticipated in order to equalise the stresses and minimise the ratings of the phase components. With a common duty cycle, phase-shifting PWM is usually used to generate phase-shifted gate signals. For instance, gate signals of a three-phase interleaved buck converter can be generated by comparing the common duty cycle with three triangular carrier waveforms with 120° phase-shifted from each other. In this paper, R_1, R_2 and R_3 represent equivalent series resistance (ESR) of the inductors. Generally speaking, the phase current can be expressed as $i_{L_k} = (d_k v_{in} - v_o)/R_k$, where $k = 1, 2, 3$. According to the schematic representation shown in Fig. 2, the input and output voltages are the same for the three interleaved phases. Given the same duty cycle applied to each phase, the inductor current only depends on ESR. If any mismatch exists among ESRs, unbalanced phase currents will occur.

The main purpose of the proposed CBA is to maintain balanced phase currents in the interleaved converter. Usually, current sensors are required to obtain the information of phase currents to realise the CBA. Without sensing phase currents, sensorless CBA has been proposed as well. However, the converter performance is compromised due to sensitivity to converter parameters [19, 20]. As an alternative, CBA can be achieved using phase current information reconstructed based on the measured dc-link current [21, 22]. However, the accuracy of the reconstructed phase current is subjected to the measurement noises. In this paper, the proposed CBA does not rely on accurate phase currents information, while instead a DM phase current information is utilised. The proposed CBA includes a PI controller in each phase to adjust the common duty cycle generated by the SMDC, such that balanced current sharing can be enforced.

3.1 Synchronous dc-link current sensing

In this paper, the proposed CBA does not rely on accurate phase current information, such that no current sensors are needed to measure the phase currents. As shown in Fig. 4, the dc-link current mainly depends on the corresponding switching transitions in each individual phase. In this work, the dc-link current is sensed at T_1, T_2 and T_3, which are the time instants corresponding to the zero value of phases 1, 2 and 3 carrier waves, respectively. The dc-link current sensed at time instants T_1, T_2 and T_3 are $i_{dc}[T_1]$, $i_{dc}[T_2]$ and $i_{dc}[T_3]$, respectively. Then, the average value of the $i_{dc}[T_1]$, $i_{dc}[T_2]$ and $i_{dc}[T_3]$ can be calculated, which is denoted as $i_{dc(avg)}$

$$i_{dc(avg)} = \frac{i_{dc}[T_1] + i_{dc}[T_2] + i_{dc}[T_3]}{3} \tag{15}$$

3.2 CBA modelling

In this work, the difference between $i_{dc}[T_k]$, ($k = 1, 2, 3$) and $i_{dc(avg)}$ is defined as the DM phase current, i.e.

$$i_{k,\,diff} = i_{dc(avg)} - i_{dc}[T_k] \tag{16}$$

If phase currents are balanced, $i_{k,diff}$ shall be close to zero. While, if unbalanced phase currents occur, the resultant $i_{k,diff}$ will be non-zero. Therefore, (16) can be utilised to determine if there is any current imbalance or not. When phase currents are unbalanced, the $i_{k,diff}$ represents the amount of phase currents that needs to be compensated. In this paper, three PI controllers are designed to enforce the $i_{k,diff}$ to be zero, such that balanced phase currents can be automatically achieved. The block diagram of the proposed CBA is shown in Fig. 5.

4 Simulation and experimental studies

In this work, both simulation and experimental studies are carried out to validate the effectiveness of the proposed control approach as well as the resulting PV simulator. In the simulation studies, both the PI compensator and proposed SMDC are implemented for the interleaved buck converter. The comparison between the performances of two controllers is presented to show the performance enhancement brought by the proposed SMDC. In addition, the effectiveness of the proposed CBA is also validated by the simulation results. Then, the experimental results using SMDC and CBA are presented to further validate the performance of the proposed PV simulator.

4.1 Simulation results

In the simulation studies, the proposed PV simulator is connected in series with a grid-tied single-phase solar inverter, which is controlled in MPPT mode. The overall simulation model is shown in Fig. 6, where the PV solar simulator is connected to the single-phase distribution system. SMDC and CBA both are shown in Fig. 6, which were designed to control the output voltage and maintain phase current balanced for interleaved buck converter, respectively. Then, the designed PV simulator is connected to the typical single-phase distribution system, which consists of RL load. Both the PI compensator and the proposed SMDC were implemented to regulate the output voltage of the PV simulator for performance comparison purpose.

Fig. 7 shows the output voltage and currents waveforms of the PV simulator using the PI controller. Since the PV simulator is connected to a single-phase grid-tied inverter system, clear double-line frequency, i.e. 120 Hz, component can be observed in both voltage and current waveforms. Current tracking performance can be observed from the bottom figure in Fig. 7, which compares the

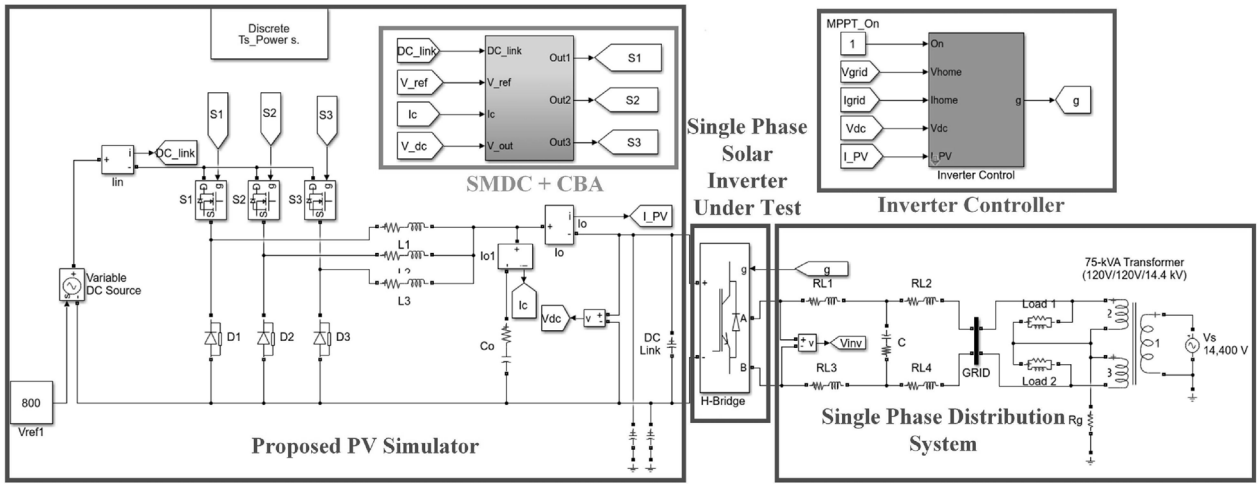

Fig. 6 *Overall Simulink model utilised in the simulation studies*

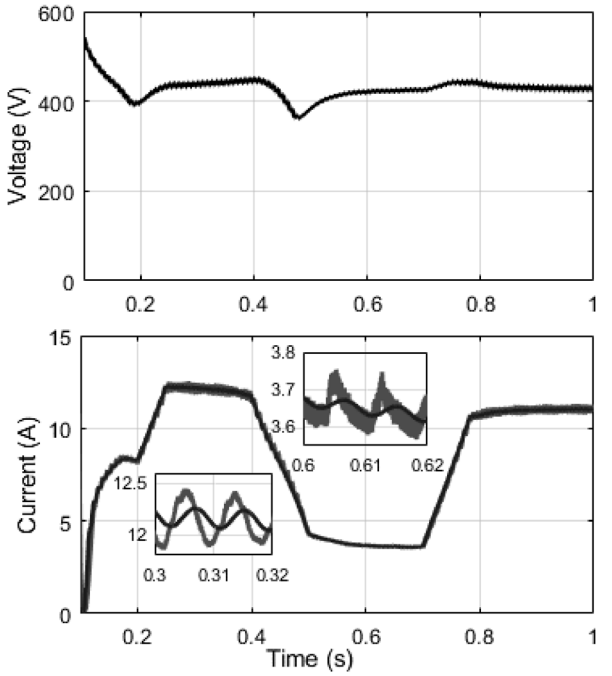

Fig. 7 *Simulation waveforms of the PV source simulator with PI controller: top figure: the output voltage waveform and bottom figure: comparison of the current reference and actual output current of the PV source simulator*

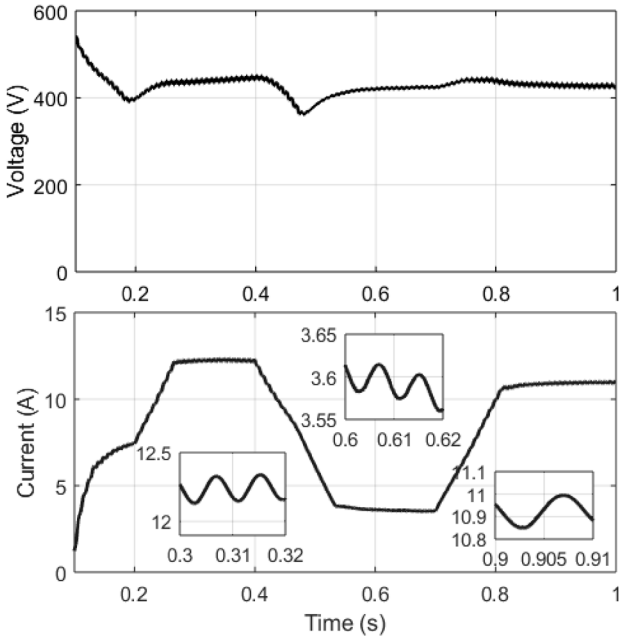

Fig. 8 *Simulation waveforms of the PV source simulator with the proposed SMDC: top figure: output voltage waveform and bottom figure: comparison of the current reference and actual output current of the PV source simulator*

current reference with the actual output current. It can be found that the actual current tracks the current reference; however, with notable steady-state error and phase delays. This phenomenon has been discussed in Section 2.

As a comparison, Fig. 8 shows the output voltage and currents waveforms of the PV source simulator using the proposed SMDC. Significant current tracking performance improvement can be observed from the bottom figure in Fig. 8. Both steady-state error and phase delay have been eliminated by the proposed SMDC, which validated the fast dynamics of the proposed PV simulator system. In addition, for both cases, the solar irradiance was intentionally reduced and then increased between 0.4 and 0.8 s. During transients, the SMDC also shows much better performance than the PI regulator.

Simulation studies are also carried out to verify the effectiveness of the proposed CBA. The ESR mismatch is intentionally added in the simulation model to make the phase currents unbalance. As shown in Fig. 9, the CBA is activated at 0.04 s. Without the proposed CBA, obvious unbalanced phase currents can be observed due to ESR mismatch. After activating the proposed algorithm, the three-phase currents quickly converged to the same value. The details of the phase currents are shown in zoomed windows in Fig. 8. In addition, the corresponding dc-link current, before and after activating CBA, is shown in the bottom figure of Fig. 9.

4.2 Experimental studies

In this work, experimental studies are also performed to validate the effectiveness of the proposed PV simulator using SMDC and CBA. The parameters of the major components in the circuit are the same as those listed in Table 1. Fig. 10 shows both dynamic and steady-state voltage tracking performances. As shown in Fig. 10*a*, when voltage reference has a step change, the output voltage can track its reference rapidly. Fig. 10*b* shows the steady-state results, where actual output voltage can well track the voltage reference with 120 Hz voltage ripple with slightly tracking error, which is caused by the low signal-to-noise ratio of the sampling since in the magnitude of the current ripple is much smaller than its dc value. Fig. 11 shows the waveforms of all three-phase currents, while Fig. 12 shows the PWM gate signal for three-phases and also the total output current on the top.

Experimental studies were also carried out to validate the effectiveness of the proposed CBA. In Fig. 13*a*, waveforms of the

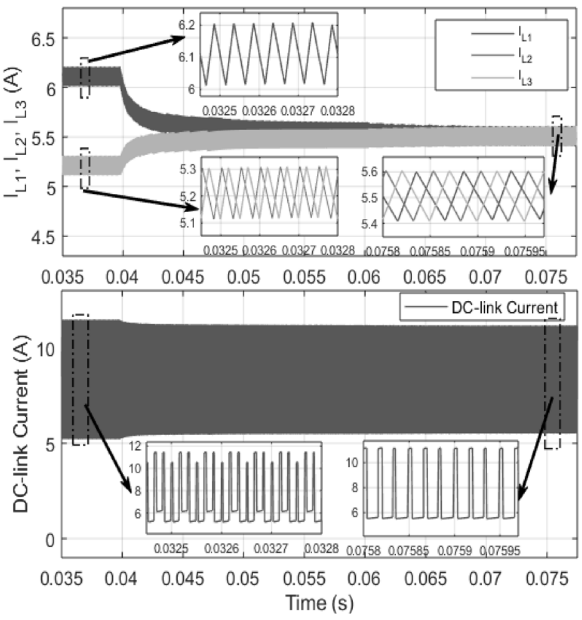

Fig. 9 *Simulation results of the current waveforms before and after activating the proposed CBA*

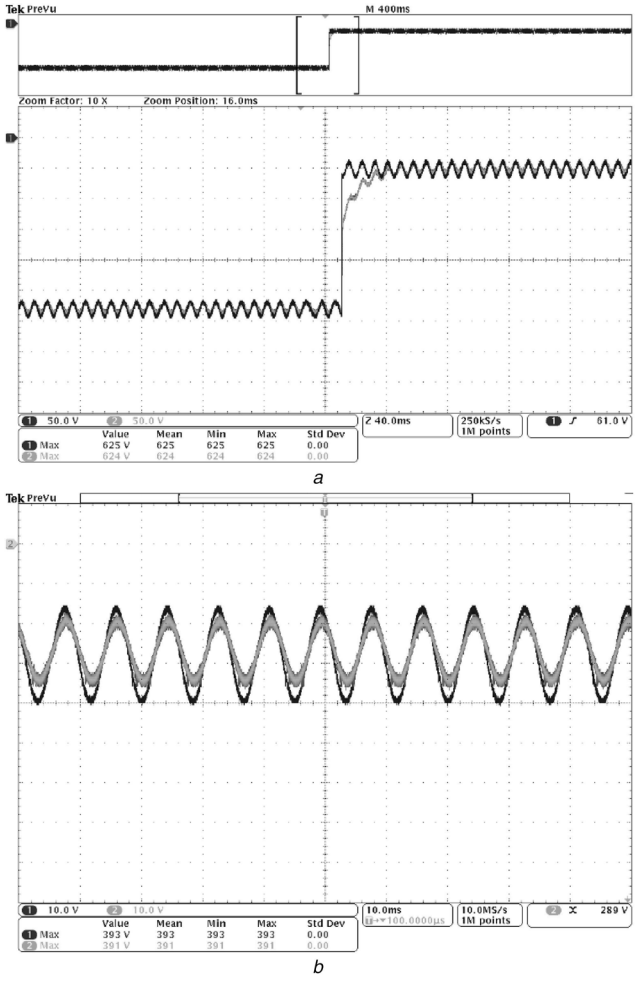

Fig. 10 *Experimental results*
(a) Output voltage waveform versus its reference, ***(b)*** Zoomed in voltage tracking performance at steady state

unbalanced three-phase currents are presented, where CBA was not activated. The corresponding dc-link current is shown in Fig. 13*c*. In the experiment, the ESR in phase 1 is smaller than the ESRs in the other two phases. Therefore, phase 1 current is higher than the other two phases. Once the proposed CBA is activated, all the

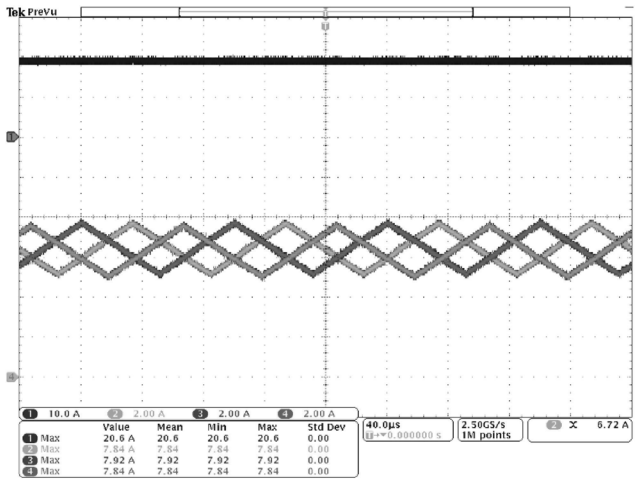

Fig. 11 *Waveforms of the phase currents*

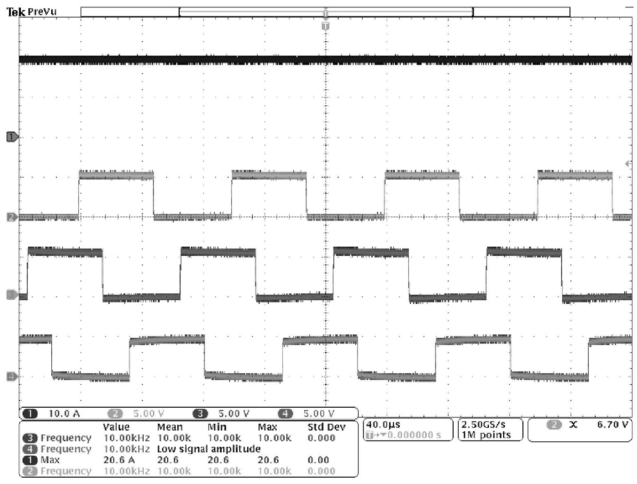

Fig. 12 *PWM gate signals applied to each phase with total output current on the top*

three-phase currents quickly converge to the same value, which is illustrated in Fig. 13*b* and the corresponding dc-link current is shown in Fig. 13*d*. To validate the effectiveness of the proposed CBA when load changes, an abrupt load increase was induced and the corresponding results are shown in Fig. 14, where balanced three-phase inductor currents were maintained both before and after load changing.

5 Conclusions

In this paper, a novel control approach, which integrates the SMDC with CBA, for an interleaved buck converter-based PV simulation is proposed, implemented and verified by using simulation and experimental studies. The proposed SMDC ensures the accurate voltage regulation performance even under abrupt load changes, while the CBA takes care of the unbalanced phase currents. In this work, only one dc-link current sensor is required to obtain the DM phase current using synchronised current sensing. Various tests were performed under steady state and transient conditions to validate the performance of the PV simulator. Both simulation and experimental results confirmed that the SMDC has better dynamic performance than the PI and the proposed CBA can effectively ensure balanced phase currents.

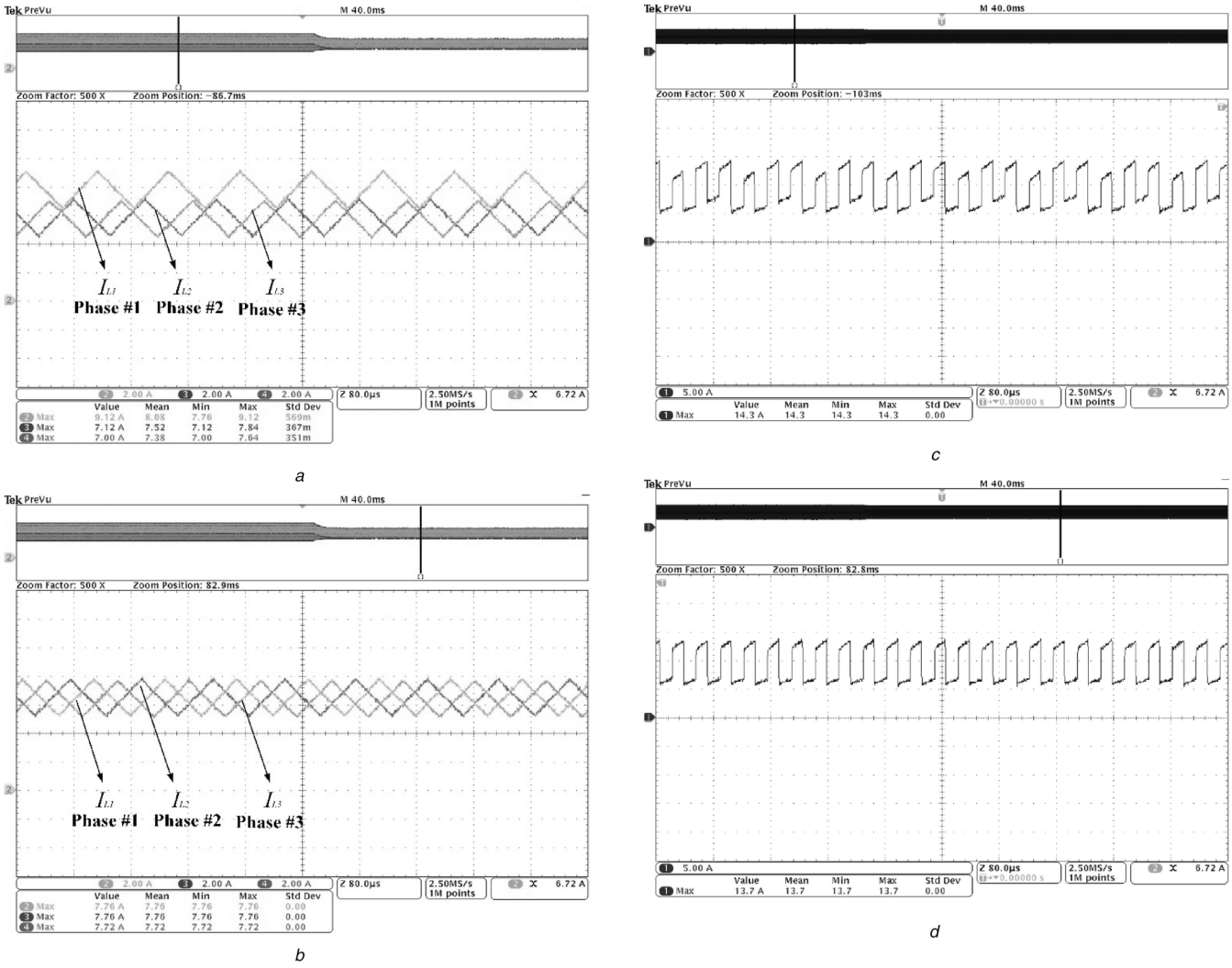

Fig. 13 *Experimental results*

(a), (c) Unbalanced phase currents and the corresponding dc-link current, ***(b), (d)*** Balanced phase currents and the corresponding dc-link current

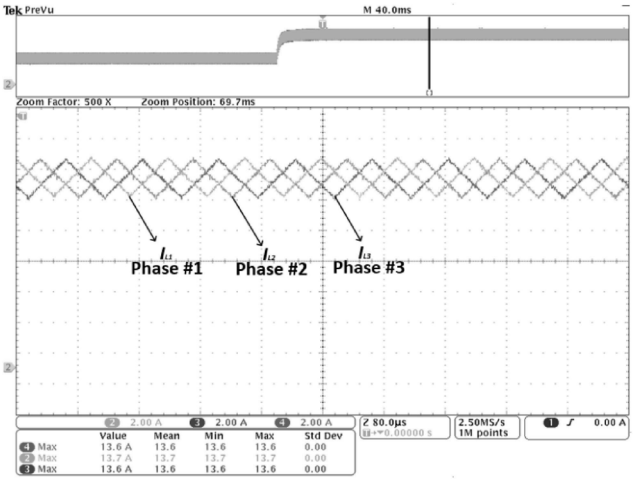

Fig. 14 *Phase current waveforms when the load has an abrupt change*

6 References

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