Experimental Study of Memristors for use in Neuromorphic Computing

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Abstract—**Memristor devices have the potential to drive a new class of specialized low power embedded hardware. The unique characteristics of these non-volatile and nanoscale devices allow them to perform parallel analog computing with extreme efficiency. To help facilitate the design of such systems, this paper describes the fabrication and characterization process used to develop memristors that are strong candidates for use in neuromorphic systems. In this work two different types of memristor devices, those with a GeTe switching layer, and those with a VO2 switching layer, are characterized and analyzed. These results are used to determine device suitability for use in neuromorphic computing applications through the properties of symmetry, reliability, stability, and programmability. In short, repeatable multi-level resistive switching has been investigated and the results have been summarized.**

Keywords—memristor, neuromorphic, hysteresis, multi-level resistive switching

I. Introduction

The memristor [1] is a non-volatile two-terminal passive circuit element with a wide programmable resistance range. Memristors can be laid out in a high density grid known as a crossbar [2], which gives them the potential to be fabricated with an areal density greater than that of synapses in brain tissue [1]. These crossbars can be used to produce high density, extreme low-power, neuromorphic hardware [3-5] capable of performing many parallel multiply-add operations in the analog domain. Existing papers [3-5] based on the simulation of neuromorphic memristor crossbars show promising results with these large high density structures. Furthermore, Neuromorphic systems based on memristor crossbars have potential to perform at a power efficiency of 6 to 8 orders of magnitude greater than that of traditional RISC processors [4]. However, before these systems can be developed, physical memristor crossbars must first be investigated.

As opposed to non-volatile memory systems [6,7], the ideal memristor in neuromorphic systems should have multiple resistance levels that allow for a programmable resistance range [3,8-16]. Work in [17-25] shows many different applications for memristors in neuromorphic computing where crossbars are used to carry out high speed, low power computation. In this work, two different types of memristors are studied in terms of efficacy and reliability. These include memristors based on germanium telluride (GeTe), as well as memristors based on vanadium oxide (VO2). Since the physical realization of the memristor at HP Labs [1], several institutions [2,14,16,26,27] have presented memristive switching in a wide array of materials. However, resistive switching thinfilms that contain GeTe and VO2 have not garnered the attention of more commonly used materials such as TiO2 [16] and TaO2 [28]. Therefore, this paper aims to analyze memristor devices based on these materials to determine the quality of their resistive switching properties. Furthermore, we aim to determine whether these materials are suitable for developing memristors that are capable of supporting neuromorphic circuit functionality.

This paper is organized as follows: Section II describes memristor structures and deposition methods. Device characterization results are presented in Section III, and Section IV provides a brief results discussion in terms of device suitability for neuromorphic systems. The conclusion is provided in Section V.

II. Memristor Devices

The memristor devices presented in this work were deposited as a Metal-Insulator-Metal (MIM) stack on Si wafers. In each chase, the substrate is silicon (Si) topped with 2 μm of Plasma Enhanced Chemical Vapor Deposited (PECVD) silicon dioxide (SiO2) [29]. Both devices were patterned with the same mask set using photolithography. Fig. 1 shows microscopic images displaying an array of isolated memristor devices, as well as a single 4 × 4 memristor crossbar. The numbers in Fig. 1 (a) correspond to the device overlap area in μm^2 for each individual memristor. Likewise, the digit '5' in Fig. 1 (b) represents an overlap area of 5 μm^2 for each memristor device in the crossbar.
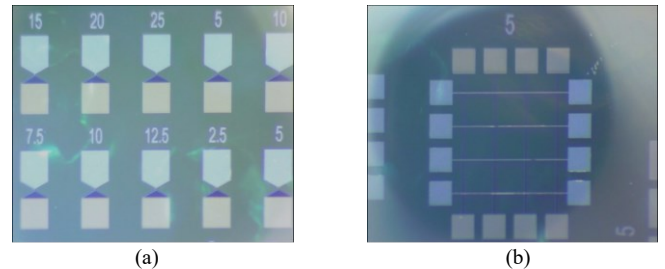

Fig. 1. Microscopic images displaying (a) an array of isolated memristor devices, and (b) a 4 × 4 memristor crossbar array.

A. The Germanium Telluride Memristor

The thinfilm layers that make up the germanium telluride memristor studied in this work can be viewed in Fig. 2 (a). The

top and bottom electrodes for this device consist of Pt, with the addition of Ti films for adhesion. Electrodes were deposited using the E-beam evaporation, and a pulsed laser deposition (PLD) process was utilized for the deposition of a 40 nm thick germanium telluride (GeTe) switching layer for all memristor devices on this wafer.

B. The Vanadium Oxide Memristor

The layer structure for the vanadium oxide memristor is displayed in Fig. 2. (b). In this case the electrode structure comprises of Pt and Au, with Ti for adhesion and Au isolation. A 50 nm vanadium oxide (VO_2) switching layer was deposited using the same PLD process as that used to deposit GeTe.
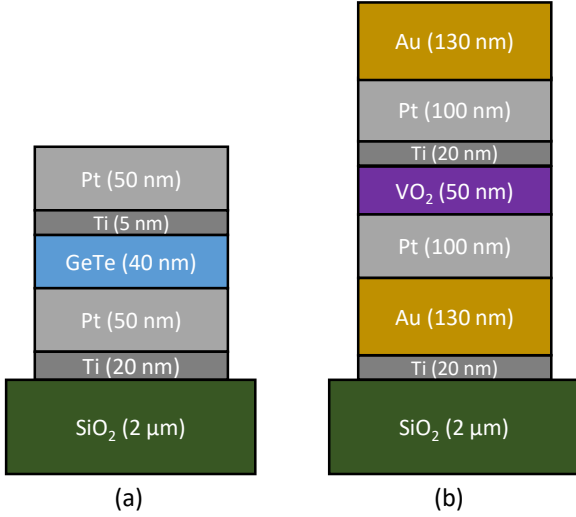

Fig. 2. Cross-sectional diagrams of the two memristors studied in this work including (a) the device based on GeTe, and (b) the device based on VO_2.

III. DEVICE CHARACTERIZATION

Electrical characterization for each memristor wafer was performed with an electrical measurement system consisting of a semiconductor characterization system (Keithley 2400-SCS) and a probing station. A MATLAB script was developed to control the Keithley system to ensure maximum versatility. Using this setup, we are able to apply any arbitrary voltage sequence to the a probed memristor wafer, with a minimum sample pulse width of one Power Line Cycle (PLC), which is about 17 ms. Highly non-linear switching kinetics are observed in the electrical characterization of each memristor device [30].

A. The Germanium Telluride Memristor

The I-V characteristic obtained from a 7.5 um² GeTe memristor device is depicted in Fig. 3. A repetitive cyclical voltage sweep was applied to the top electrode, and the bottom electrode was set to ground. At approximately 0.7 V the device current increases which bring the memristor device to its low resistance state (LRS). This mechanism is called SET. If no further external bias acts upon the memristor, it should theoretically retain the low resistive state until significant charge is once again applied. To turn the memristor off, a bias of opposite polarity is applied. In this case the memristor device was RESET at approximately 0.75 V. This switching pattern produces the familiar bowtie-shaped pinched hysteresis loop that is characteristic of memristors. To ensure the device safety,

a compliance current of 3 mA is fixed within the test setup. The cyclic voltage sweep was repeated eight times to test device stability with successive stimuli. This GeTe memristor shows strong repeatability with only minor degradation in hysteresis during the 8th cycle.
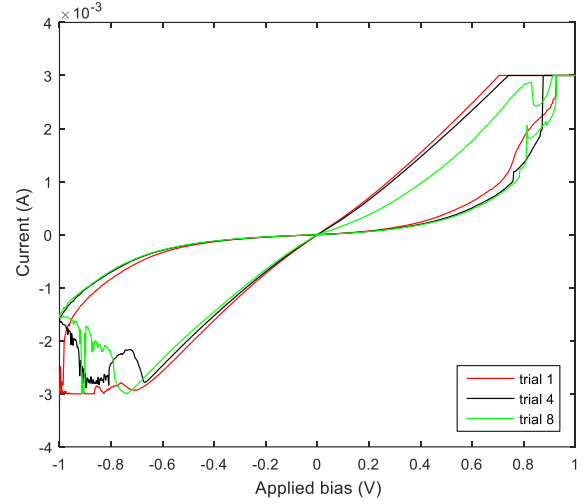

Fig. 3. Plot displaying the I-V characteristic of a 7.5 μm² GeTe memristor showing resistive switching over multiple cyclic voltage sweeps.

Furthermore, the electrical characterization in Fig. 4 shows hysteresis in both the positive and negative regimes for ten consecutive voltage sweeps. In this case, even with identical cyclic inputs, identically overlapped hysteresis is not achieved. Rather, some deviation is seen between cycles. This is assumed to be due to the existence of quasi fermi levels within the device electrodes, which would alter the population of electrons available between cycles. Furthermore, a continuously high field stress may alter tunnel current probability between cycles based on the changing state of the chalcogenide thinfilm.
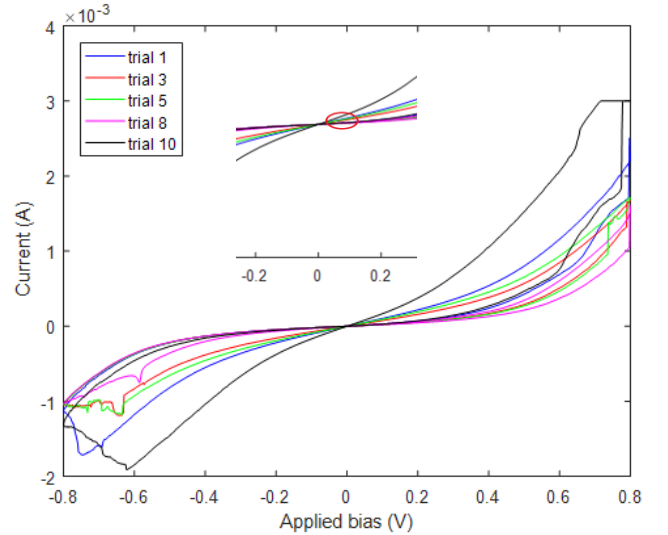

Fig. 4. Characterization of a 10 μm² GeTe memristor displaying the slight variations observed in ten repetitive cyclic voltage sweeps.

In Fig. 4, the SET voltage is found to be approximately 0.75 V. Assuming read voltage is less than 0.15 V, it can be concluded from this characterization that it is possible to retain

multiple resistance states due to the tunneling of charge carriers from the electrode quasi fermi levels towards the traps within the switching layer. With every individual trial, different resistive states are obtained after the SET voltage is applied. The inset in Fig. 4 shows a closer view of the existence of multiple states within the READ voltage range.

The result in Fig. 5 displays a characterization of a GeTe memristor where multiple RESET sweeps are applied after a single SET sweep. Each consecutive RESET sweep pushes the current level to a lower position.
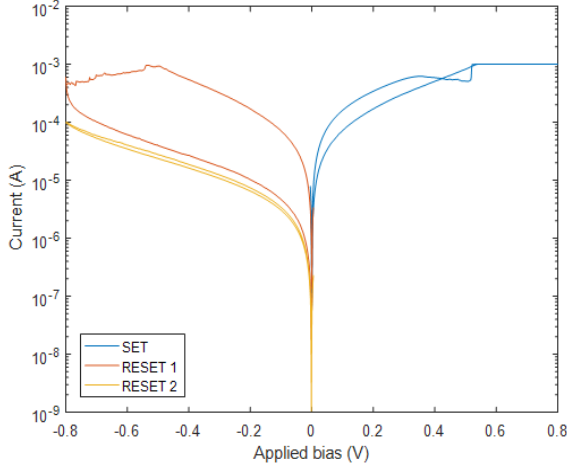

Fig. 5. Semi-log plot displaying an I-V characeristic where multiple negative voltage sweeps are applied after a single SET sweep on a $10 \mu m^2$ GeTe memristor.

The current levels corresponding to the positive SET sweeps are shown with the blue line in the right half plane of Fig. 5. Application of two RESET sweeps with a minimum voltage of -0.8 V produces two distinct hysteresis loops, which signifies an intermediate resistive state during the RESET process.

To further investigate the presence of intermediate resistance states, electrical characterization was performed by varying the current compliance level between cyclic sweeps. A cyclic sweep with a magnitude of 2 V both along the positive and negative direction was applied three times, each with a different current compliance. A zero-crossing pinched hysteresis is observed when current compliance is set to either 40 µA, 400 µA, or 4 mA. These results are displayed in Fig. 6.

Fig. 7 displays current compliance dependent multi-level switching from a 5 µm² device from the same GeTe wafer. This is a similar experiment to the one shown in Fig. 6, although the compliance current is varied from 30 µA to 3 mA to facilitate a smaller device area. This experiment also produces individual resistive states, although the current loops produced at the 300 µA and 3 mA compliance levels are much closer together when compared to the result in Fig. 6. This is because the compliance current was not reached in these cases, so compliance had less impact on device current.

The characterization results obtained from these GeTe memristors can be explained by the elastic trap assisted tunneling phenomenon. Distinct trap energy levels within GeTe dominate the charge transport mechanism. Multiple stable

resistance states can be observed which produce a hysteresis at different compliance currents. Experimentally, it was found that these GeTe based memristor devices are capable of retaining multiple states based on different current compliances. It may be possible to construct a neuromorphic circuit based on memristors that are capable of a slower transition from a high resistance state (HRS) to a low resistance state (LRS) by emulating this compliance with a series transistor in a 1T1M crossbar design [31].
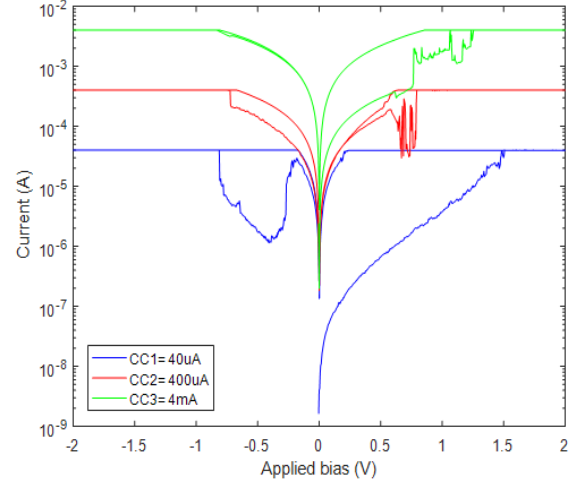

Fig. 6. Compliance current dependent multi-level resistive switching for a GeTe memristor with device area of 12.5 µm².
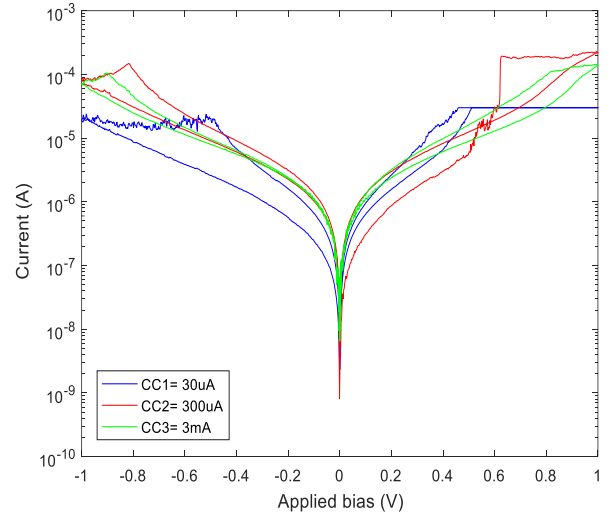

Fig. 7. A characterization result where compliance current is used to induce intermediate resistance states with a more subtle change based on a reduced voltage sweep magnitude in a 5µm² GeTe memristor.

B. The Vanadium Oxide Memristor

The I-V characteristic obtained from the vanadium oxide (VO$_2$) memristor device is shown in Fig. 8. In this case the compliance current was fixed at 3 mA. Based on this data, the SET voltage is approximately 1 V, and the RESET voltage is in the range of -1 V. When looking at Fig. 8, several non-linear jumps can be observed near the switching points. In future work, we aim to take advantage of these semi-stable current changes to induce multistage programmability.
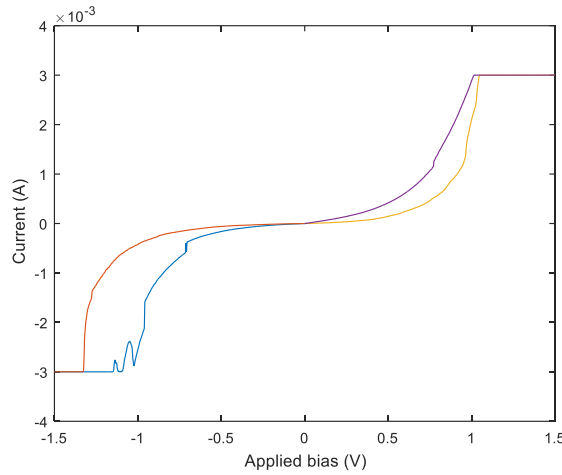
Fig. 8. Memristor I-V characteristic of $10\mu m^2$ VO$_2$ device.

IV. DISCUSSION

When studying the results obtained in this work, one notices a high degree of variability in these devices. However, that is not necessarily harmful to the desired neuromorphic computing applications [17-25]. This is because the goal in these neuromorphic systems is to program memristor devices along a continuous conductivity range, as opposed to inducing uniform binary switching. Many neuromorphic programming approaches contain a feedback mechanism to ensure the correct value is written within a memristor [12,15,22,23], even if that value is not obtained in a single cycle. Furthermore, work in [32] shows that stochastic devices are a necessity in some electronic computation systems, as they alleviate the need for expensive random number generators. Thus, we desire a device that is flexibly programmable over one that is perfectly uniform.

V. CONCLUSION

This paper presents two memristor devices, one based on GeTe and one based on VO$_2$. Based on the corresponding I-V characterizations, hysteresis and intermediate resistance states can be observed. The experiments in this work determined that there is a programmable resistance range within these devices.

In the future we plan to develop methods for creating devices with a smaller cross-sectional area using higher resolution fabrication methods. We also plan to perform electrical characterizations that test thermal stability. Finally, we plan on testing memristor crossbars to determine if structures based on the devices examined are capable of learning.

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