Real Time Simulation of Transient Overvoltage and Common-Mode during Line-to-Ground Fault in DC Ungrounded Systems

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***Abstract*—Real Time (RT) simulation of Power Electronics (PE) allows engineers to interface real-time controls for controller hardware-in-the-loop CHiL. CHiL verification moves a design from Technology Readiness Level (TRL) 3 to TRL 4. For RT CHiL simulation of DC protection systems, the RT simulation platform must be able to simulate common mode behavior, various grounding schemes, and fault transients at sufficiently high resolution so as not to interfere with the protection system design. This paper demonstrates this capability using a Latency Based Linear Multistep Compound (LB-LMC) simulation method implemented in Field Programmable Gate Arrays (FPGAs), in order to achieve 50ns resolution of common mode behaviors, including Line-to-Ground (LG) overvoltages resulting from LG faults and fault recovery in ungrounded DC systems. This resolution in RT cannot be achieved with today's commercial off-the-shelf (COTS) RT CHiL platforms. Furthermore, this capability can be expanded to other grounding schemes and larger PE networks, enabling RT CHiL validation of protection schemes for networks of power electronic converters at TRL 4.**

***Index Terms*—Hardware-in-the loop simulation, Power system simulation, Fault protection, microgrids, Power distribution faults**

I. Introduction

Power produced by renewable sources vary with time, requiring a power electronic interface for power conditioning. In order to achieve 100% renewable energy generation, and electrification of transportation such as ships and more electric aircraft (MEA), the majority of power and energy will flow through power electronic converters. This means next generation of power distribution systems will be a *network of power electronic converters* (PECs).

Protective system design is challenging for PEC-based systems, given by the lack of standards and experience-based design practices. Microgrids, electrified ships, and MEA have short cable lengths, DC distribution, and, generally, meshed power and energy delivery. In such systems, fault behavior at its extreme, i.e. sudden inception, is characterized by cable inductance and the filter capacitance of the connected PECs [1]. There will also be a race condition between the time for protective circuits to respond to isolate a fault and the actuation of internal unit-protection of the PECs. The factors result in the demand for extremely fast time response protective equipment and protection scheme trip settings to achieve fault discrimination. This capability is enabled by solid state circuit breakers and fast acting isolating switches within the protective equipment. Radially distributed architectures require extremely fast coordination to achieve overcurrent relay capability [2] and meshed distribution architectures will additionally require high speed communications for protective relaying.

RT simulation provides an opportunity to help move up TRL [3] when paired with RT controls, or CHiL [4], [5]. CHiL allows engineers to test their controls schemes in real time on real hardware, i.e. moving from TRL 3 with offline simulation to TRL 4 with RT simulation. Prior to CHiL, engineers would have to go from offline simulation to hardware without an intermediate step. Additionally, most COTS RT simulation systems are meant for testing controls of power electronics to validate differential mode (DM) behavior, but not necessarily common mode (CM) nor fault transient behavior. One down side of having all of the power processes through power electronics is the production of fault-induced and resonant CM voltages which can lead to circulating CM current between non-isolated paralleled converters and through unintended PEC fault paths during multiple LG fault scenarios [6].

To achieve PEC-based distribution system simulations in RT, suitable for testing of protective approaches, the RT simulation must be able to simulate 1.) Accurate grounding of TT, TN, IT, or ungrounded networks to enable correct LG fault characterization; 2.) Mixed mode DM/CM behavior resulting from PEC network asymmetry and the impacts controls delays and Pulse-Width Modulation (PWM); 3.) Ability to perform high speed FPGA-to-FPGA communication sufficient for high speed protective relaying; 4.) Sufficient simulated

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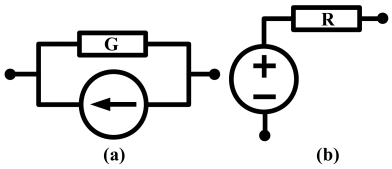

Fig. 1: LB-LMC Component Models; (a) component with current state, (b) component with voltage state

fault transient resolution to test out the capability of the protective control hardware; 5.) Ability to simulate infinitely large networks through plug and play parallel-ability of the RT simulator components; 6.) Ability to add limitations such as compute and sensor bandwidth, and communication delays, in order to derive the performance requirements for protection schemes, controls, and sensors.

This paper demonstrates that CM and LG fault transients can be simulated in RT without resolution issues. Section II describes the simulation method used. Section III shows the FPGA-based implementation of LB-LMC, enabling RT simulation time-steps in the tens of nanoseconds. IV describes the simulation model, and shows common mode and fault transient behavior. Lastly, Section V draws conclusions.

II. Summary of LB-LMC Method

This section provides a brief summary of the LB-LMC simulation method used for this proposed approach. A full description and analysis of the LB-LMC method is given in [7] [8] which contains details of the method not presented here.

LB-LMC method is a non-iterative, transient simulation method for the fast real-time solving of non-linear multi-physics network systems such as power electronic and generation systems in discrete time steps. The method models systems by solving as linear set of equations $Gx = b$ where x is a vector of system solutions, b is a vector of source contributions solved from state equations of components in the system, and G is the system coefficient matrix. Regardless of linearity or switching behavior of components of the system, the LB-LMC method holds the matrix G constant for every time step. Source contributions of non-linear components in a given system are kept separate from linear parts of the system, injected into the linear equations $Gx = b$ through b, so that non-linear behavior of system is maintained. To keep G constant and to avoid use of iterative solving (i.e. Newton-Raphson) for non-linear component solving, explicit discretization of component state equations is applied. From these properties of LB-LMC method, the method can solve non-linear systems using linear approaches.

The LB-LMC method models components of a system, depicted in Fig. 1, as voltage (across) or current (through) source contributions, where the sources are updated from state equations of the component in question. Components with more than two terminals can be modeled with a collection of these sources. For linear components, the state equations are discretized using Trapezoidal rule which introduces a series resistance or parallel conductance to the sources that models the memoryless terms of the discretization. These resistances and conductances are imprinted into the G matrix of the system. Non-linear components are discretized using explicit methods such as Euler Forward or Explicit Runge-Kutta. They introduce no resistance/conductance to the system, being modeled as only ideal voltage or current sources.

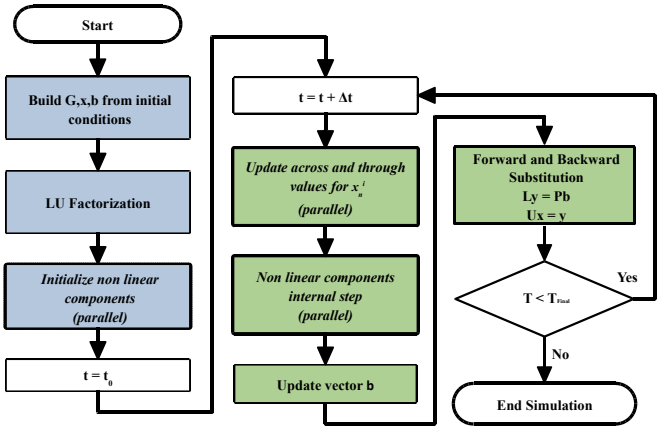

Fig. 2: LB-LMC Solution Flow

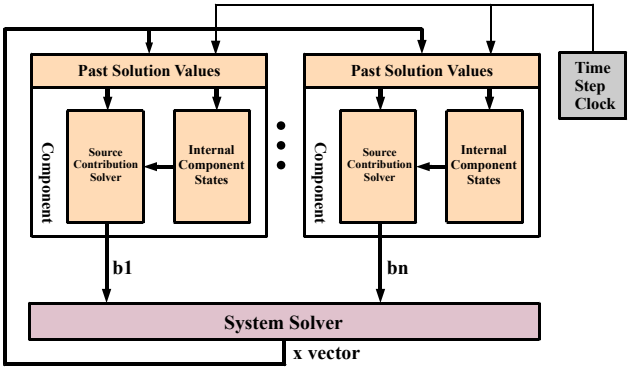

Fig. 3: LB-LMC Solver Engine

As shown in Fig. 2, the solution flow at every time step under LB-LMC method is depicted. Before online simulation, the system equations are defined from network of system and G is pre-inverted. Then, the initial conditions of components and system solutions are set before the simulation goes online. After initialization, the simulation goes online, starting each time step with the solving of component state equations in parallel. Once all component equations are solved, their source contributions are aggregated into b and the system solutions are solved using $x = G^{-1}b$. If simulation is to continue, a new time step execution is started, using solutions from past time step.

III. FPGA Implementation of LB-LMC Solver Engine

The brief description of the FPGA implementation of LB-LMC method solvers are presented in this section. Full description of the implementation not provided here are found in [7] [9].

Fig. 4: National Instruments Control for FlexRIO (NI-7935R)

The scheme for the FPGA design of the LB-LMC solver engine is depicted in Fig. 3. In this scheme, each component of the system to be solved for is encapsulated as a dataflow execution core. Each core takes as input relevant system solutions from previous time step and any data signals that control the behavior of the component (such as gate signals for a power converter component). From only these inputs and the past states of the component, the component computes its source contributions for present time step. To compute the system solutions x of the system for present time step, a system solver core is defined. This core takes as input the source contributions from the component cores and from these inputs computes vector b. With b and the pre-computed matrix G^{-1} inlined into logic of the core, the core solves $x = G^{-1}b$ for current time step. Both component and system solver cores use fixed-point arithmetic instead of floating-point to significantly reduce computation FPGA resource usage and latency for smaller time steps and larger system models in real-time execution. To achieve real-time execution, the execution of the LB-LMC solver engine is scheduled using a system clock provided by FPGA platform loaded with the engine design. The engine is scheduled to execute and solve for system solutions x in a single execution cycle, where the component and system solver cores are executed in a parallelized dataflow manner. On the rising edge of the system clock, the engine is triggered to execute for new time step. To set the time step of the engine to real-time, the clock period is set to the time step of the engine. As seen in [7] [9], the LB-LMC FPGA solvers are capable of executing in real-time with ≤50 ns discrete time steps.

The solver was implemented on National Instruments Controller for FlexRIO, model number NI-7935R (Fig. 4). The FlexRIO has a Xilinx Kintex-7 410T FPGA, where the LB-LMC solver and controls were implemented. Due to limitations in data logging ability, the longer time data captures are at lower resolutions, and the shorter time captures are at higher resolutions. The code generation c++ library for the LB-LMC solver can be found at https://github.com/MatthewMilton/LBLMC-Solver.

IV. Common Mode and +LG fault in an Ungrounded DC system

Fig. 5 shows a AC to DC VSR with LCL differential mode filter and LC common mode filter powering a resistive load, and measurement points refered to throughout the paper. The VSR regulates to the DC bus voltage to 12 kV. For simplify, a 2-level converter was used, but in practical application, a high number of levels would be used to reach a 12 kV Bus.

The source is modeled as an ideal 3-phase voltage source of 6 kV_{LLRMS} with a feeder cable. The feeder cable represents resistance and inductance from cabling and a synchronous generator's stator windings. The controls used are decouple voltage oriented controls in rotating dq frame [10], but with 3^{rd} harmonic injection and per-unitized input signals. Line to ground AC and DC voltage measurements are used in the simulation, but for the controls, their respective DM part are extracted. Table I shows the equations used to extract DM and CM from MM for 2 and 3 phases for voltages and currents.

IT grounding is modelled with a capacitor (C_{og}) and resistor (R_{og}) in parallel to ground, with values of 0.1μF and 10kΩ, respectively. This represent the parasitic capacitance in an ungrounded system [11], [12]. The parallel resistor R_{og} is present to ensure the bus voltages returns to initial conditions. Change this Resistance affects how long the bus voltage to recover after a fault is removed, governed by the RC time constant of R_{og} and C_{og}. To get exact value of the parasitics to ground, one would have to use a Network Vector Analyser (NVA) to extract S-parameters or make a FEA model, for example with COMSOL Multiphysics [13]. However, this changes with the geometry of the system. So unless the exact system is know before hand, the protection scheme will have to be modified once it is deployed. The contribution of this paper is to show qualitatively, that this high frequency ringing during Line-to-Ground faults can be modeled in Real-Time Simulation. A list of circuit parameters can be found under Table II.

The 2 level, 3 phase VSR produces CM voltage due to its switching states [14]. The CM voltage levels are $\pm V_{dc}/2$, and $\pm V_{dc}/6$. With a 12 kV bus, the CM voltage outputs are ± 6 kV and ± 2 kV, as seen in Fig. 7. This leads to CM currents as seen at measurement point $iabc_f$ in Fig. 8a. The CM current is reduce after passing through the CM LC filter, Fig. 8b. This shows the LB-LMC solver is able to simulate CM currents and CM filters correctly.

During a LG fault in an unground system, the DM voltage remains constant while the CM shifts [15]. In normal operation, positive Vdc rail to ground, Vpg, is +6 kV, and negative Vdc rail to ground, Vng, is -6 kV, giving a differential mode voltage, Vdc_{DM} of 12 kV. Applying a +LG fault on the positive DC rail forces the positive rail to zero volts. The ungrounded system will keeps the 12 kV DM voltage, and shift the negative rail to -12 kV. When the fault is removed, the voltage will go back to nominal. This fault will cause all parts of distribution system that are not transformer isolated to shift voltages as well. This is why the AC side voltages, $Vabcg$, shifts as well, as seen in Fig. 9a. Fig. 9e shows the DC DM voltage remaining constant at about 12kV during the fault, and Fig. 9b shows the AC DM voltages remain constant as well. The voltage shift during the fault can be seen in their common mode counter parts for DC and AC in Fig. 9f and

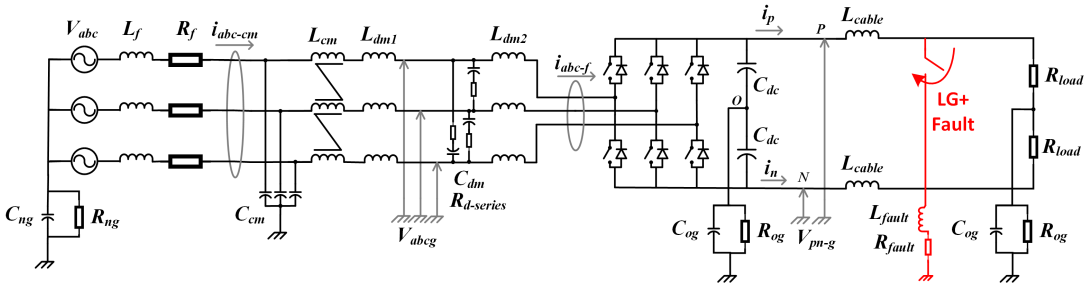

Fig. 5: Voltage Source Rectifier Circuit

TABLE I: Equations for extracting DM and CM from MM signals

Description	Signals	MM	DM	CM
3-phase Voltage	Vag, Vbg, Vcg	$Vabcg_{MM}$	$Vabc_{DM} = Vabcg_{MM} - Vabcg_{CM}$	$Vabcg_{CM} = (Vag + Vbg + Vcg)/3$
3-phase Current	ia, ib, ic	$iabc_{MM}$	$iabc_{DM} = iabc_{MM} - iabc_{CM}/3$	$iabc_{cm} = ia + ib + ic$
2-phase Voltage	Vpg, Vng	Vdc_{MM}	$Vdc_{DM} = Vpg - Vng$	$Vdc_{CM} = (Vpg + Vng)/2$
2-phase Current	ip, in	idc_{MM}	$idc_{DM} = (ip - in)/2$	$idc_{CM} = ip + in$

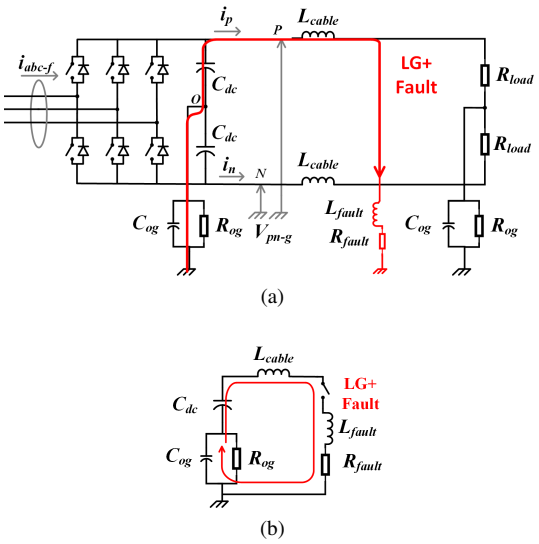

Fig. 6: DC+ Line to Ground Fault (a) current path and (b) equivalent circuit during fault.

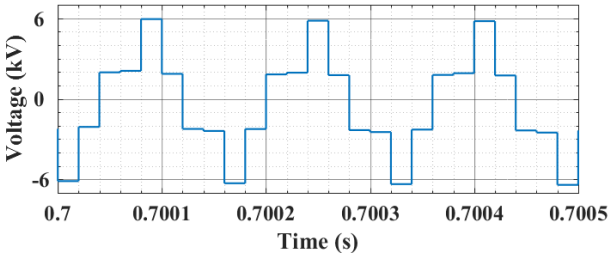

Fig. 7: CM Voltage at $Vabcg$. Data is captured at 50 kHz.

Fig. 9c, respectively.

Fig. 6a shows the path of current during a LG fault, and

TABLE II: VSR Parameters

Parameter	Symbol	Value
Vdc rated	V_b	12 kV
AC Source, V_{LL} RMS	V_{abc}	6 kV
AC Source, Frequency	f_e	60 Hz
Switching Frequency	f_{sw}	6.25 kHz
Feeder Cable, Resistance	R_f	0.198 Ω
Feeder Cable, Inductance	L_f	1.8 mH
CM Filter, Inductors	L_{cm}	60 mH
CM Filter, Capacitors	C_{cm}	0.1 μF
DM Filter, Inductor 1	L_{dm1}	0.955 mH
DM Filter, Inductor 2	L_{dm2}	5.6 mH
DM Filter, Capacitor	C_{dm}	16.652 μF
DM Filter, Damping Resistor	$R_{d-series}$	55.1822 Ω
DC Link Capacitance	C_{dc}	20 mF
Cable Inductance	L_{cable}	10 μF
Resistive Load	R_{load}	100 Ω
Floating Ground, Capacitance	C_{og}	0.1 μF
Floating Ground, Resistance	R_{og}	10 kΩ
Fault Inductance	L_{fault}	10 μH
Fault Resistance	R_{fault}	1 mΩ

Fig. 6b shows the equivalent circuit during the fault. The equivalent circuit forms an under damped LC circuit with resistant frequency of

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \quad (1)$$

For this circuit, L would be the sum of the cabling and fault inductance, 20 μH, and C would be the parasitic capacitance to ground, 0.1 μF. The parasitic capacitance and DC link capacitance are in series, but since the DC link cap is many orders of magnitude larger than the parasitic capacitance, it

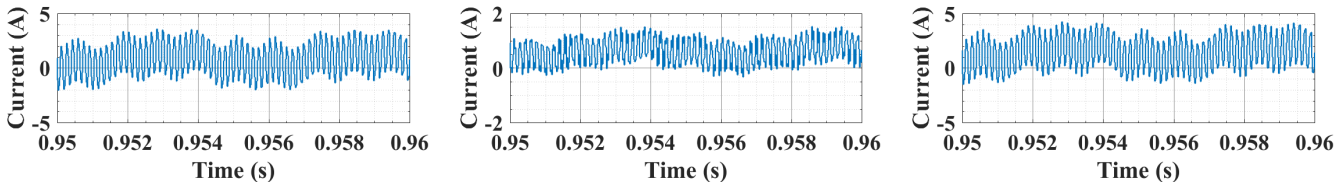

Fig. 8: VSR CM current at (a) $iabc_f$ (b) $iabc$ (c) idc. Data is captured at 50 kHz.

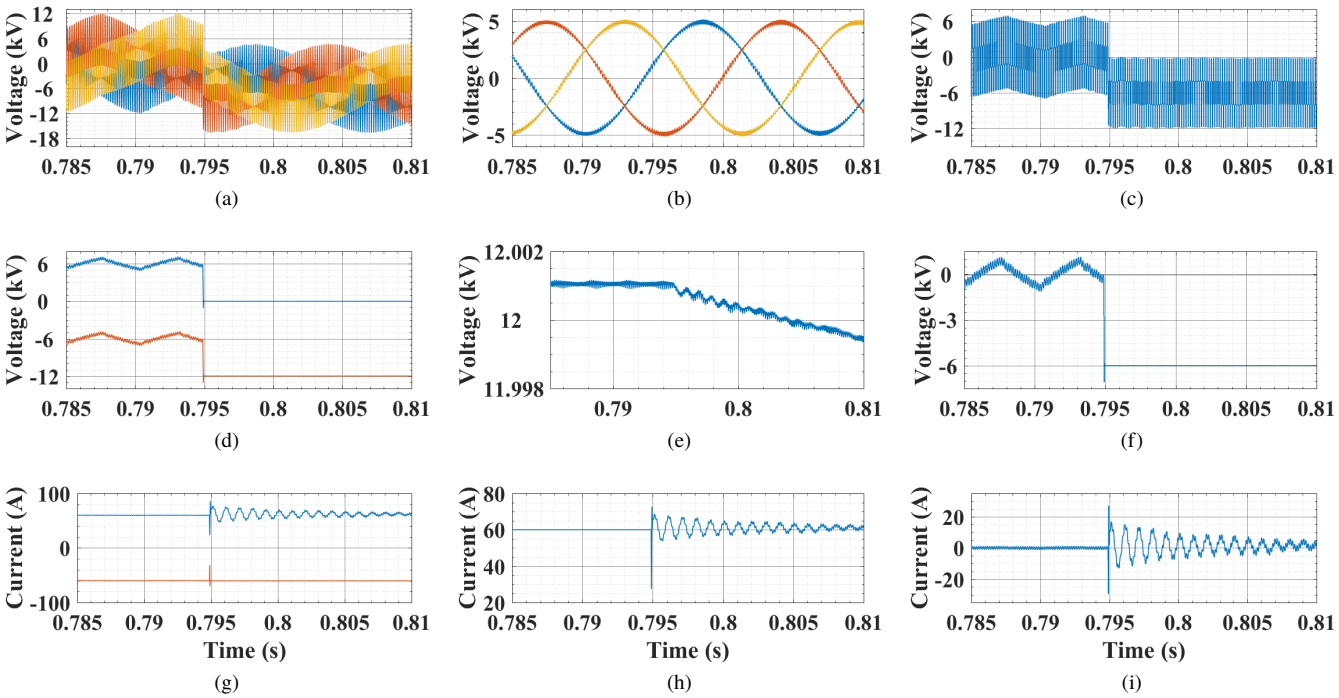

Fig. 9: +LG fault at 0.795 seconds. Data is captured at 50 kHz. Left, Middle and Right Columns are MM, CM, and DM, respectively. Vabcg (a) MM (b) DM (c) CM; Vpng (d) MM (e) DM (f) CM; ipn (g) MM (h) DM (j) CM.

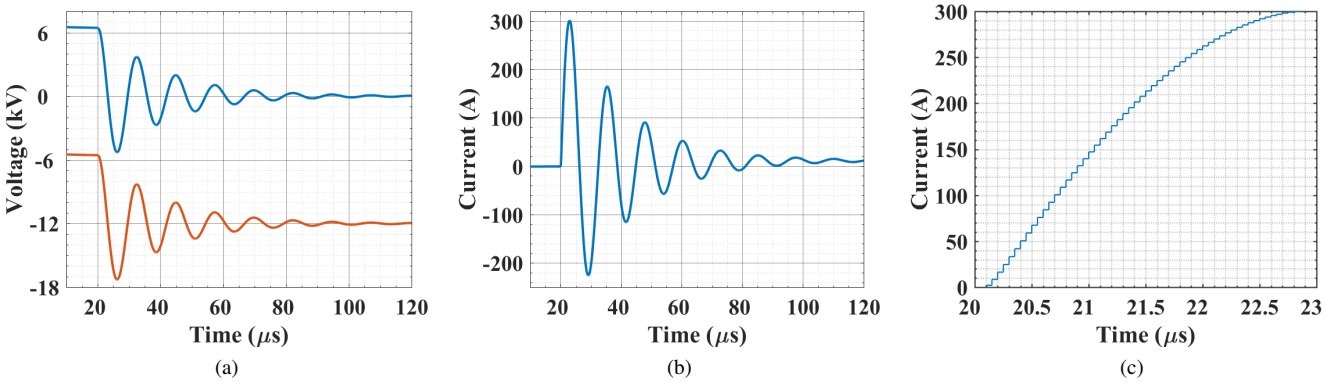

Fig. 10: +LG fault applied at 20 μs. Data is captured at 20 MHz. (a) Vpng (b) idc CM (c) idc CM zoomed.

can be ignored. This gives a resonant frequency of 125.4 kHz or period of 8.89μs.

This underdamped response causes a transient voltage to the DC bus, and as in Vpg and Vng in Fig. 10a. Vpg's overshoot

peaks at about -5kV and *Vng*'s overshoot peaks at about -17 kV. This large swing in voltage could exceed the isolation rating of the power electronics module and/or stress cable insulation; however, since this transient only lasts tens of μs, the energy content maybe very low, so its exact impact may not be significant. This is an area for future research. Similar voltage transients can be expected if a LG fault was applied to the negative DC rail, just in the opposite voltage direction. The transient peaks in Fig. 9a and Fig. 9i are missed due to the lower sampling resolution of the larger time capture.

The CM DC current transient can be seen in Fig. 10b. This transient is also a function of C and L. So if the cable length increases, the transient will increase in period and decrease in amplitude. The significance of this CM DC current waveform is that in a real implementation of power converters in floating system, LG voltage measurement may not be viable, leaving only the CM DC current transient for ground fault detection and location. For example, one could use high bandwidth Rogowski coil spread through the network, paired with Wavelet analysis do help detection and locate ground faults [16] [17], or other methods that require high resolution simulation [18].

COTS RT FPGA-based simulators have time-steps that range from about 0.5 μs to 4 μs, depending on the size of the circuit. From experience, this VSR runs at about 1μs. This means for this particular example, the transient waveform with a period of 8.89 μs will have, slightly less than 9 data points per period. This is poor resolution for a simulation that is trying to *characterize* fault transient in order to design protection schemes are it. With LB-LMC's 50 ns timestep, this example can simulate the transient waveform with 177 data points. The resolution of the solver can be seen in Fig. 10c. This significantly increases the resolution of the transient, allowing for accurate fault characterization of high frequency transient in system with short cable lengths.

V. Conclusion

In this paper, common mode voltage and current were simulated in RT for a 12 kV VSR in an ungrounded system. Though ungrounded systems were looked at, any grounding scheme can be used. A +LG fault on the bus was applied, and it was shown overvoltage and CM DC current transient were able to simulated in RT with high resolution of 50 ns, a level currently non present in the COTS RT simulators. This high resolution was achieved using LB-LMC FPGA based RT simulation. Due to the scalibility of LB-LMC, larger power electronic networks can be made at this resolution. This will enable ground fault protection design for DC ungrounded system, without bandwidth limitations. This makes sure the protection scheme design is not drive by the resolution of the RT simulator. Since the solver is FPGA based, SFP protocol can be used to test FPGA to FPGA high speed protective relaying schemes. Moreover, since the LB-LMC simulation engine is an entity on the FPGA, any logic can be added on the same FPGA, allowing to test the logic without sensor bandwidth limitations or communication delays.

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