Impact of Communication Latency on the Bus Voltage of Centrally Controlled DC Microgrids During Islanding

Mahmoud Saleh, Yusef Esa, *Student Member, IEEE*, and Ahmed Mohamed, *Senior Member, IEEE*

***Abstract*—Maintaining a sustainable and reliable source of energy to supply critical loads within a renewable energy-based microgrid (MG) during blackouts is directly related to its bus voltage variations. For example, voltage variation might trigger protection devices and disconnect DERs within the MG. Centrally controlled MGs (CCMGs) type is dependent on communication. Therefore, it is very important to analyze the impact of communication networks performance degradation, such as latency, on the bus voltage of CCMGs. This paper investigates the effect of wireless communication technologies latency on the bus voltage and performance of DC CCMGs and how to mitigate it. Two mathematical models were developed to describe and predict the behavior of MGs during latency. As a case study, a renewable energy-based DC MG with its centralized control scheme was simulated to validate and compare the developed mathematical models. Results verify the accuracy of the developed models and show that the impact may be severe depending on the design, and the operational condition of the MG before latency occurs.**

***Index Terms*—Communication-based control, communication latency, DC microgrid, sustainable microgrids.**

I. Introduction

THE transition from traditional power grids to smarter ones mandates increased dependence on information and communication technologies (ICT) [1], [2]. This dependence is continuously growing with the introduction and evolution of emerging technologies, such as advanced metering infrastructure (AMI), MGs, phasor measurement units and electric vehicles. A Smart Grid can be defined as a modernized electrical grid that utilizes communications and information technology to make automated decisions to improve the reliability, economics, efficiency and sustainability of the production and distribution of electricity. The definitive model of the Smart Grid has yet to be defined, however, the model will reflect the widely recognized key capabilities essential for successful implementation, such as [3]: enabling massive deployment and efficient use of distributed energy resources with integration capabilities to fully communication based control platforms; enhancing the efficiency, resiliency, sustainability and self-healing capabilities of an electric power grid; facilitating the interaction of consumers with energy management systems to support demand-response and load shaping (e.g., peak shaving) functionalities; allowing real-time, scalable monitoring of grid status and operations through the deployment of advanced metering and supervising systems; supporting the electrification of transportation systems (e.g., plug-in electric vehicles and electric rail systems) [4], [5].

From a practical point of view, the above vision of a smart grid requires pervasive communication and monitoring capabilities [6]. Therefore, it is crucial to analyze the impact of ICT networks performance degradation on the grid operation.

A microgrid is a group of interconnected loads and distributed energy resources within clearly defined boundaries. It acts as a single controllable entity with respect to the grid and can function in either grid-connected or islanded mode [7], [8]. In order to optimize the operation of an MG, i.e., maintain generation/demand balance, maximize energy harvesting from renewables, minimize dependence on the main grid, etc., an efficient control technique is required. DC MG control could be realized, among others, using one of two main methods: (1) Voltage based droop control; or (2) Centralized control [9].

Voltage droop control is akin to frequency droop in AC networks and is achieved by sharing the demand among parallel converters. It is based on using the voltage of the physical link between the converters, namely the DC bus, to signal deviations in the generation/demand ratio [10], [11]. For instance, a decrease in the DC bus voltage indicates generation deficiency; therefore, all converters start to increase their output power set points until the balance is achieved, i.e., the DC bus voltage is restored. This control technique has several pros, e.g., it allows power sharing while providing active damping to the system, it offers a plug and play feature since new converters can be seamlessly integrated to the DC bus, and above all, it does not require communication [11]. However, it has drawbacks as well, such as the deterioration of current sharing caused by load dependent voltage deviations, having circulating currents [12], and its failure to achieve optimal performance of the MG.

In centralized control, individual DERs and controllable loads, if any, are controlled via local control agents. The data

Manuscript received December 6, 2017; revised April 16, 2018 and July 3, 2018; accepted August 9, 2018. Date of publication October 4, 2018; date of current version September 18, 2019. This work was supported in part by the National Science Foundation awards number 1640715 and 1830105. Paper no. TSTE-01109-2017. *(Corresponding author: Ahmed Mohamed.)*

M. Saleh and Y. Esa are with the Smart Grid Laboratory, Department of Electrical Engineering, City University of New York, New York, NY 10031 USA (e-mail: mahmoudsalahem@gmail.com; yusefesa@gmail.com).

A. Mohamed is with the Smart Grid Laboratory, Department of Electrical Engineering, City University of New York, New York, NY 10031 USA, on leave from the Department of Electrical Engineering, Menia University, Menia 11432, Egypt (e-mail: amohamed@ccny.cuny.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TSTE.2018.2873699

from local DERs and load agents are aggregated in the MG central controller (MGCC), processed through a predefined control algorithm, then feedback commands are sent back to the local agents through wired or wireless communication. This allows the design of energy management algorithms that have the potential to achieve optimal, or at least near-optimal, MG performance. However, the main concern about communication-based control is the hypothesis that the reliability of the MG may be affected by the intrinsic drawbacks to ICT networks, e.g., delays and/or packet loss. Even though this hypothesis is decisive while designing MGs and MGCCs, proving it right or wrong, received minor attention in literature.

A few papers in the literature have studied the interdependence between the power grid and ICT network on a large scale [13]–[15], which modeled and analyzed the impact of communication nodes failure on a large-scale power system, and the initiation of a cascading failure. However, there is no technical analysis on the impact of ICT latency, from the power systems perspective, on the performance of smart grids or small-scale systems such as distributed energy resources (DERs) and/or DC MGs. Some papers focused on the AC MGs [16], [17]. The work in [18] introduced an improved droop control method by integrating it with a low bandwidth communication decentralized control scheme. A portion of the work briefly discussed the impact of communication delay on the control of the MG. In [19], researchers proposed a hierarchical control scheme for DC MGs cluster, where the primary control layer is droop control based and the secondary level is decentralized control based. A portion of that work briefly showed the impact of communication delay on their proposed control without analysis, concluding that with long delays the proposed control system fails. To the best of our knowledge, this paper is the first attempt to investigate/analyze the impact of communication latency on the performance of centralized control DC MGs from a power system perspective.

II. MG Communication Networks

In MGs, and in smart grids generally, the communication network functional requirements, e.g., data rate and coverage range, significantly vary depending on the control layer. Therefore, the communication networks of a smart grid are typically designed in a hierarchical multilayered architecture [20], as shown in Fig. 1. This architecture includes:

Home Area Network (HAN): It provides low bandwidth, two-way communications between home appliances and equipment (e.g., smart meters), or among MG resources and loads. Data being exchanged might be voltage, current and frequency measurements, which could be utilized in MGCC, demand response, home/building automation, etc. The communication techs that are usually deployed within these networks could be wired or wireless, such as Zigbee, Bluetooth, and WiFi [21].

Neighborhood Area Network (NAN): It acts as a gateway between HANs and the upper layer, transmitting information from the consumer premises to the utility data center for processing and feedback action [22], [23]. NANs involve LTE, WiMax, WiFi, etc. This layer is needed when aggregating

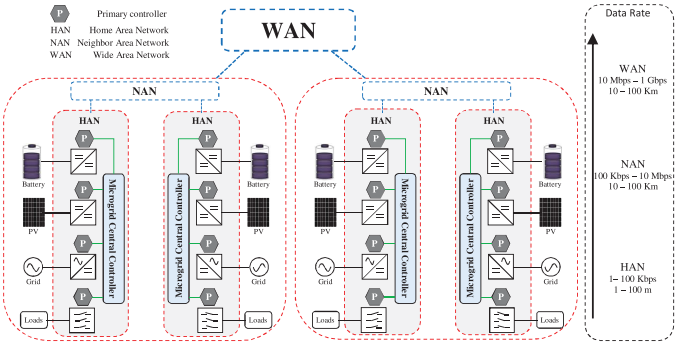


Fig. 1. Smart grid communication hierarchical multi-layer architecture.

TABLE I
Wireless Communication Technologies

Tech name	Zigbee	LTE M2M	HSPA M2M	WIFI
Average Delay (msec)	50 ~ 140 [24]	30 ~ 40 [25]	10 ~ 26 [25]	Up to 300 [26]
Coverage range	Short	Wide	Wide	Short
Advantages	Low cost, power & scalable	Reliable	Low latency	Ease of use

geographically dispersed DERs in a community MG or a virtual power plant.

Wide Area Network (WAN): Its main task is to transfer the overall aggregated data to grid operators, and command signals to the consumers; therefore, it has to be highly reliable, and be able to carry large data on a wide range [23].

Wireless technologies can be used for information exchange between controllers in an MG. They eliminate the need for physical connections. Moreover, they can be used as a redundant system even if a wired connection exists for increased reliability. For instance, data traffic could be routed to the wireless network, mitigating congestion on wired links, to increase data transfer speed. Table I shows a comparison of some common wireless communication technologies, including Zigbee, Long Term Evolution Machine to Machine (LTE M2M), High Speed Packet Access Machine 2 Machine (HSPA M2M) and WiFi [24]–[26]. Their delay impact on the DC MGs performance will be discussed in Section V.

III. Transient Analysis During Delay

In this section, analysis of the impact of communication latency on DC MGs during islanding was conducted. Moreover, a discussion of how the DC bus voltage varies when a communication delay takes place was presented. Deviations in the bus voltage are critical since they affect the stability of the MG, and are directly related to the relays settings within the MG. Two mathematical models were derived to examine the variation of the large signal (ignoring ripples) of the DC bus voltage $V_{\text{Bus}}(t)$ with various ranges of time delays, associated with the various communication techs described in Section II.

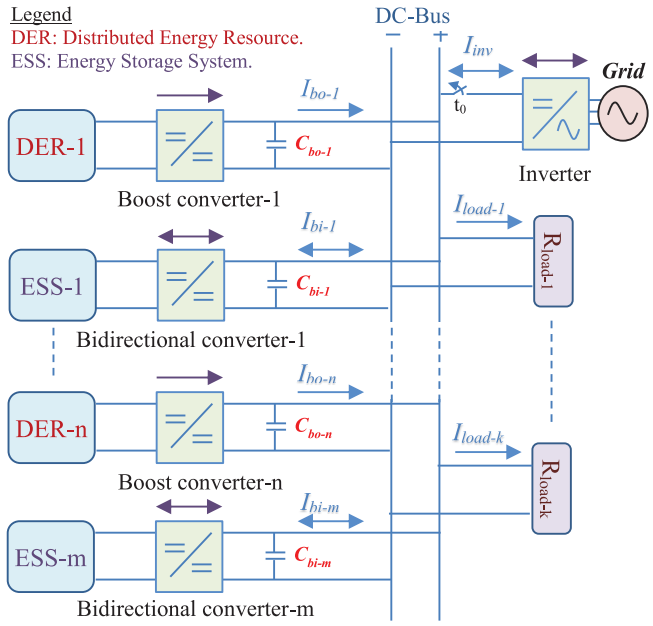


Fig. 2. Block diagram of a general DC microgrid.

A. Approximate Model

Considering the Block diagram of a general DC MG, at the islanding instant (t_o) as shown in Fig. 2, an approximate mathematical model was derived representing the circuit response. In case of delay and none of the converters is preserving the DC voltage, KCL can be applied at t_0 as follows:

$$\left(\sum_{i=1}^{n} C_{bo-i}+\sum_{j=1}^{m} C_{bi-j}\right)\times\frac{dV_{\text{Bus}}(t)}{dt}+\frac{V_{\text{bus}}(t)}{\left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1}} = \sum_{i=1}^{n+m} I_{DG-i} \tag{1}$$

Where

$$\sum_{i=1}^{n+m} I_{DG-i} = \sum_{j=1}^{m} I_{bi-j}+\sum_{i=1}^{n} I_{bo-i} \tag{1-a}$$

$$\frac{dV_{\text{Bus}}(t)}{dt} = \frac{-1}{\sum_{i=1}^{k} R_{\text{load}-i}\times\left(\sum_{i=1}^{n} C_{bo-i}+\sum_{j=1}^{m} C_{bi-j}\right)} \times\left(V_{\text{Bus}}(t)-\left(\sum_{i=1}^{n+m} I_{DG-i}\times\left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1}\right)\right) \tag{2}$$

Where C_{bi} and C_{bo} are the capacitances of the bidirectional and boost converters respectively, m and n are the numbers of bidirectional and boost converters, R_{load} is the DC bus load and k is their number connected the DC bus. Integrating (2):

$$\int_{V_{DC}(0-)}^{V_{\text{Bus}}(t)} \frac{dV_{\text{bus}}(t)}{V_{\text{bus}}(t)-\left(\sum_{i=1}^{n+m} I_{DG-i}\times\left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1}\right)} = \int_{t_0}^{t} \frac{-1}{\left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1}\times\left(\sum_{i=1}^{n} C_{bo-i}+\sum_{j=1}^{m} C_{bi-j}\right)}.dt \tag{3}$$

$$V_{\text{bus}}(t) = \left(\sum_{i=1}^{n+m} I_{DG-i}\times\left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1}\right) + \left(V_{DC}^{(0-)}-\left(\sum_{i=1}^{n+m} I_{DG-i}\times\left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1}\right)\right) \times e^{\frac{-\alpha}{\left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1}\times\left(\sum_{i=1}^{n} C_{bo-i}+\sum_{j=1}^{m} C_{bi-j}\right)}} \tag{4}$$

Where $V_{DC}^{(0-)}$ is the DC bus voltage just before the islanding, $\alpha = t - t_0$ is the delay time. (4) Introduces a rough estimation of how the DC bus voltage will behave in an islanding mode, while none of the MG agents received a signal to regulate the DC bus voltage, because of the time delay within centralized control. The accuracy of this model is noticeably degraded with increased latency, since the dynamics of the sources and converters were not included, as will be discussed in Section V.

B. Detailed Model

Considering the Block diagram shown in Fig. 2, during grid-connected operation, applying KCL at the DC bus:

$$\left(\sum_{i=1}^{n} C_{bo-i}+\sum_{j=1}^{m} C_{bi-j}\right)\frac{dV_{\text{Bus}}(t)}{dt} = I_G - I_D = \left(\pm I_{inv}\pm\left(\sum_{j=1}^{m} I_{bi-j}+\sum_{i=1}^{n} I_{bo-i}\right)-\sum_{i=1}^{k} I_{\text{load}-i}\right) \tag{5}$$

Where $I_G, I_D, I_{inv}, I_{bo}$ and I_{bi} are the generated currents from all sources, total demand, inverter, bidirectional and boost converters currents, respectively. During steady state, $I_G \approx I_D$. Therefore, the rate of change of the DC bus voltage with respect to time is almost zero. However, at the moment of islanding, $I_{inv} = 0$ A almost instantaneously, forcing the capacitors connected to the DC bus to inject or receive current (discharge or charge) to maintain its voltage level at the instant of

islanding.

$$\left(\sum_{i=1}^{n} C_{bo-i} + \sum_{j=1}^{m} C_{bi-j}\right) \frac{dV_{\text{Bus}}\ (t)}{dt} = \left(\sum_{j=1}^{m} I_{bi-j}|_{t_{0-}} + \sum_{i=1}^{n} I_{bo-i}|_{t_{0-}} + \sum_{j=1}^{m} \Delta I_{bi-j}|_{t_{0+}} + \sum_{i=1}^{n} \Delta I_{bo}|_{t_{0+}}\right) - \frac{V_{\text{bus}}\ (t)}{R_{eq}} \tag{6}$$

Where:

$$\sum_{i=1}^{n} I_{bo}|_{t_{0-}} = 1'_{1\times n} \cdot \left[\left(\mathrm{I}_n - \begin{bmatrix} D_1|_{t0-} & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & D_n|_{t0-} \end{bmatrix}\right) \cdot \begin{bmatrix} I_{pv-1}|_{0-} \\ \vdots \\ I_{pv-n}|_{0-} \end{bmatrix}\right] \tag{7}$$

$$\Delta I_{bo-i}|_{t_{0+}} \approx \pm \frac{C_{bo-i}}{\left(\sum_{i=1}^{n} C_{bo-i} + \sum_{j=1}^{m} C_{bi-j}\right)} .I_m \tag{8}$$

$$I_m = I_G|_{t_{0+}} - I_G|_{t_{0-}} = I_{inv} \tag{9}$$

$$\Delta I_{bi-j}|_{t_{0+}} \approx \pm \frac{C_{bi-j}}{\left(\sum_{i=1}^{n} C_{bo-i} + \sum_{j=1}^{m} C_{bi-j}\right)} .I_m \tag{10}$$

Where $I_{bo-i}|_{t_{0-}}$, $I_{bi-j}|_{t_{0-}}$, $I_{pv-i}|_{0-}$, $I_G|_{t_{0-}}$ and $D_i|_{t0-}$ are the boost, bidirectional, photovoltaic, generated currents and duty cycle right before islanding, respectively. The value of $I_{bi-i}|_{t_{0-}}$ is calculated based on the current reference prior to islanding, I_m is the difference between the currents $I_G|_{t_{0-}}$ and $I_G|_{t_{0+}}$ that was generated just before and after islanding. $\Delta I_{bo-i}|_{t_{0+}}$ and $\Delta I_{bi-i}|_{t_{0+}}$ are the difference in boost and bidirectional converters output currents just after islanding. The signs in (8) and (10) are dependent on whether $P_{\text{generated}}$ is greater or less than P_{demand} in the islanded mode. (6) could be rewritten as:

$$\frac{dV_{\text{bus}}\ (t)}{dt} = \frac{-1}{\sum_{i=1}^{k} R_{\text{load}-i} \times \left(\sum_{i=1}^{n} C_{bo-i} + \sum_{j=1}^{m} C_{bi-j}\right) \times \left(V_{\text{Bus}}(t) - I_G|_{t_{0+}} \times \left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1}\right)} \tag{11}$$

Where:

$$I_G|_{t_{0+}} = \sum_{j=1}^{m} I_{bi-j}|_{t_{0-}} + \sum_{i=1}^{n} I_{bo-i}|_{t_{0-}} + \sum_{j=1}^{m} \Delta I_{bi-j} + \sum_{i=1}^{n} \Delta I_{bo-i} \tag{12}$$

By integrating (11), (13) is obtained, then simplified to get (14):

$$\int_{V_{DC}\ (0-)}^{V_{bus}\ (t)} \frac{dV_{bus}\ (t)}{V_{bus}\ (t) - I_G|_{t_{0+}} \times \left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1}} = \int_{t_0}^{t} \frac{-dt}{\left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1} \times \left(\sum_{i=1}^{n} C_{bo-i} + \sum_{j=1}^{m} C_{bi-j}\right)} \tag{13}$$

$$V_{\text{Bus}}\,(t) = I_G|_{t_{0+}} \times \left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1} + \left(V_{DC}^{(0-)} - I_G|_{t_{0+}} \times \left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1}\right) \times e^{\frac{-\alpha}{\left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1} \times \left(\sum_{i=1}^{n} C_{bo-i} + \sum_{j=1}^{m} C_{bi-j}\right)}} \tag{14}$$

The dynamics of the sources and controllers need to be introduced to (14), to improve the accuracy of the model. At the instant of islanding, the increase/decrease in the DC/DC boost converter output current is governed by (8). This leads to a new operating point on the I–V curve of the solar array (towards $\{0, I_{sc}\}$ if I_m is $-$ve, and $\{V_{OC}, 0\}$ if I_m is $+$ve). The maximum power point (MPP) tracker (MPPT) attempts to recover to the MPP. However, since the delay time is short compared to the MPPT speed, the new operating point can be considered stationary during the delay time. Therefore, I_{bo-i} can be considered as a constant current source during that time, while the discharging rate will be dominated by the highest C_{bi} and the DC MG equivalent circuit will be as shown in Fig. 3, with the circuit components colored in blue connected. However, if there is C_{bo-i}, which is greater than any other individual capacitance, the discharging rate will be dominated by that C_{bo-i} and the equivalent circuit will be as shown in Fig. 3, with the circuit components colored in red connected instead of the blue ones. Therefore (12) and (14) can be written as follows:

$$I_G|_{t_{0+}} \approx \begin{cases} \sum_{j=1}^{m} I_{bi-j}|_{t_{0-}} + \sum_{i=1}^{n} I_{bo-i}|_{t_{0-}} + \sum_{\substack{j=1 \\ j\neq x}}^{n} \Delta I_{bi-j}|_{t_{0+}} + \sum_{i=1}^{n} \Delta I_{bo-i}|_{t_{0+}} & , \textit{Condition } 1 \\ \sum_{j=1}^{m} I_{bi-j}|_{t_{0-}} + \sum_{i=1}^{n} I_{bo-i}|_{t_{0-}} + \sum_{j=1}^{n} \Delta I_{bi-j}|_{t_{0+}} + \sum_{\substack{i=1 \\ i\neq y}}^{n} \Delta I_{bo-i}|_{t_{0+}} & , \textit{Condition } 2 \end{cases} \tag{15}$$

Where x is the number of the bidirectional converter that has the highest capacitance, y is the number of the boost converter that has the highest capacitance, Condition 1 is:

$$\exists j \left[\begin{array}{c} (\forall i\,(C_{bi-j} \geq C_{bo-i})) \wedge \\ (l = \{1,\ 2,\ \ldots m\}\,(l \neq j \rightarrow C_{bi-j} \geq C_{bi-l})) \end{array}\right] \tag{15-a}$$

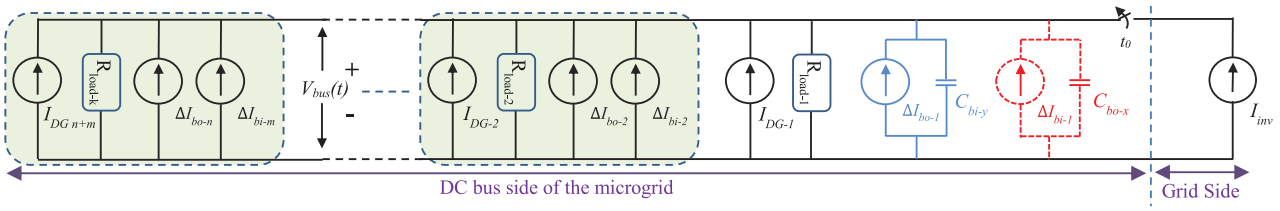


Fig. 3. DC microgrid approximate equivalent circuit in case of Condition 1 and 2.

And Condition 2 is:

$$\exists i \left[\begin{array}{c} (\forall j\,(C_{bo-i} > C_{bi-j})) \wedge \\ (l = \{1,\ 2,\ \ldots n\}\,(l \neq i \rightarrow C_{bo-i} > C_{bo-l})) \end{array} \right] \quad \text{(15-b)}$$

Conditions 1: Means that if there exists a bidirectional converter capacitance in the circuit which is greater than any other individual capacitance in the DC MG then $I_G|_{t_{0+}}$ can be approximated as shown in (15).

Conditions 2: Means that if there exists a boost converter capacitance in the circuit which is greater than any other individual capacitance, the discharging rate will be dominated by it.

$$V_{bus}(t) \approx \begin{cases} I_G|_{t_{0+}} \times \left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1} \\ + \left(\begin{array}{c} V_{DC}^{(0-)} - I_G|_{t_{0+}} \\ \times \left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1} \end{array} \right) \\ \overline{e^{\left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1} \times C_{bi-x}}}, \end{cases} \quad \textit{Condition 1}$$

$$\begin{cases} I_G|_{t_{0+}} \times \left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1} \\ + \left(\begin{array}{c} V_{DC}^{(0-)} - I_G|_{t_{0+}} \\ \times \left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1} \end{array} \right) \\ \overline{e^{\left(\sum_{i=1}^{k} 1/R_{\text{load}-i}\right)^{-1} \times C_{bo-y}}}, \end{cases} \quad \textit{Condition 2} \quad \text{(16)}$$

(4) and (16) will be used to calculate the DC bus voltage at the instant of islanding and during the delay, and their accuracies will be compared with detailed simulation results. During the delay, the controllers are blind and there is no local controller to regulate the DC bus voltage and therefore the bus voltage temporarily floats. (4) and (16) capture this floating behavior during the delay.

IV. DC Microgrid Case Study

A. System Topology

The topology of the DC MG example under study in this paper is depicted in Fig. 4. It comprises the followings: a 6 kW photovoltaic (PV) system that is integrated to the DC bus through a step up DC-DC converter, a 1.8 kW batteries integrated to the DC bus through a bidirectional DC-DC charger, a bidirectional AC-DC smart inverter tying the DC MG to the main grid. The working voltage of the DC MG is 300 V, and it includes a total load of 8 kW, where 1.5 kW connected to the AC side and 6.5 kW connected to the DC bus. The various individual converters are controlled locally, and a central MGCC is used to coordinate the operation of the local control agents and optimize the MG performance. The complete details about the example MG including the circuits design, the components values, the monitoring system, and the complete control algorithm can be found in [27]–[36].

B. System Control Scheme

The control hierarchy for the DC MG is a communication-based scheme. In the primary layer, the local controllers (LCs) are state driven (i.e., controlling their respective converters by continuously monitoring certain state variables), which requires incessant communication, e.g., voltage/current measurements and pulse signals to the switches of the converters. These types of signals are usually transmitted through wired communication channels since the LCs collocate with the measurement devices of their converters. In the secondary layer, the modes and set points are being assigned to each LC by the MGCC, to maintain the required voltage level within the DC MG and optimize its operation [29]. DC/AC agents are being utilized for monitoring purposes to detect and report any violations to the MGCC, e.g., exceeding the permissible voltage limits, according to the standards [37], [38]. Also, the relays within the protection system report any fault to the MGCC. In the presented control scheme, all signals received or sent by the MGCC (i.e., signals within the secondary layer) are wireless signals. These signals are explained in Table II and can be seen in Fig. 4.

The LCs of the DC MG understudy have different types of control. The boost converter LC (BLC) could operate as a voltage regulator or MPPT as shown in Fig. 4, based on the Cm_{Bo} signal from the MGCC. The bidirectional converter LC (BiLC) has two types of operation, current and voltage control. For the current control, two PIs are being utilized to reach the desired current reference for charging and discharging operations. For the voltage control, a nested PI is implemented as shown in Fig. 4. As for the inverter LC, it is responsible for fixing the DC bus voltage during the grid-tied mode. It could operate in current or voltage control. The inverter LC receives the voltage measurements of the three phases (v_{abc}) on the AC side, then the phase and frequency are acquired using phase locked loop (PLL) to enable synchronization with the main grid as shown in Fig. 4. Also, it receives the inverter output currents in the abc frame of reference and converts them to the $dq0$ frame of reference. In order to control the active and reactive current (i.e., power) separately, the inverter LC regulates I_d and I_q currents through separate PI controllers. Then, the output dq voltages, after decoupling, are used to generate the modulation signals.

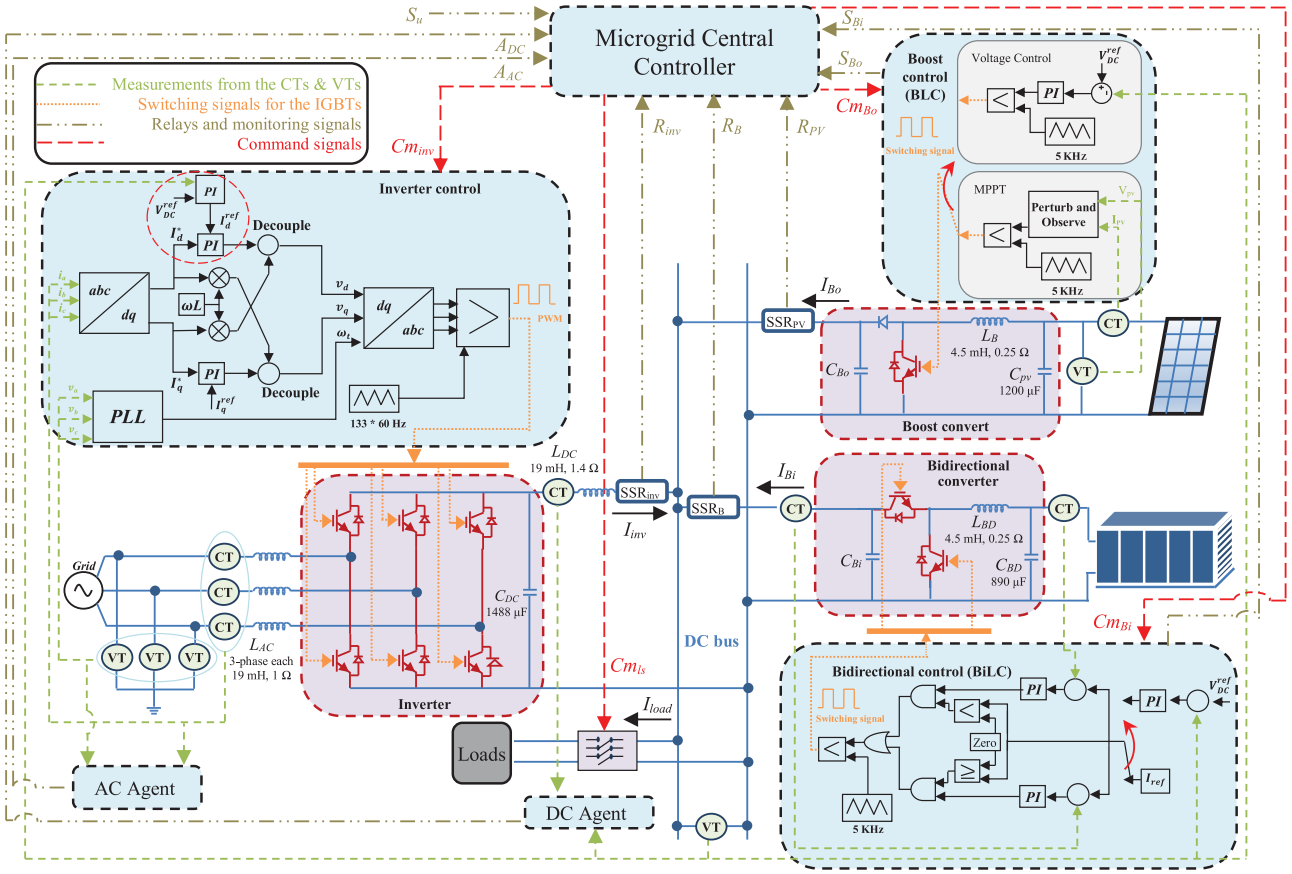


Fig. 4. DC microgrid under study.

TABLE II
SIGNALS TRANSMITTED AND RECEIVED BY THE MGCC

	Signals	Functionality
Command signals	Cm_{inv}	Select voltage or current control for the inverter
	Cm_{Bi}	Select voltage or current control for the bidirectional
	Cm_{Bo}	Select voltage or MPPT control for the Boost
	Cm_{ls}	Execute load shedding
Relay and monitoring signals	A_{DC}	DC agent reports violations of DC bus operation limits
	A_{AC}	AC agent reports violations of AC bus operation limits
	R_{inv}	Solid state relay signal within the inverter zone
	R_B	Solid state relay signal in the bidirectional zone
	R_{PV}	Solid state relay signal in the boost converter zone
	S_u	Cost signal from the utility
	S_{Bi}	Batteries state of charge signal
	S_{Bo}	BLC signals major changes in the V and I of the PV that the boost cannot supply the loads while fixing the bus voltage
	S_u	Utility pricing signal

For the inverter LC to regulate the DC bus voltage, I_d is regulated through another PI, which has two inputs, the desired DC bus voltage (V_{DC}^{ref}), and the measured one as shown in the red circle in Fig. 4. The values of K_p and K_i for all controllers are shown in the Appendix, Table III.

C. System Operational Modes

The MGCC of the DC MG shown in Fig. 4. operates in either grid-tied or islanded mode as shown in Figs. 5 and 6. Each mode encompasses several sub-modes. The MGCC triggers a transition between the modes/sub-modes based on the most recent and

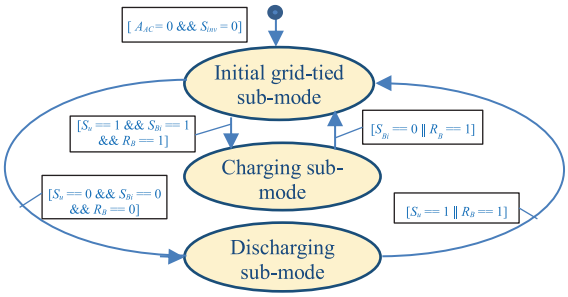


Fig. 5. Grid-tied sub-modes control logic/flowchart.

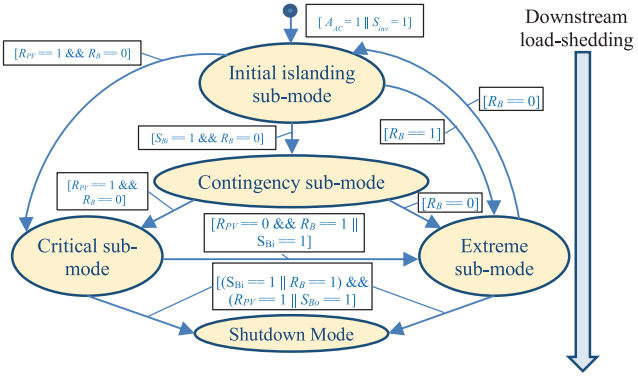


Fig. 6. Islanded sub-modes control logic/flowchart.

the stored signaled events from the agents, relays, and LCs. All transition triggering signals ($A_{DC}, A_{AC}, R_{inv}, R_B, R_{PV}, S_{bi}$, and S_u) are either one or zero, where "0" indicates normal operation and "1" indicates the opposite. For example, if R_B is "1," that means that the bidirectional converter is disconnected, when it's "0," it indicates normal operation.

Grid-tied Mode: In this mode, the objective is to maintain economic operation by managing the exchange of power between the MG and the main grid. The transition between the sub-modes occurs according to the pricing signal from the utility S_u, the state of charge of the batteries S_{Bi}, and the state of the bidirectional relay R_B. During normal operation, the MGCC commands the inverter LC to regulate the DC bus voltage, the BLC to perform MPPT, and the bidirectional converter to be neutral (i.e., current control with $I_{ref} = 0$). If S_u changed to "1" (i.e., energy price is low), the MGCC checks the last battery state of charge (SOC) to confirm it's not fully charged ($S_{Bi} = 0$), and $R_B = 0$ to assure that there is no fault operation, then a transition to the charging sub-mode takes place. In this sub-mode the BiLC start charging the batteries with maximum current (i.e., $I_{ref} = 5$ A, 1C) to exploit the advantages of low energy price, while the other LCs maintain the same operation. The rest of the transitions can be observed in Fig. 5 and Table IV.

Islanded Mode: This mode is either triggered if $\mathrm{SSR_{inv}}$ signals fault condition ($R_{inv} = 1$) or the AC agent reports a grid disconnection due to frequency or voltage violations on the AC side ($S_{AC} = 1$). The islanded mode contains initial islanding; contingency; critical; extreme; and shutdown sub-modes as shown in Fig. 6. Once this mode is triggered, the MGCC activate the initial islanding sub-mode commanding the BiLC to fix the bus voltage and the BLC to maintain MPPT control. If R_B changed to "1" (i.e., faulty operation of the bidirectional converter), a transition to the extreme sub-mode occurs. In this sub-mode, the boost converter regulates the bus voltage and a maximum load shedding is executed (i.e., 5$\sim$10% of the total loads). This is because of the intermittent nature associated with the photovoltaic generation. During the extreme sub-mode, if R_{PV} changed to "1" indicating faulty operation of the boost converter, or S_{Bo} changed to "1" indicating sever intermittency, a transition to the shutdown sub-mode will take place. This transition occurs to preserve the safety of the connected loads. The rest of transitions can be observed in Fig. 6 and Table IV.

The MG was designed to self-sustain its loads during initial islanding sub-mode. There are three levels of load shedding within the rest of sub-modes. The first level of load shedding is executed during the contingency sub-mode such that a portion of the solar energy power is supplying the critical loads and the rest is charging the batteries for emergencies. The second level of load shedding takes place during the critical sub-mode when the boost converter is tripped, or it is sunset. Load shed in this sub-mode is done such that the amount of power of connected loads is equal to that from batteries. The maximum level of load shed is commanded during the extreme sub-mode such that the connected loads has minimal demand and could withstand a wide range of voltage variations to handle solar fluctuations due to intermittency. Through these sub-modes, load shed is done in a downstream unidirectional fashion (i.e., no reconnection of loads unless the normal operation is restored).

In order to analyze the impact of ICT dependence, we will intentionally delay the control messages between the MGCC and LCs and inspect the impact on the MG operation and the transitions between its sub-modes. If the signal transmitted from the MGCC to the LC that is supposed to fix the bus voltage is delayed, then no converter is regulating the MG bus voltage during the delay. Therefore, the DC bus voltage temporarily floats, which may lead to the MG shutdown if the V or I swing meet one of the protection system pick-up thresholds.

V. Results and Discussion

The proposed control scheme operations described in the previous section will be shown through selected case studies, during which a series of transitions between the sub-modes of the islanding and grid-tied modes take place. The cases will be presented by two sub-plots showing five different states of operation. The first sub-plot of each case shows the load, inverter, bidirectional, and boost converter currents. The second sub-plot shows the variation of the DC bus voltage. Two cases will be presented showing the DC MG operation in grid-tied and islanded modes. A third case will be presented to show the impact of delay on the MG operation during the transitions between the islanding sub-modes. Then the math model validation and applications will be discussed.

A. Cases Demonstrating the DC MG Operations

Case 1: Demonstrates the MGCC control during the grid-tied mode, the connected loads to the DC bus in this scenario are equal to 3.6 kW. BLC is MPPT controlled, BiLC is in a neutral state (i.e., $I_{ref} = 0$), and the inverter is regulating the bus voltage to 300 V. During segment (1), S_u changed to "1" indicating low energy price. The MGCC checks the last signal sent from $\mathrm{SSR_{Bi}}$ to confirm the bidirectional converter connectivity ($R_B = 0$) and the last signal from BiLC confirming that the batteries are not fully charged ($S_{Bi} = 0$). Then the MGCC switch to the charging sub-mode commanding the BiLC to charge the batteries with 1C (i.e., current control with $I_{ref} = 5$ A) to take advantage of the low energy price. It can be seen in Fig. 7(a) that the bidirectional current (I_{Bi}) changed to -5 A and since the inverter is maintaining the bus voltage, the inverter current (I_{inv}) increased to 5 A while the boost converter (I_{Bo}) and load (I_{load}) currents still the same. In segment (2), BiLC signals that the batteries are fully charged ($S_{Bi} = 0$), then a transition back to the initial grid-tied happens. It can be seen in Fig. 7(a) that I_{bi} and I_{inv} dropped to zero since the MG can self-sustain its loads, maintaining the bus voltage to 300 V as shown in Fig. 7(b). In segment (3), the intermittency of the solar energy is demonstrated. The solar irradiance started to decrease gradually leading to a gradual decrease in I_{Bo}, simulating an example of a passing cloud. It can be seen from Fig. 7(a) that I_{inv} started to increase gradually as well to maintain the bus voltage. Throughout segment (4), the solar irradiance goes back to its value in segment (1) and I_{Bo} and I_{inv} as well, as seen in Fig. 7. During

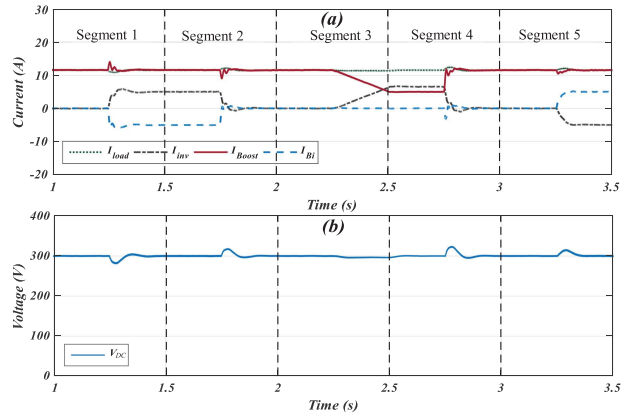


Fig. 7. Case 1 shows the MGCC control operation during grid-tied mode.

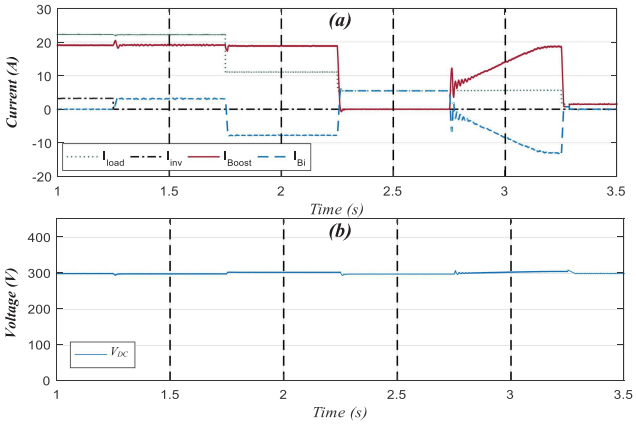


Fig. 8. Case 2 shows the MGCC control operation during islanded mode.

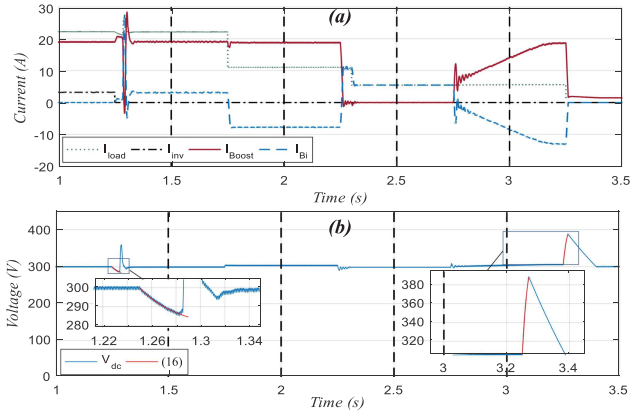


Fig. 9. Case 3 shows the impact of delay during the islanded mode operation.

the last segment, S_u changes to "0" (i.e., high energy price). The MGCC checks the last status of the batteries SOC to make sure it can discharge ($S_{Bi} = 1$) and that $R_B = 0$, then a transition to the discharging sub-mode occurs. The MGCC tries to increase the economic savings by commanding the BiLC to discharge the batteries at a rate of 1C. It can be observed that I_{Bi} changes to 5 A and I_{inv} changes to -5 A to maintain the DC bus voltage to 300 V.

Case 2: Shows the MGCC operation during islanded mode. The connected loads to the DC bus are 6.5 kW, and the total connected capacitance is 4800 μF. The first segment shows a transition to the initial islanding sub-mode due to power outage signaled by the AC agent or SSR_{inv} ($A_{AC} = 1$ or $R_{inv} = 1$), where I_{inv} drops to zero as shown in Fig. 8(a). Through this sub-mode, the MGCC commands BiLC to maintain the DC bus voltage ($Cm_{Bi} = 1$), while the BLC to keep operating as MPPT ($Cm_{Bo} = 0$). It can be seen from Fig. 8(a) that I_{Bi} increases to cover the loss of I_{inv}. In segment (2), BiLC signals batteries depletion ($S_{Bi} = 1$). The MGCC subsequently checks the last SSR_{Bo} signal to confirm that the boost converter is connected ($R_{PV} = 0$) and then triggers a transition to the contingency sub-mode. Within this sub-mode, the first level of load shed is triggered ($Cm_{ls} = 01$) and the extra energy from the solar panels is utilized to charge the batteries with a rate of 2C to prepare it for emergencies. These changes could be observed in Fig. 8(a), where the load current dropped as a result of the load shed ($\sim$11 A) and the bidirectional starts charging instead of discharging (i.e., current changes from $\sim$3 A to -8 A) maintaining the bus voltage to 300 V. During segment (3), SSR_{Bo} signals the tripping of the boost converter ($R_{PV} = 1$). The MGCC checks the last SSR_{Bi} signal to confirm it's not tripped and then switches to the critical sub-mode. In this sub-mode, the second level of load shed is triggered ($Cm_{ls} = 10$) such that the amount of the load power connected to the bus is equal to the batteries power, which corresponds to 1C. These changes could be seen in Fig. 8(a), where I_{Bo} drops to zero while I_{Bi} and I_{load} coincide at 5 A. In segment (4), the boost converter is reconnected and the solar irradiance is increasing (i.e., a cloud is moving away from the solar panels) leading to a gradual increase in I_{Bo}. It can be seen in Fig. 8(a) that as I_{Bo} increases gradually, I_{Bi} decreases gradually to maintain the bus voltage. During the last segment, SSR_{Bo} signals that the bidirectional is tripped ($R_B = 1$). Then the MGCC confirms that the boost converter is connected ($R_{PV} = 0$), subsequently a transition to the extreme sub-mode is triggered. In this sub-mode, the MGCC commands the BLC to regulate the bus voltage ($Cm_{Bo} = 1$) and maximum level of load shed ($Cm_{ls} = 11$). The remaining connected loads can handle voltage variations as explained earlier. It can be seen in Figs. 8(a) and 8(b) that I_{Bi} drops to zero while I_{Bo} and I_{load} coincide, and the bus voltage was fixed at 300 V through all transitions.

Case 3: Is similar to case 2; however, a delay is imposed on different signals during the transitions. During segment (1), The MGCC receives a signal ($R_{inv} = 1$) and then sends a command signal ($Cm_{Bi} = 1$) while the other controllers maintain the same operation. A delay of 40 msec in total has been imposed on the received-sent signals to the MGCC. During this delay, there was no LC regulating the bus voltage and since $I_{\text{load}} > I_{Bo}$, the DC bus voltage started to decrease as shown in Figs. 9(a) and 9(b). Once the delay ended and the BiLC received the command signal ($Cm_{Bi} = 1$), it attempted to retain the bus voltage to 300 V. It can be noticed in Fig. 9(a) high oscillations once the BiLC starts regulating the bus voltage due to the increased error

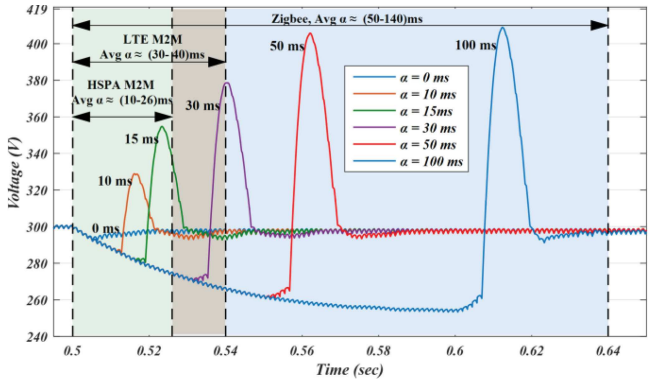


Fig. 10. $V_{\text{Bus}}(t)$ with different α, $C_T = 4800\ \mu$F and $I_m = 7.1$ A.

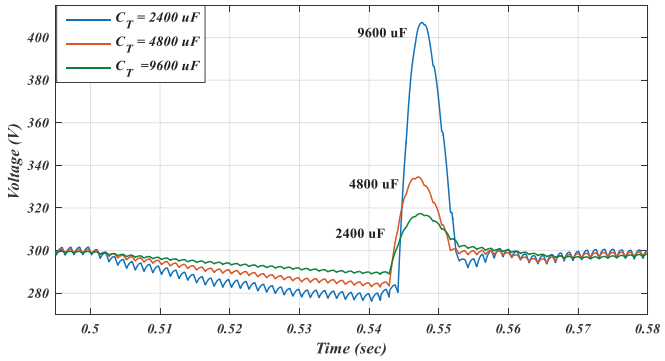


Fig. 11. $V_{\text{Bus}}(t)$ with different C_T, $C_{bi} : C_{bo}$ = 1:1, $\alpha = 40$ msec and $I_m = 3.2$ A.

input to its PI controller, which will be explained in the next sub-section. During segment (2), the MGCC receives a signal ($S_{Bi} = 1$) and sends a signal ($Cm_{ls} = 01$). A delay of msec order in this segment will not have a significant impact on the batteries SOC. In segment (3), the MGCC receives a signal ($R_{PV} = 1$) and sends a command ($Cm_{ls} = 10$). A collective delay of 50 msec was imposed on the received-sent signals to the MGCC. It can be seen from Fig. 9(a) that the delay led to over discharge of the batteries during the delay interval. This is because BiLC is responsible for regulating the bus voltage during this period of time. During the last segment, the MGCC receives a signal ($R_B = 1$) and send two signals to execute load shed ($Cm_{ls} = 11$) and to change the boost converter control ($Cm_{Bo} = 1$). A collective delay of 20 msec has been imposed on the received-sent signals (R_B and Cm_{Bo}). During this delay, the bidirectional converter was disconnected and there was no LC regulating the bus voltage. It can be seen from Fig. 9(b) that the bus voltage has increased significantly because I_{Bo} is much higher than I_{load} during the delay. Once the BLC received the command to regulate the bus voltage after the delay ended, the bus voltage started to be retained to its original value 300 V. It can be seen in the zoomed areas in Fig. 9(b) that (16), derived in Section III, matches the simulation results, which will be further explained in the following section.

B. Mathematical Model Verification

The mathematical models derived in Section IV, representing communication delay impact on the DC MG bus voltage, were compared and validated with the help of results obtained from the Simulink model in Fig. 4. The variation of $V_{bus}(t)$ during MG islanding with various delays (i.e., representing different wireless techs), mismatch currents (i.e., demonstrating several operating conditions), capacitance ratios and total capacitance (i.e., showing different designs) was shown and analyzed in this section. The delay event starts at 0.5 sec in the following results.

Fig. 10 shows the effect of different intervals of delays (α) on the DC bus voltage with constant total capacitance ($C_T = 4800\ \mu$F), and mismatch current ($I_m = 7.1$ A). The first shaded area represents the average delay of the HSPA M2M technology ($\alpha \approx 10 \sim 26$ msec), the second shaded area represents the delay of LTE M2M, which is almost double the first one ($\alpha \approx 30 \sim 40$ msec), then the Zigbee technology latency, which is higher ($\alpha \approx 50 \sim 140$ msec). Hybrid communications shall have a delay-impact in-between these curves. It can be noticed that as the delay lasts longer, the voltage deviation increases, which leads to an increased error in the PI controller of the bidirectional converter, that is supposed to regulate the bus voltage in case of islanding, causing higher spikes. This error could be expressed as $e(t = \alpha) = V_{ref} - V_{bus}(t = \alpha)$, where $V_{bus}(t)$ could be calculated from (16) and subsequently calculate the expected error. With HSPA M2M, LTE M2M and Zigbee, at this value of C_T and I_m, the voltage deviation reaches up to 6.67%, 10%, and 16.67%, respectively. Furthermore, the voltage deviation is a function of the mismatch current I_m and total capacitance C_T as well, i.e., worst-case scenario could take place if the generated power from the DERs at the instant of islanding is zero, e.g., a cloud was passing by the solar panels, the batteries were depleted and C_T was critically small. This scenario might lead to swift changes in the voltage level, triggering protection relays of the DC MG, which are occasionally based on the (d/dt) values of voltage and current, and/or voltage limits of $\pm(0.05 \sim 0.01$ pu) [37]. Spikes are a function of $C_{bi} : C_{bo}$ among other variables, which will be discussed hereafter.

Fig. 11 demonstrates how the DC bus voltage behaves with different C_T values, fixed $\alpha = 40$ msec and $I_m = 3.2$ A. It can be seen that the rate of voltage deviation is decreasing with the increase in the capacitance value, as the discharge rate is governed by $e^{\alpha/\tau_{MGI}}$, where τ_{MGI} is the circuit time constant, which is equal to $(\sum_{i=1}^{k} 1/R_{\text{load}-i})^{-1} \times (\sum_{i=1}^{n} C_{bo-i} + \sum_{j=1}^{m} C_{bi-j})$.

Fig. 12 presents the DC bus voltage behavior at fixed $C_T = 4800\ \mu$F, $\alpha = 40$ msec and various mismatch currents. It can be noticed that as the I_m increase/decreases, the DC bus voltage varies proportionally with it. If $P_{\text{generated}} \approx P_{\text{demand}}$, the DC bus voltage remains around 300 V, as shown when $I_m \approx -0.25$ A.

Fig. 13 verifies that at the islanding moment, for different I_m values, constant $\alpha = 40$ msec, $C_{bi} : C_{bo}$ = 1:1 and $C_T = 4800\ \mu$F, the average output boost current changes suddenly and almost stays at the new operating point during the delay (varies slowly), since the latency duration is short compared to the

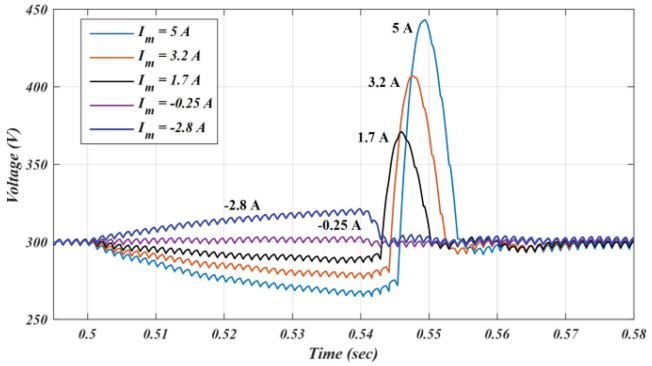


Fig. 12. $V_{\text{Bus}}(t)$ with different I_m, $\alpha = 40$ msec, $C_{bi} : C_{bo} =$ 1:1 and $C_T = 4800$ μF.

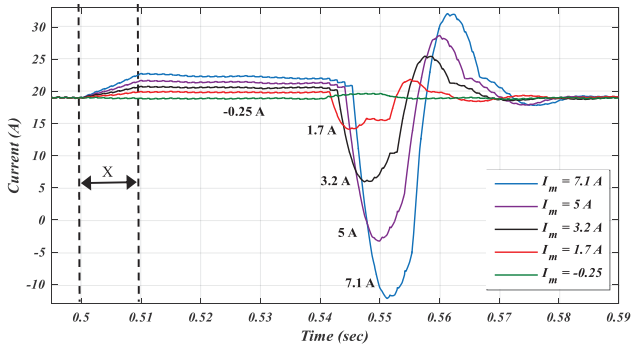


Fig. 13. I_{Boost} with different I_m, $\alpha = 40$ msec, $C_{bi} : C_{bo} =$ 1:1 and $C_T = 4800$ μF.

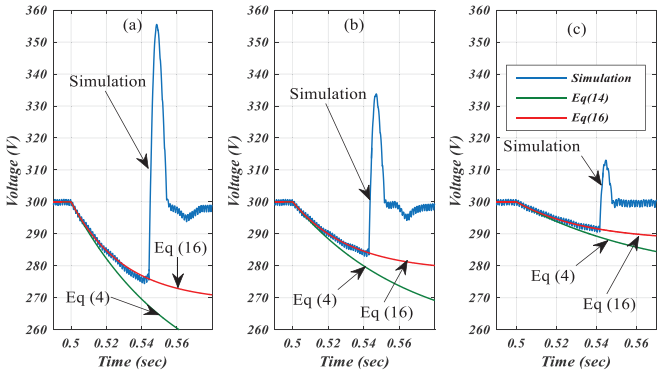


Fig. 14. $V_{\text{Bus}}(t)$ of (4), (16) and simulation results with different I_m, $\alpha = 40$ msec, $C_{bi} : C_{bo} =$ 1:1 and $C_T = 4800$ μF: (a) $I_m = 5$. (b) $I_m =$ 3.2 A. (c) $I_m = 1.7$ A.

MPPT speed, which is consistent with (15) when $C_{bi} \geq C_{bo}$. In addition, it can be noticed that in the time interval marked (X) all the currents take 10 msec to reach the new operating point. This is due to the low pass filter, which collects the measurements with an average of 100 cycle/sec.

Fig. 14 shows a comparison of (4), (16) and the simulation results at different I_m and constant $\alpha = 40$ msec, $C_{bi} : C_{bo} =$ 1:1 and $C_T = 4800$ μF. It can be seen that the error in (4) is around 20% and increases with α, while it's less than 4% in (16). This is due to the fact that (4) was simplified using ideal sources.

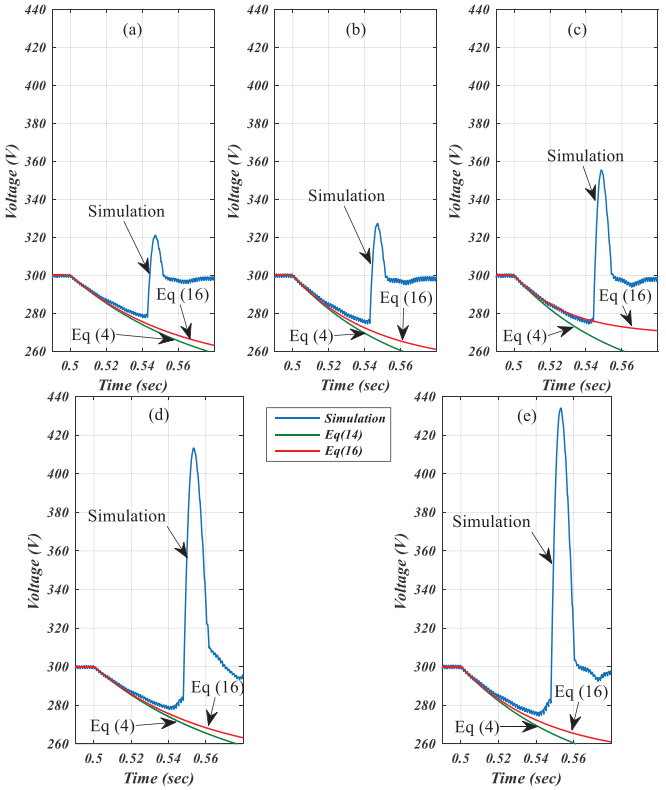


Fig. 15. $V_{\text{Bus}}(t)$ of (4), (16) and simulation at $\alpha = 40$ msec, $I_m = 5$ A and various $C_{bi} : C_{bo}$. (a) 1200:4800. (b) 1200:3600. (c) 2400:2400. (d) 4800:1200. (e) 3600:1200 μF.

Fig. 15 shows a comparison of (4), (16) and the simulation results at different capacitance ratios and constant $\alpha = 40$ msec and $I_m = 5$ A. It can be noticed that the error increases in (4) and (16) as the ratio $C_{bi} : C_{bo}$ varies from unity, this can be explained in (16) due to the approximation, that one of the DERs with its converter, could be represented as a current source depending on the ratio of $C_{bi} : C_{bo}$ as mentioned earlier in Section IV. Furthermore, it can be seen that as C_{bo}/C_{bi} increases, the DC voltage spike decreases and that is because most of the current injected by C_{bi} to recover to 300 V is being absorbed by the bigger capacitor C_{bo}. Moreover, this has to do with the dynamics of the PI controllers, sources and the converters after the delay ends, which is beyond the scope of this paper. It can be perceived from Figs. 14 and 15 that (16) can be used to represent the behavior of the DC bus during a delay.

Fig. 16(a) captures the floating behavior of the DC bus voltage during the delay using the mathematical model (16). It represents the variation of the mismatch current I_m, delay α and the DC bus voltage $V_{\text{bus}}(t)$ in (16) at load demands 7.8 kW, DERs generation ≥ 5.7 kW, $C_T = 2400$ μF and capacitance ratio 1:1. It can be observed that as the delay and the mismatch current increase ($I_{DERs} -_{\text{generation}}|_{t0-}$ greater than $I_{\text{demand}}|_{t0-}$), $V_{\text{bus}}(t)$ increases. This is because once the inverter got disconnected, the extra current that was going to the grid started to increase the bus voltage since there was no LC to regulate the voltage during the delay (i.e., take the extra current). While, as the delay increases and mismatch current decreases, $V_{bus}(t)$ decreases.

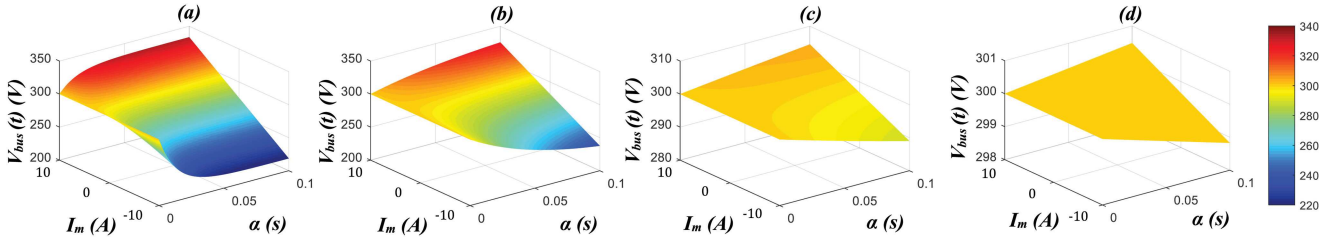


Fig. 16. Representation of the mathematical model (16) showing the DC bus voltage behavior of the MG with the variation of I_m and α, at operational conditions: load demands = 7.8 kW and DERs generation ≥5.7 kW, and at different C_T. (a) 2*1200 μF. (b) 10*1200 μF. (c) 100*1200 μF. (d) 1000*1200 μF.

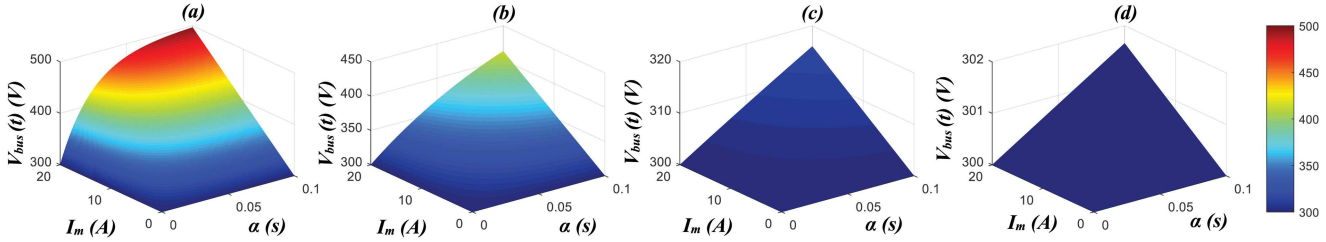


Fig. 17. Representation of the mathematical model (16) showing the DC bus voltage behavior of the MG with the variation of I_m and α.at operational conditions: load demands = 4.5 kW and DERs generation ≥4.5 kW, and at different C_T. (a) 2*1200 μF. (b) 10*1200 μF. (c) 100*1200 μF. (d) 1000*1200 μF.

This is because $P_{\text{generation}}|_{t0-}$ of the DERs $< P_{\text{demand}}|_{t0-}$ (i.e., the MG was receiving current from the grid right before the inverter got disconnected and the delay occurrence). At $\alpha =$ zero (i.e., no delay), it can be seen that the DC bus voltage will be $V_{DC}^{(0-)}$, which is the value of the bus voltage right before any delay happens, in our case it is 300 V, assuming the voltage was regulated by one of the LCs. This validates (16) conceptually.

Also, it can be seen in Fig. 16(a) that $V_{bus}(t)$ could vary between ∼116% and 67% of its original value (i.e., 300 V) under these operational conditions with long delays. It can be noticed in Figs. 16(a)–16(d) that as C_T increases, $V_{bus}(t)$ variation decreases, and at high C_T values, $V_{bus}(t)$ variation becomes >0.3% (i.e., > 1 V) as shown in Fig. 16(d). Then it can be perceived that as a physical solution to mitigate the latency impact of the ICT to be used in the MG, is to increase C_T.

Figs. 17(a)–17(d) are similar to Figs. 16(a)–16(d). However, the MG operational condition inputs to the mathematical model were $P_{\text{demand}} = 4.5$ and DERs generation ≥4.5 kW. It can be seen that at $I_m =$ zero (i.e., MG was not sending or receiving any current to the grid), $V_{bus}(t)$ is fixed at 300 V regardless of α. This is due to the operational conditions of the MG right before and during the delay (i.e., $I_{\text{demand}}|_{t0-} = I_{\text{generation}}|_{t0-}$). Also, it can be seen that the bus voltage could reach up to ∼500 V with $\alpha = 100$ msec under certain operational conditions.

VI. Conclusion

This paper presents a control scheme for DC MGs and analyzes the impact of latency of various wireless communication technologies, within HAN, on the DC CCMGs performance. Mathematical models were developed to illustrate and predict the behavior of MGs during latencies. It was found that the impact severity varies with the mismatch current, which is an unpredictable factor, and the total capacitance/capacitance ratios of the converters, which is a design factor. This study suggests that the design of an MG should be coordinated along with the selection of the ICT. If cost-effective ICT with long delays is to be deployed, more investment has to be done on the MG design. For example, if Zigbee is to be used, a high capacitance should be utilized to mitigate the impact of long delays, and if HSPA M2M is to be employed, less capacitance is required. However, the use of large capacitances to compensate for the mechanical inertia, as in the AC systems, leads to high fault currents. Moreover, long latencies at high mismatch current and low capacitance will cause a swift change in DC bus voltage and current, which might cause the protection relays to be triggered. Therefore, MGs should be designed, while considering ICT latency, the capacitance of the DER's converters, protection relay settings and the proposed mathematical models to have more sustainable CCMGs.

The mathematical model could be used to give insight and predict the DC bus voltage behavior during a delay. The inputs to the mathematical model are design parameters, the total capacitance, capacitances ratio of the DERs, and ICT to be used. The operational condition inputs to the mathematical model are the load demands and the DERs generation. The output shall show the DC bus variation under the various selected operational conditions, which could be used either to alter the MG design parameters or change the protection set points to tolerate the delay impact while no LC is regulating the bus voltage. The model shows a physical solution to mitigate the impact of latency of the ICT to be used in the MG, which is increasing the total capacitance connected to the DC bus C_T.

Appendix

Functionalities of LCs are highlighted in blue in Table IV.

TABLE III
TRANSITIONS BETWEEN FUNCTIONAL SUB-MODES WITHIN THE ISLANDED AND GRID-TIED MODES OF OPERATION

Islanding Mode Transitions		
Present Sub-mode	**Next Sub-mode**	**Transition Explanation**
Initial islanding - BLC operates with MPPT control -BiLC maintain the DC bus voltage	Contingency	Batteries are depleted and boost converter is available
	Critical	Boost converter is tripped and bidirectional converter is available
	Extreme	Bidirectional converter is tripped
	Shutdown	-
Contingency - BLC operates with MPPT control -BiLC charges the batteries while maintaining the DC bus voltage -Trigger the 1st level of load shedding	Islanding	-
	Critical	Boost converter is tripped and bidirectional converter is available
	Extreme	Bidirectional converter is tripped
	Shutdown	-
Critical -BiLC maintain the DC bus voltage -Trigger the 2nd level of load shedding	Islanding	-
	Contingency	-
	Extreme	Boost is tripped and bidirectional is available, or batteries are depleted
	Shutdown	Boost and bidirectional converters are tripped
Extreme -BLC maintain the DC bus voltage -Trigger the maximum level of load shedding	Islanding	Bidirectional converter is available
	Contingency	-
	Critical	-
	Shutdown	Boost and bidirectional converters are tripped
Grid-tied Mode Transitions		
Initial grid-tied -Inverter LC regulates the DC bus voltage - BLC operates with MPPT control -BiLC operate with current control $I_{ref} = 0$	Charging	Energy price is low, the bidirectional converter is available, and the batteries are not fully charged
	Discharging	Energy price is high, the bidirectional converter is available, and the batteries are fully/near full charged
Charging -Inverter LC & BLC maintain similar operation -BiLC operate with current control I_{ref} = maximum charging current	Initial grid-tied	Batteries got fully charged or bidirectional converter got disconnected
	Discharging	-
Discharging -Inverter LC & BLC maintain similar operation -BiLC operate with current control I_{ref} = maximum discharge	Initial grid-tied	Batteries are not fully charged, or bidirectional converter got disconnected
	Charging	-

TABLE IV
Kp AND K_i OF VARIOUS CONTROL TECHNIQUES USED IN THE DC MG

Converter	Control technique	Outer Loop		Inner Loop			
				Charge		Discharge	
		K_p	K_i	K_p	K_i	K_p	K_i
Bidirectional converter	Current	N/A	N/A	0.02	110	0.02	3
	Voltage	3	1	0.002	10	0.02	3
		Outer Loop		I_d		I_q	
Inverter	Current	N/A	N/A	192.1	97671	192.1	97671
	Voltage	0.1	10	192.1	97671	192.1	97671
Boost converter	Voltage	0.02	100	N/A	N/A	N/A	N/A
	MPPT	N/A	N/A	N/A	N/A	N/A	N/A

REFERENCES

[1] Y.-F. Huang, S. Werner, J. Huang, N. Kashyap, and V. Gupta, "State estimation in electric power grids: meeting new challenges presented by the requirements of the future grid," *IEEE Signal Process. Mag.*, vol. 29, no. 5, pp. 33–43, Sep. 2012.

[2] *Smart Grid*, Dept. Energy, Washington, DC, USA, Jun./Jul. 2016.

[3] E. Ancillotti, R. Bruno, and M. Conti, "The role of communication systems in smart grids: Architectures, technical solutions and research challenges," *Comput. Commun.*, vol. 36, pp. 1665–1697, 2013.

[4] C. Greer *et al.*, "NIST framework and roadmap for smart grid interoperability standards, release 3.0," U.S. Nat. Inst. Standards Technol., Gaithersburg, MD, USA, Tech. Rep. 1108r3, Oct. 2014.

[5] F. Wu, K. Moslehi, and A. Bose, "Power system control centers: Past, present, and future," *Proc. IEEE*, vol. 93, no. 11, pp. 1890–190, Nov. 2005.

[6] L. Atzori, A. Iera, and G. Morabito, "The internet of things: A survey," *Comput. Netw.*, vol. 54, no. 15, pp. 2787–2805, 2010.

[7] Microgrid Activities, Dept. Energy, Washington, DC, USA, Mar. 2016.

[8] A. Ali, A. Farooq, Z. Muhammad, F. Habib, and S. Malik, "A review: DC microgrid control and energy management system," *Int. J. Elect. Electron. Sci.*, vol. 2, p. 24–30, 2015.

[9] P. Karlsson and J. Svensson, "DC bus voltage control for a distributed power system," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1405–1412, Nov. 2003.

[10] R. S. Balog, "Autonomous local control in distributed DC power systems," Ph.D. dissertation, Univ. Illinois, Champaign, IL, USA, 2006.

[11] T. Dragicevic, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC microgrids—Part I: A review of control strategies and stabilization techniques," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4876–4891, Jul. 2016.

[12] Y. Ito, Y. Zhongqing, and H. Akagi, "DC micro-grid based distribution power generation system," in *Proc. IEEE Int. Power Electron. Motion Control Conf.*, 2004, vol. 3, pp. 1740–1745.

[13] M. Parandehgheibi and E. Modiano, "Robustness of interdependent networks: The case of communication networks and the power grid," in *Proc. IEEE Global Commun. Conf.*, Dec. 2013, pp. 2164–2169.

[14] V. Rosato, L. Issacharoff, F. Tiriticco, S. Meloni, S. De Porcellinis, and R. Setola, "Modelling interdependent infrastructures using interacting dynamical models," *Int. J. Crit. Infrastruct.*, vol. 4, Jan. 2008, pp. 63–79.

[15] M. Rahnamay-Naeini and M. M. Hayat, "On the role of power-grid and communication-system interdependencies on cascading failures," in *Proc. IEEE Global Conf. Signal Inf. Process.*, Austin, TX, USA, Dec. 2013, pp. 527–530.

[16] S. C. Liu, X. Y. Wang, and P. X. Liu, "Impact of communication delays on secondary frequency control in an islanded microgrid," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 2021–2031, Apr. 2015.

[17] C. A. Macana, E. Mojica-Nava, and N. Quijano, "Time-delay effect on load frequency control for microgrids," in *Proc. 10th IEEE Int. Conf. Netw. Sens. Control*, Apr. 2013, pp. 544–549.

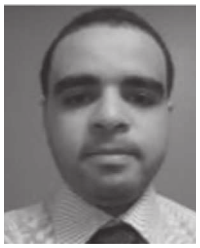
[18] X. Lu, J. M. Guerrero, K. Sun, and J. C. Vasquez, "An improved droop control method for DC microgrids based on low bandwidth communication with dc bus voltage restoration and enhanced current sharing accuracy," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1800–1812, Apr. 2014.

[19] Q. Shafiee, T. Dragicevic, J. C. Vasquez, and J. M. Guerrero, "Hierarchical control for multiple DC-microgrids clusters," *IEEE Trans. Energy Convers.*, vol. 29, no. 4, pp. 922–933, Dec. 2014.

[20] M. Kuzlu, M. Pipattanasomporn, and S. Rahman, "Communication network requirements for major smart grid applications in HAN, NAN and WAN," *Comput. Netw.*, vol. 67, pp. 74–88, Jul. 2014.

[21] S. Safdar, B. Hamdaoui, E. Cotilla-Sanchez, and M. Guizani, "A survey on communication infrastructure for micro-grids," in *Proc. IEEE 9th Int. Wireless Commun. Mobile Comput. Conf.*, Jul. 2013, pp. 545–550.

[22] A. Llaria, G. Terrasson, O. Curea, and J. Jimenez, "Application of wireless sensor and actuator networks to achieve intelligent microgrids: A promising approach towards a global smart grid deployment," *Appl. Sci.,* vol. 6, Feb. 2016, pp. 1–23.
[23] M. Kuzlu, "Assessment of communication technologies and network requirements for major smart grid applications," in *Proc. IEEE PES Innovative Smart Grid Technol.*, 2013, pp. 1–6.
[24] H. Sherazi, R. Iqbal, S. Hassan, M. Chaudary, and S. Gilani, "ZigBee's received signal strength and latency evaluation under varying environments," *J. Comput. Netw. Commun.*, vol. 2016, 2016, Art. no. 5.
[25] M. Laner, P. Svoboda, P. Romirer, N. Nikaein, and F. Ricciato, "A comparison between one-way delays in operating HSPA and LTE networks," in *Proc. 10th Int. Symp. Model. Optim. Mobile Ad Hoc Wireless Netw.*, 2012, pp. 286–292.
[26] Swappa :: Reti wireless - zigbee, Oct./Nov. 2016.
[27] M. Saleh, Y. Esa, and A. Moahmed, "Communication based control for DC micrgrids," *IEEE Trans. Smart Grid*, Jan. 2018, [Online]. Available: https://doi.org/10.1109/TSG.2018.2791361.
[28] M. Saleh, Y. Esa, and A. Mohamed, "Hardware based testing of communication based control for DC microgrid," in *Proc. Int. Conf. Renew. Energy Res. Appl.*, San Diego, CA, USA, 2017, pp. 902–907.
[29] M. Saleh, Y. Esa, and A. Moahmed, "Design and implementation of CCNY DC microgrid testbed," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, Portland, OR, USA, Oct. 2016, pp. 1–7.
[30] M. Saleh, Y. Esa, and A. Moahmed, "Centralized control for DC microgrid using finite state machine," in *Proc. IEEE Innovative Smart Grid Technol. Conf.*, Washington, DC, USA Apr. 2017, pp. 1–5.
[31] M. Saleh, Y. Esa, and A. Mohamed, "Application of complex network analysis in electric power systems," *Energies*, vol. 11, Mar. 2018, Art. no. 1381.
[32] M. Saleh, Y. Esa, and A. Moahmed, "Energy management algorithm for resilient controlled delivery grids," in *Proc. Ind. Appl. Soc. Conf.*, Cincinnati, OH, USA, Oct. 2017, pp. 1–8.
[33] M. Saleh, O. Dutta, Y. Esa, and A. Moahmed, "Quantitative analysis of regenerative energy in electric rail traction systems," in *Proc. Ind. Appl. Soc. Conf.*, Cincinnati, OH, USA, Oct. 2017, pp. 1–7.
[34] M. Saleh, A. Althaibani, Y. Esa, Y. Mhandi, and A. Mohamed, "Impact of clustering microgrids on their stability and resilience during blackouts," in *Proc. Int. Conf. Smart Grid Clean Energy Technol.,* 2015, pp. 195–200.
[35] M. Saleh, Y. Esa, and A. Mohamed, "Optimal microgrids placement in electric distribution systems using complex network framework," in *Proc. Int. Conf. Renewable Energy Res. Appl.,* San Diego, CA, USA, 2017, pp. 1036–1040.
[36] M. Saleh, Y. Esa, and A. Moahmed, "Effect of wireless communication delay on DC microgrids performance," in *Proc. 10th Annu. IEEE Energy Convers. Congr. Expo.,* Portland, OR, Sep. 23–27, 2018, p. 38.
[37] J. Choi, H. Jeong, J. Choi, D. Won, S. Ahn, and S. Moon, "Voltage control scheme with distributed generation and grid connected converter in a DC microgrid," *Energies*, vol. 7, pp. 6477–6491, 2014.
[38] *IEEE Standard for Interconnecting Distributed Resources With Electric Power Systems*, IEEE Std 1547, Jun. 2003.



Mahmoud Saleh received the M.S. degree from City College of New York, New York, NY, USA, in 2013. He is currently working toward the Ph.D. degree at the Department of Electrical Engineering, City College of New York. His research interests include enhancing grid resilience, microgrid designs, control and automation, analyzing the electric power systems using complex network analysis, and the impact of ICT degradations on the smart grids.

Yusef Esa received the B.S. degree in electrical engineering from City College of New York, New York, NY, USA, in 2015. He is currently working toward the M.S. degree at the Smart Grid Laboratory, City College of New York. His research interests include microgrids design and control, and optimal power flow.

Ahmed Mohamed (GM'09–M'13–SM'17) is an Assistant Professor of electrical engineering, and the Director of the Smart Grid Laboratory, City University of New York, City College, New York, NY, USA. His main research interests include microgrid design and control and electric transportation.