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Additive Laser Metal Deposition onto Silicon for Enhanced Microelectronics Cooling

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***Abstract*—We previously demonstrated how the Sn3Ag4Ti alloy can robustly bond onto silicon via selective laser melting (SLM). By employing this technology, thermal management devices (e.g., micro-channels, vapor chamber evaporators, heat pipes) can be directly printed onto the electronic package (silicon die) without using thermal interface materials. Under immersion two-phase cooling (pool boiling), we compare the performance of three chip cooling methods (conventional heat sink, bare silicon die and additively manufactured metal micro-fins) under high heat flux conditions (100 W/cm^2). Heat transfer simulations show a significant reduction in the chip temperature for the silicon micro-fins. Reduction of the chip operating temperature or increase in clock speed are some of the advantages of this technology, which results from the elimination of thermal interface materials in the electronic package. Performance and reliability aspects of this technology are discussed through experiments and computational models.**

Keywords- Electronic Cooling; Thermal Management; Additive Manufacturing; Laser Metal Deposition; Performance and Reliability.

I. INTRODUCTION

Based on Moore's Law, the trend towards higher computational power in microprocessors, heat fluxes double every ~3.5 years [1]. Current conventional chip level cooling methods that rely on thermal interface materials may simply fail to meet this demand, even with optimization in cooling design [2]–[4]. Moreover, current electricity reduction can also be reduced by better cooling. Every year ~73 billion kWh of electricity is consumed in data centers in the US alone. Reducing the core temperature of microprocessors by 10 °C can improve computational efficiency by over 5%. Furthermore, this temperature reduction would save $450 million per year in electricity, and greatly reduce CO_2 emissions and e-waste.

In conventional microprocessor packages, the silicon die is attached to the lid/heat spreader using a thermal interface material (TIM 1), and the heat spreader is attached to the heat sink via a second TIM (TIM 2) (Figure 1). The TIMs in applications with low heat fluxes are usually thermal pastes, greases, or pads with conductivities up to 10 W/m-K [5]. Even in high-performance applications that utilize high conductivity materials such as indium foils, appreciable temperature drops are observed (thermal resistance of ~0.13 cm^2 -°C/W at ~70 PSI for solid Indalloy®19 with thickness of 76.2 µm) [6]. The thermal resistances of TIMs in the cooling paradigm has become a key issue as the chip heat fluxes move beyond 100 W/cm^2.

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In high-end packages, at least one of the TIMs are replaced with indium foil with thermal conductivity of up to 86 W/m-K [6], [7]. However, indium films have certain limitations such as cost and the die metallizations are deposited by expensive and time-consuming methods such as chemical or physical vapor deposition or sputtering.

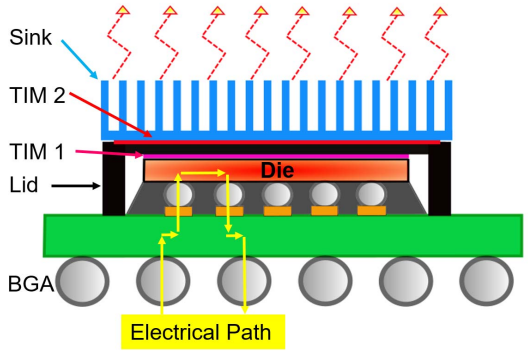

Figure 1 Conventional packaging strategy in microprocessors.

We have recently demonstrated how additive laser metal deposition can be used to bond Sn3Ag4Ti brazing alloy onto a silicon substrate [8], [9]. In this process, a thin layer of metal powder (~20 µm) consisting of Sn3Ag4Ti is deposited onto the backside of a silicon die or wafer and bonded by a laser beam in a protective N_2 gas environment. The temperature of the metal powder being exposed to the laser will reach thousands of degrees Celsius in microseconds and melt the powder. The localized heating will enable the reactive element of the alloy, which in this case is titanium, to overcome the energy barrier of reaction and react with silicon substrate to create a strong silicide bond [8].

It is also possible to print another metal, such as copper or aluminum, onto the Sn3Ag4Ti alloy to take advantage of their higher thermal conductivity [9]. In this case, the alloy acts as an interlayer which bonds both to the silicon substrate via silicide bonding and to the copper via intermetallics. The resolution of this technique is limited by the optics and powder size. Our current printer has an x-y minimum feature of 100 um, but different optics and powders can reduce this further. Various structures such as fins, pillars and lattice structures can be built on top of the interlayer alloy to optimize the fluid flow and heat transfer characteristics. Modulated porosity can be produced by changing the laser power, which is of interest for wick design. These fine features can be used to increase the surface area of a chip for single phase or two phase cooling approaches (*e.g.* pool boiling or impinging jets) [10]–[17].

II. PERFORMANCE CHARACTRIZATION

In order to better understand how this printing technique may yield enhanced thermal performance, three configurations subject to immersion cooling were computationally modeled. The first case is a conventional heat sink with thermal interface materials and heat spreaders (Figure 2). The second case has micro-fins directly manufactured onto the silicon via selective laser melting (Figure 2). The third case is a fully immersed bare chip (Figure 2). ANSYS Fluent 19.2 was used for this study. Mesh independency studies were performed for each case. The boundary conditions are prescribed to mimic realistic conditions. Pool boiling with phase change was represented by using a constant heat transfer coefficient of 15,000 W/m^2-K. The working fluid was assumed to have free stream temperature of 40 °C for all cases. All simulations were performed under steady state conditions. The thermal conductivities used in the simulations are provided in table 1.

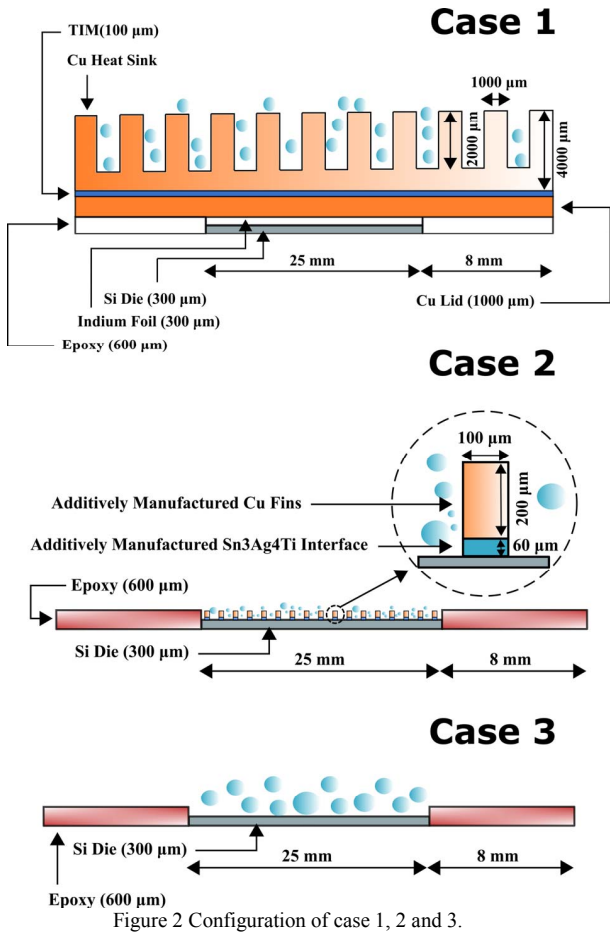

Figure 2 Configuration of case 1, 2 and 3.

Table 1 Thermal conductivity of materials.

	Material	*Thermal conductivity [W/m-K]*	*Reference*
1	Indium (pure)	86	[6]
2	Thermal paste	8.4	[5]
3	Copper (C10400)	384	[18]
4	Sn3Ag4Ti alloy	39.4 (*)	[8]
5	Silicon	148	[19], [20]
6	High conductivity epoxy	0.49	[21]
7	AISI 1018	51.9	[22]

(*) With process improvement, should be able to increase up to 70 W/m-K.

A. *Case 1: Si + Indium + Cu Lid + TIM + Cu Heat Sink*

In this case, a silicon die with a heat flux of 100 W/cm^2 is considered with an area of 25 × 25 mm and a thickness of 300 µm. On top of the die, an indium foil is placed with the same thickness as the silicon die. On top of the indium foil, a copper lid with thickness of 1mm is stacked and afterwards a conventional TIM (100 µm) in the form of thermal paste and finally on top a copper heat sink consisting of fins with 2 mm height and 1 mm spacing is installed (Figure 2) and immersed on the working fluid. The near-junction temperature reached 85.5°C (Figure 3, 4).

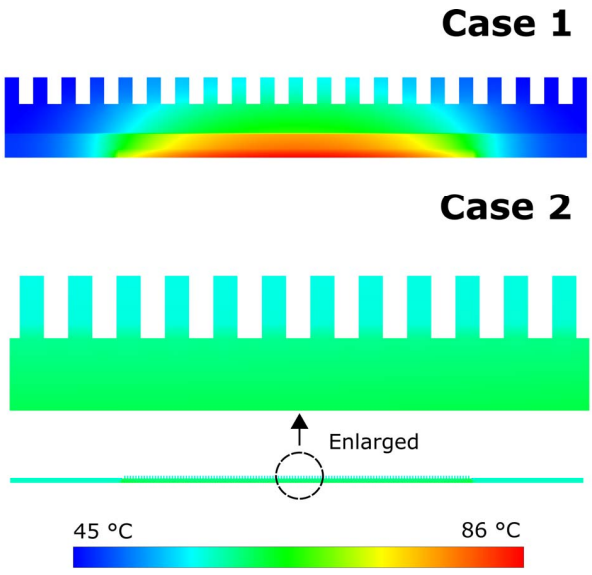

Figure 3 Temperature profile of case 1 and 2.

B. *Case 2: Si + Sn3Ag4Ti Interface + Cu micron sized Fins by Additive Manufacturing (AM)*

The motivation of this research is direct printing of micro-fins on top of the silicon chip. Copper fins with height of 200 µm and width of 100 µm and 100 µm spacing is additively manufactured by laser deposition onto silicon die with heat flux of 100 W/cm^2 with 60 µm of Sn3Ag4Ti as an interfacial alloy (Figure 2) and then immersed for pool boiling, as were the previous scenarios. Near-junction temperature in this case reached 62.4 °C (Figure 3, 4). The predicted decrease in near-junction temperature in the simulation with same boundary conditions as the other cases is due to minimization of interfacial thermal resistances and the large increase of the active surface area for heat transfer by printing micron sized fins.

C. *Case 3: Bare Si*

Two-phase immersion cooling of the bare chip (no heat sink) has been available in the industry for some time [23], [24]. In this case study, a bare silicon die (300 µm) is immersed in working fluid with the same heat flux and heat transfer coefficient as case 1. This configuration takes advantage of minimal conduction thermal resistance as no TIMs are involved. However, the near-junction temperature was estimated as 108.5 °C due to low surface area negating any benefit of no TIM (Figure 4). This number is not physically true as in reality critical heat flux is reached and the assumed heat transfer coefficient is no longer valid.

Based on the simulations we have observed that the additively manufactured fins have higher performance compared to conventional methods of chip thermal management (Figure 4). This technology can be used to either increase the microprocessor performance or save energy by the chip operating at lower junction temperatures.

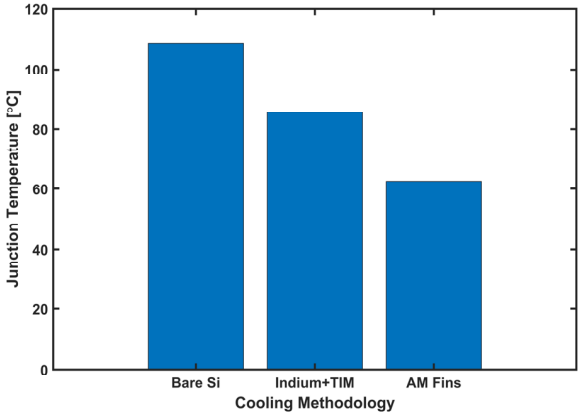

Figure 4 Comparison of near-junction temperature of three configurations with same boundary conditions.

Furthermore, by employing AM fins, the size of the package can significantly decrease due to the removal of heat spreaders and heat sinks, which is important for applications that tightly pack electronics (*eg* future high-density computing servers). For instance, the AM fins printed directly on silicon die (case 2) are 5 mm shorter than the conventional heat sink with TIMs and a heat spreader (case 1) (Figure 5).

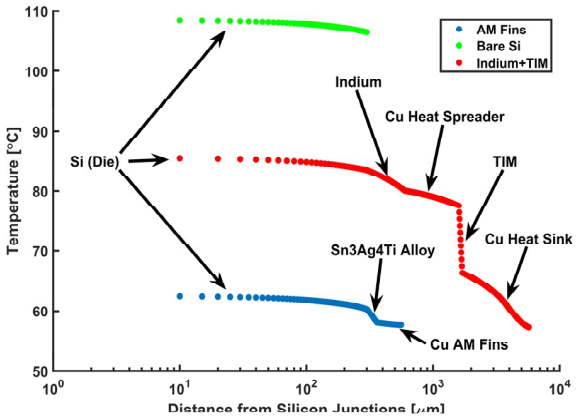

Figure 5 Comparison of different cases in terms of cooling device height.

III. RELIABILITY AND TESTING

The process of selective laser melting heat removal devices onto silicon must not damage the underlying transistors. One reliability concern is how much the transistors will heat up during laser processing. In order to answer this question, two approaches are considered. When the metal powder on the back of the die is exposed to the laser beam, an extremely fast (~µs) and localized (~µm) temperature rise will occur [25]. The amount of heat being absorbed, depends on the optical absorption coefficient of the metal powder at laser wavelength, laser power and scanning rate [26], [27]. A melt pool is created during this process which cools down at the rate of millions of degrees per second. As the heating and cooling process occurs extremely fast, it is not straightforward to measure instantaneous temperature rise accurately. As a result, transient numerical simulation for fast temperature changes and experimental temperature sensing for slower variations of the thermal wave is used.

A. Experimental thermal measurement of die heating during additve laser metal deposition

An experiment was designed in order to evaluate the temperature rise at the transistor side of the Si substrate during the laser deposition of Sn3Ag4Ti alloy. On one side of a 4-inch silicon wafer (553 µm thick) two E Type thermocouples (gauge 36 and PFA insulation from Omega™) were attached using high conductivity thermal grease to ensure fastest and most accurate response during laser processing within the accuracy of the temperature measurement technique (Figure 6, 7) [28]. LabJack U6-Pro with sampling rate of 3.58 ms and effective resolution of 0.6 µV was used for datalogging [29]. The response rate of the thermocouple is slower than 10 ms, as a result, all signals are picked up real-time by the datalogger. Furthermore, the Seebeck voltage of the E type thermocouple in temperatures between 20 °C to 500 °C is 1 mV to 37 mV respectively which provide a strong signal for the datalogger to pick up [30].

The sample is installed on an AISI 1018 steel wafer holder with the thermocouple located at the interface between the wafer holder and Si wafer (Figure 7). A thin layer of powder with ~20 µm thickness was deposited on the silicon wafer and was then exposed twice by the laser beam at a power of 120 W and a scan velocity of 1700 mm/s in skin exposure setting (Figure 8).

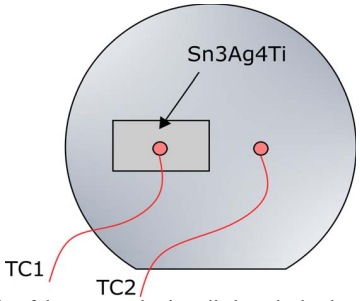

Figure 6 Schematic of thermocouples installed on the back of Si wafer and the footprint of Sn3Ag4Ti surface bring scanned on the other side.

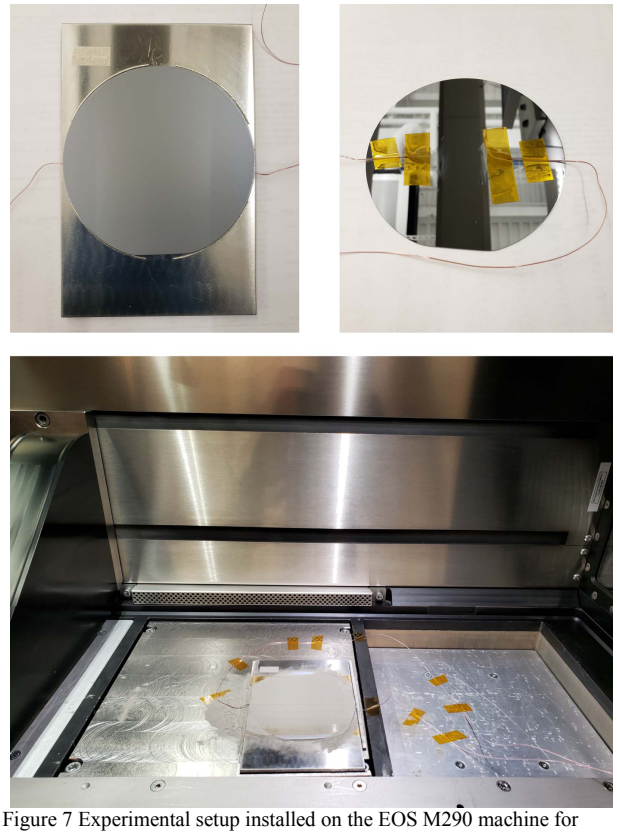

Figure 7 Experimental setup installed on the EOS M290 machine for temperature measurement on the back of silicon wafer.

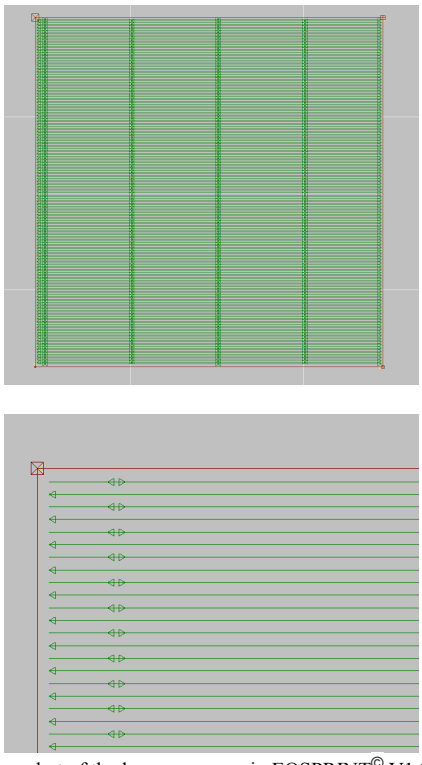

Figure 8 Snapshot of the laser scan map in EOSPRINT© V1.3 software. The laser scan lines are shown as green.

Thermocouple 1 is placed directly under the laser exposure area and thermocouple 2 is installed away from the exposure area (Figure 6). The first and second exposure peaks were detected by thermocouple 1. Substrate heating by conduction were also sensed by thermocouple 2. The maximum temperature rise of 231 °C was recorded on the back of the silicon wafer (Figure 9). This is a worst-case heating, as we printed a large area at one time. By changing the geometry printed from a cube to fins or pillars, the temperature rise will decrease. We can also refine the print path to avoid heat buildup.

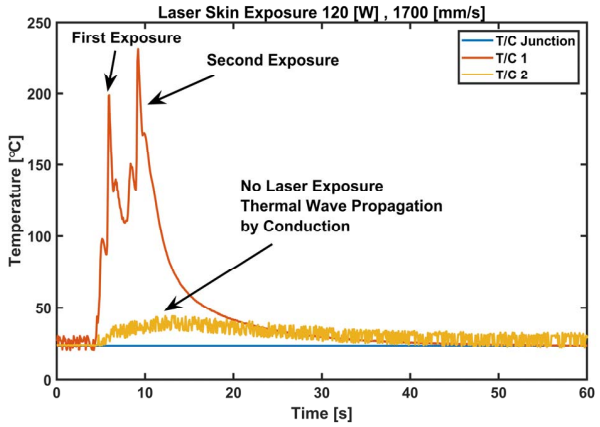

Figure 9 Temperature measurement by thermocouples on the back of silicon wafer during laser processing.

B. Numerical simulation of die heating during additve laser metal deposition

A set of numerical simulations to model the effects of the laser melting on temperature rise through the Si substrate was conducted using ANSYS Fluent 19.2. The computational (solid) zones were set to move at the constant laser velocity of 1700 mm/s through the domain. Constant heat flux at the substrate surface is applied on a fixed area to model the gaussian beam with power of 120 W and diameter of 80 µm at focal plane. Melting in general is a transient problem due to the time dependent physics involved in phase transformation. However, by employing the above methodology, it is possible to treat this problem as steady state and decrease computational requirements without a loss of accuracy.

Three separate zones (solids) are created for this simulation. The first zone is a 20 µm thick Sn3Ag4Ti alloy which represents a single layer of powder deposited on the die surface. The next zone is silicon with 500 µm thickness which is created from the bottom of the previous zone. Finally, the third zone is steel substrate with 500 µm thickness that represents the steel wafer holder which the Si substrate is attached to during the print. The size of the computational domain is 0.5 (x-direction) × 2 (y-direction) ×1.5 (z-direction) mm^3. The mesh is created with a gradient which increases in cell size moving away from the laser spot. After mesh independency study, the size of cells in final mesh at the location of laser spot were 1×1×1 μm^3. Total number of 11,594,880 computational cells are used in this simulation.

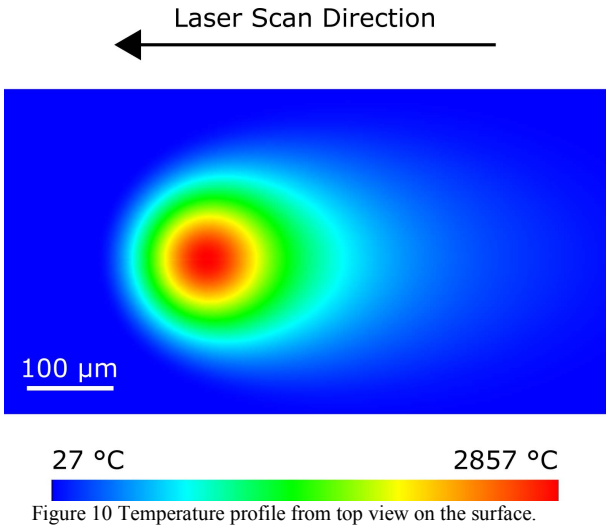

Figure 10 Temperature profile from top view on the surface.

Radiative losses at the surface are also accounted for by Stefan-Boltzmann law for black body radiation. Optical absorptivity and emissivity of the Sn3Ag4Ti alloy is approximated by pure Sn metal which is 0.18 and 0.05, respectively. The maximum temperatures were recorded at depths of 10 µm to 500 µm below the Sn3Ag4Ti-Si interface (Figure 12).

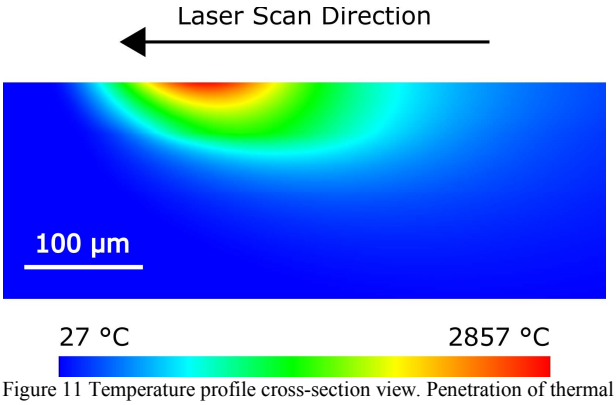

Figure 11 Temperature profile cross-section view. Penetration of thermal wave into the sample can be seen.

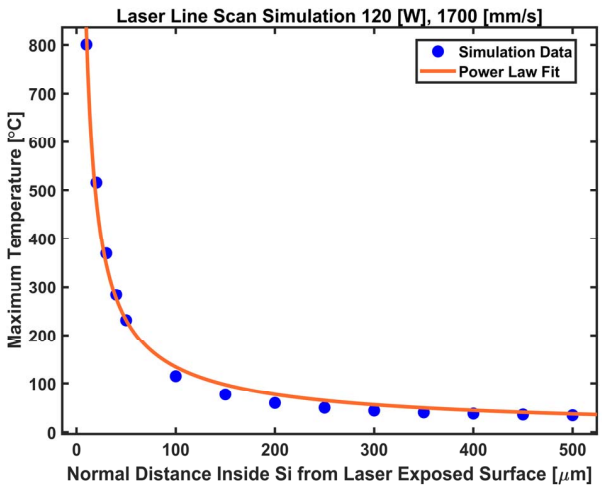

Figure 12 Maximum temperature rise inside Si substrate during additive laser deposition of a single line scan.

Another concern is whether the structure being deposited on the die surface can handle the thermal stresses of laser processing and the temperature fluctuations during computational cycles. Thermal stresses occur due to the large difference in coefficient of thermal expansion (CTE) in materials. Silicon has low CTE as oppose to metals such as copper or aluminum which have at least 5 times bigger CTEs. By using a low melting point interlayer alloy which in this study is Sn3Ag4Ti, which melts at ~250 °C, less thermal stress is imposed to the Sn3Ag4Ti-Si interface during manufacturing and usage. Our previous work thermal cycled a 316L structure built onto silicon with Sn3Ag4Ti as an interlayer. This part was thermal cycled from -40 °C to 130 °C 100 times. Afterwards, the part was visually inspected for signs of delamination or fracture, which was not observed [8].

In the case of additive laser deposition of copper on silicon, at the interface between the Sn3Ag4Ti interlayer alloy and Cu heat sink, intermetallic phases in Sn-Cu couples will form. Intermetallic compounds are phases of precise constituent stoichiometry and are common in lead-free Cu-Sn solders. Cu_6Sn_5 and Cu_3Sn are the primary phases found in isothermal and transient liquid phase bonding. However, in selective laser melting, both the interlayer alloy and copper will melt. Amongst the Cu-Sn intermetallic phases, Cu_3Sn has the most exothermic enthalpy of formation and will thus form first and constitute the main IMC phase at the interface [31]. The exact morphology and properties of Cu_3Sn formed during laser melting has not yet been thoroughly studied. However, Frederikse et al. reported the thermal conductivity of Cu_3Sn to be 70.4 W/m-K.

AUTHOR CONTRIBUTIONS

S.N.S. conceived the initial idea of this research. A.A. developed the processing technique and performed all experimental and numerical characterizations and testing. M.A.D. carried out the FDTR thermal measurement and contributed towards intermetallics section. J.C.S performed laser melting simulations. S.N.S. guided the work. All authors contributed to the writing of this paper.

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