Discrete Time Synchronization Modeling for Active Rectifiers in Wireless Power Transfer Systems

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***Abstract*—Active rectifiers in wireless power transfer systems exhibit many benefits compared to diode rectifiers, including increased efficiency, controllable impedance, and regulation capability. To achieve these benefits, the receivers must synchronize their switching frequency to the transmitter to avoid sub-fundamental beat frequency oscillations. Without additional communication, the receiver must synchronize to locally-sensed signals, such as voltages and currents induced in the power stage by the transmitter. However, the waveforms in the receiver are dependent on both the transmitter and receiver operation, resulting in an internal feedback between sensing and synchronization which prohibits the use of traditional phase-locked-loop design techniques. In this digest, a discrete time state space model is developed and used to derive a small signal model of these interactions for the purpose of designing stable closed-loop synchronization control. A prototype 150 kHz wireless power transfer converter is used to experimentally validate the modeling, showcasing stable synchronization.**

***Index Terms*—wireless power transfer, synchronization, PLL, discrete time**

I. Introduction

Active rectification is capable of providing control and efficiency benefits to WPT systems [1]–[4]. In addition to increasing rectifier efficiency through synchronous switching, on-line adjustment of switching actions can be used to alter the real and reactive components of the rectifier impedance presented to the transmitter, allowing regulation and system maximum efficiency point tracking [1]–[4]. Active rectifiers as wireless power transfer (WPT) receivers have been demonstrated at various WPT frequencies, including 110-205 kHz [1], [5], 6.78 MHz [2]–[4], and 13.56 MHz [6], [7]. These implementations exhibit higher efficiency and greater control capabilities than passive diode rectifiers [1]–[5]. In order to leverage these benefits, active rectifiers must be controlled to synchronize their switching actions to magnetic field, as induced by the transmitter.

Fig. 1 is a simplified diagram of an example WPT system, showing the receiver synchronization control loop. In this system, both the transmitter and receiver hardware consist of a a transistor power stage coupled through a passive impedance matching network (IMN) to a WPT coil. Switching actions in the transmitter power stage may be derived in open loop from a reference transmitter switching frequency, $f_{s,p}$. For proper operation, the receiver must recover this switching frequency, and align its switching actions with a constant phase offset relative to the transmitter. Fig. 1 gives a generic block diagram of the conceptual control needed to accomplish this task. One or more ac signals x_r are sensed from the IMN and phase information ϕ_r is extracted through sensing circuitry H. A phase-locked loop (PLL), or functionally similar circuitry, then aligns the switching actions of the rectifier to the sensed phase information ϕ_r, with regulated offset Φ_{os}.

As discussed in detail later, the PLL circuitry has an internal feedback loop, the design and stability analysis of which is well established [8], [9]. However, in this application, there exists a second feedback loop through the power stage. As the PLL alters the switching signals of the power stage, the switching behavior of the rectifier is changed, in turn altering the power stage operating waveforms and thereby the sensed signal x_r. Any power component signal sensed in the receiver will contain frequency components related to both the transmitter and receiver switching frequency. This inherent feedback, through the power stage and WPT tank, from the PLL output $\phi_{pwm,s}$ to its synchronization reference ϕ_r, must be considered when designing the dynamic behavior of the PLL block itself.

Synchronization has previously been demonstrated in active WPT rectifiers [4], [10]–[15]. An additional optical link is used in [10] to overcome the issue using additional hardware, and requiring line-of-sight between transmitter and receiver. Additional auxiliary coils are used to obtain a synchronization

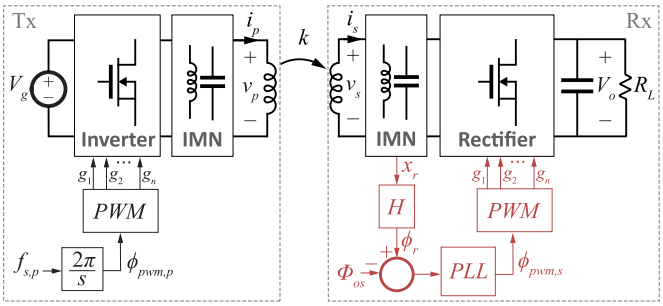

Fig. 1. Simplified WPT system with rectifier synchronization control loop shown in red.

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reference which exhibits high sensitivity to the transmitter field while attenuating feedback from the receiver [11], [12] at the expense of additional hardware. Sensed voltages and currents in the IMN or device currents in the rectifier are used directly to program switching actions, requiring additional filtering or deglitching to overcome noise sensitivity [4], [13], [14]. Previous studies have also used PLLs to align switching actions, though sufficiently conservative bandwidths and phase margins are employed to allow averaged equations to be used in the dynamic modeling [11], [15].

To date, the dynamics of the inherent power stage feedback loop, and their impact on synchronization, have not bee presented in detail. This work seeks to develop a dynamic model of the synchronization loop in WPT systems, to facilitate the design of high-bandwidth control. Using a general analysis and design framework, based on discrete time modeling, the results are applicable to WPT systems at varying frequency, and using varying sensing approaches for synchronization. The modeling is employed to demonstrate synchronization on a prototype 150 kHz, 20 W WPT system, showcasing stable synchronization and dynamic phase control. The remainder of this paper is organized as follows. Section II reviews traditional discrete time modeling, applied to a WPT converter. Section III extends these concepts to model synchronization dynamics. The models are validated experimentally in Secion IV. The work is concluded in Section V.

II. Discrete Time Modeling of WPT System

To examine the dynamics of the WPT synchronization loop, the general dynamics of the converter are first modeled using discrete time, state space modeling techniques [16]–[20]. Because this approach is general for switched systems, the analysis applies without modification to WPT converters regardless of IMN implementation, power stage implementation, or parameter selection. However, for clarity, discussion will reference the example WPT tank implementation of Fig. 2, which uses series-series compensation for the two IMNs. To abstract from the power stage implementation, v_{tx} and v_{rx} are independent inputs to the model, which are assumed to be piecewise-constant voltages. This approach has the additional benefit of resulting in a model which is topologically time-invariant. This approach remains valid so long as there is minimal loss in the transmitter and receiver switching devices, and the input and output dc voltages are constant or quasi-static withing timeframes of interest for the dynamic modeling.

A. Steady-State Model

The system is modeled using its state space description

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t). \tag{1}$$

Example matrices and vectors for the system shown in Fig. 2 are given in (2), where $d^* = L_{tx}L_{rx}(1-k)$ and $M = k\sqrt{L_{tx}L_{rx}}$. Example waveforms are given in Fig. 3 over one complete period of operation in steady state.

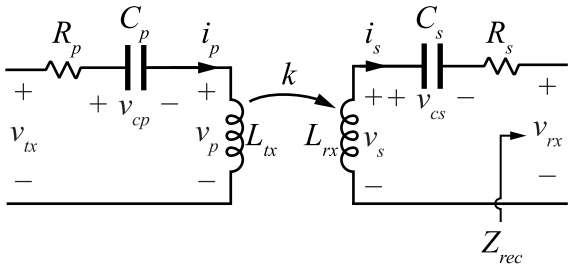


Fig. 2. Modeled WPT system

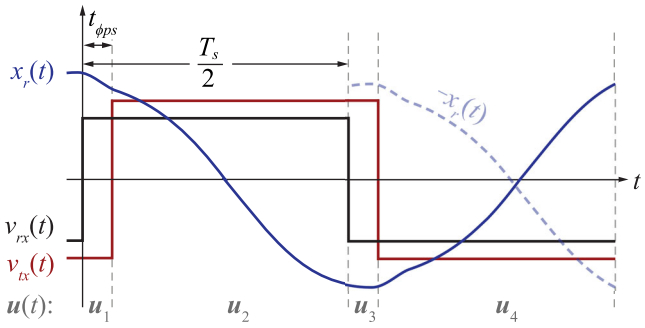


Fig. 3. Example steady state waveforms and discrete time sampling points. The waveform x_r is one state of $\mathbf{x}$, in this case the waveform matches that of $v_{cs}(t)$.

When $\mathbf{A}$ is invertible, (1) has a closed-form solution within any time interval where $\mathbf{u}(t) = [v_{tx}(t) \;\; v_{rx}(t)]^T$ is constant,

$$\mathbf{x}(t) = e^{\mathbf{A}t}\mathbf{x}_0 + \mathbf{A}^{-1}\left(e^{\mathbf{A}t} - \mathbf{I}\right)\mathbf{B}\mathbf{u}_i, \tag{3}$$

which is valid for $t \in [0, \; t_i]$, the duration of an individual interval where $\mathbf{u}(t) = \mathbf{u}_i$, and $\mathbf{x}_0$ is the state vector at the beginning of the interval. Applying (3) recursively across one half period, and noting that all states in $\mathbf{x}(t)$ are anti-symmetric across one half-period [21], the steady-state solution for the state vector at the beginning period is

$$\begin{aligned}\mathbf{X}_{ss} = \left(\mathbf{I} + e^{\mathbf{A}T_s/2}\right)^{-1}\Big[&\mathbf{A}^{-1}\left(e^{\mathbf{A}(T_s/2 - t_{\phi ps})} - \mathbf{I}\right)\mathbf{B}\mathbf{u}_2 \\ &+ e^{\mathbf{A}(T_s/2 - t_{\phi ps})}\mathbf{A}^{-1}\left(e^{\mathbf{A}t_{\phi ps}} - \mathbf{I}\right)\mathbf{B}\mathbf{u}_1\Big].\end{aligned} \tag{4}$$

After finding the discrete steady-state, (3) can be applied numerically produce continuous waveforms of the steady-state operation. For the component values of the experimental prototype given in Table I, and combining with a state space description of the topology described in [5], steady-state operating characteristics are shown in Fig. 4. Note that while the inverter is a traditional full bridge, the rectifier in [5] is a switched capacitor implementation which is operated at a fixed, maximum modulation index in Fig. 4, approximating the behavior of a full bridge followed by a 3:1 step-down dc-dc converter.

Note that the optimal coil-to-coil efficiency is 90.8% and occurs at $Z_{rec} = (8.5 + j0.06)\Omega$ which closely matches the

$$\mathbf{A}=\frac{1}{d^*}\begin{bmatrix}-L_{rx}R_p & -MR_s & -L_{rx} & -M\\ -MR_p & -L_{tx}R_s & -M & -L_{tx}\\ d^*/C_p & 0 & 0 & 0\\ 0 & d^*/C_s & 0 & 0\end{bmatrix}\quad \mathbf{B}=\frac{1}{d^*}\begin{bmatrix}L_{rx} & -M\\ M & -L_{tx}\\ 0 & 0\\ 0 & 0\end{bmatrix},\ \mathbf{x}(t)=\begin{bmatrix}i_p(t)\\ i_s(t)\\ v_{cp}(t)\\ v_{cs}(t)\end{bmatrix}\quad \mathbf{U}(t)=\begin{bmatrix}v_{tx}(t)\\ v_{rx}(t)\end{bmatrix} \tag{2}$$

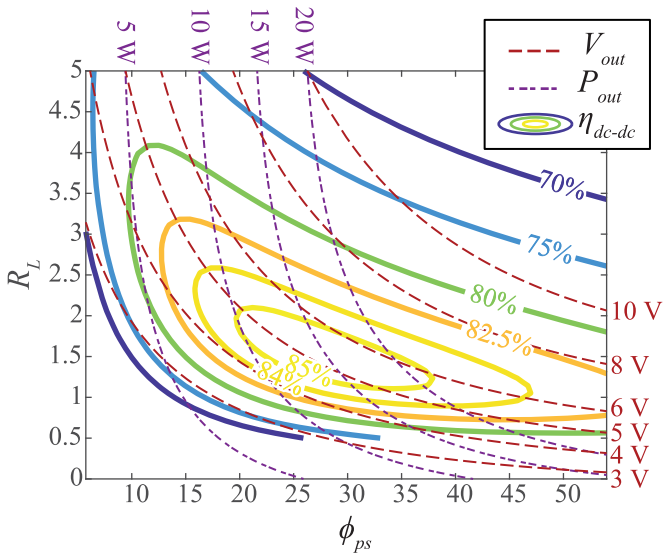


Fig. 4. Steady state output voltage, power, and dc-dc efficiency of the WPT prototype.

well-known optimal load predicted in prior literature, e.g. [22], [23]

$$\eta_{max}=\frac{k^2Q_pQ_s}{\left(1+\sqrt{1+k^2Q_pQ_s}\right)^2} \tag{5}$$

$$Z_{rec,opt}=R_s\sqrt{1+k^2Q_pQ_s}+j\left(\omega_sL_{rx}-\frac{1}{\omega_sC_s}\right), \tag{6}$$

which predict a maximum coil-to-coil efficiency of η_{max} =91.2% at optimal load $Z_{opt}=(8.6+j0.15)\Omega$. These minor differences are a result of the traditional analysis in [22], [23] employing a fundamental harmonic approximation, whereas the model presented here is considers a full range of harmonics. The maximum predicted dc-dc efficiency is 85.6%, which occurs at a load resistance of 1.5 Ω

B. Small-Signal Dynamic Model

To examine the stability of the synchronization loop, a model for the dynamic behavior in the sensed phase ϕ_r (in Fig. 1) as a result of perturbations to the rectifier switching actions is needed. In this section, a more traditional discrete time, small-signal model of the response of circuit signals (voltages or currents) to perturbations in rectifier phase is developed based on established modeling techniques [16]–[20]. This model is then extended in Section III-B to model the phase of a sensed synchronization signal.

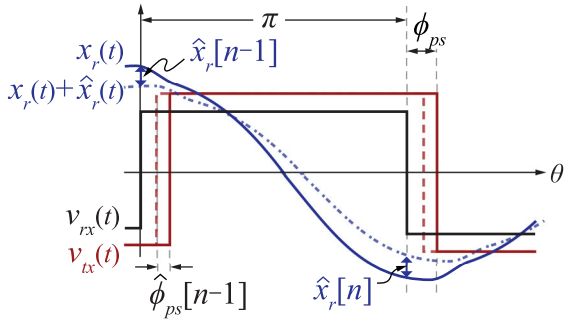


Fig. 5. Example waveforms showing system response to a pertubation in ϕ_{ps}. Waveforms are shown with respect to $\theta=t(2\pi/T_s)$

Traditional discrete time modeling is used to develop a small signal model of the form

$$\hat{\mathbf{x}}[n]=\mathbf{F}\hat{\mathbf{x}}[n-1]+\mathbf{\Gamma}\hat{\phi}_{ps}[n-1], \tag{7}$$

where $\hat{x}[n]$ is the system's small-signal response to control perturbation $\hat{\phi_{ps}}[n-1]$. Again exploiting half-period symmetry, the model is derived using a sampling frequency of $T_s/2$. Example waveforms showing a single state $x_r(t)\in\mathbf{x}(t)$ are given in Fig. 5.

The forced and natural response matrices are

$$\mathbf{F}=-e^{\mathbf{A}T_s/2}, \tag{8}$$

$$\mathbf{\Gamma}=e^{\mathbf{A}(T_s/2-t_{\phi ps})}\mathbf{B}(\mathbf{u}_1-\mathbf{u}_2)\frac{T_s}{2\pi}, \tag{9}$$

where $\phi_{ps}[n]=t_{\phi ps}[n]\frac{2\pi}{T_s}$. The transfer function from $\hat{\phi}[n-1]$ to $\hat{\mathbf{x}}[n]$ is then

$$G_{x\phi}=(z\mathbf{I}-\mathbf{F})^{-1}\mathbf{\Gamma}. \tag{10}$$

Although for the purposes of synchronization, the transmitter is assumed to be operating in open loop without perturbation, because (7) has the phase difference between the transmitter and receiver ϕ_{ps} as an input, it can equally model perturbations occurring at either the transmitter or receiver side switching signals. The discrete time model is time-aligned to the receiver switching actions, therefore the waveforms of Fig. 5 are identical whether the perturbation occurs because the rectifier has a lagging phase perturbation, or the transmitter has a leading perturbation.

Prior to further development of the synchronization model, (7)-(9) are verified by comparing to experimental step response in the prototype system detailed in Section IV (with C_s = 175 nF). Fig. 6 and Fig. 7 show oscilloscope waveforms and overlaid discrete time model switching instance predictions, following a step change in phase of 0.2% of T_s, or about

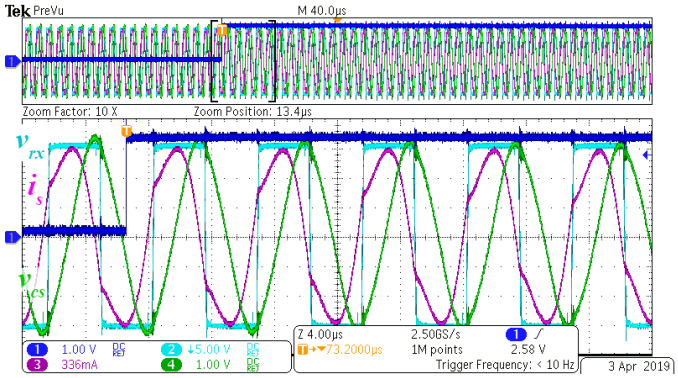


Fig. 6. Oscilloscope waveforms of the experimental step response.

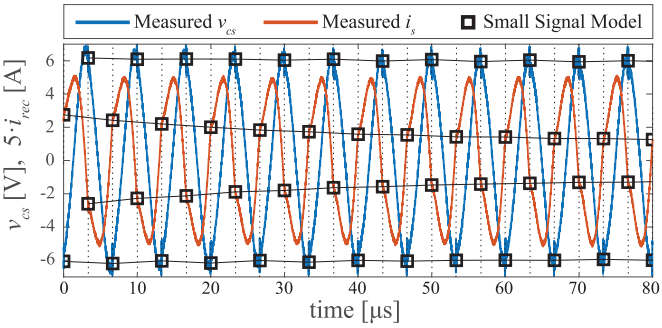


Fig. 7. Measured experimental waveforms (blue lines) with overlaid discrete time predictions (black squares), following a step in rectifier phase. Thin black line added between discrete time model samples to emphasize dynamics.

0.013 radians. The blue lines in Fig. 7 are data-points taken from the same oscilloscope capture shown in Fig. 6. In the discrete time model, the steady-state solution is re-introduced and every-other sample is negated to remove the half-wave anti-symmetry so that the points visually align. The good correspondence in Fig. 7 demonstrates the accuracy of the model.

III. Synchronization Model

In order to expand the dynamic modeling of the previous section to the synchronization loop, both the dynamics of the PLL itself and the power stage waveform phase dynamics are modeled. The general approach, as shown in Fig. 1, is to sense some signal x_r and extract phase information ϕ_r from it. In the 150 kHz system under study in this work, and moreso in 6.78 MHz and above WPT systems, cost and complexity may prohibit the use of full-waveform analog-to-digital conversion with sufficient resolution to implement an analog PLL. Instead, phase information is commonly extracted through a zero-crossing detector (ZCD) from one of the ac-only waveforms in the IMN.

Prior work in [13] attempted to use i_s, sensed through a current transformer, for synchronization. In many designs, high efficiency operation of the rectifier requires operation which results in a rectifier impedance Z_{rec} which is nearly resistive. In a traditional two-level rectifier, this will place the switching actions concurrent with the zero-crossings of i_s, indicating that the current sensor will require significant noise immunity with respect to common-mode voltage transients. Additional sensing coils [11], [12] eliminate this issue and can be designed to exhibit minimal interference from $v_{Rx}(t)$, but may be difficult to implement in space-constrained mobile electronics or when employing a commercial receiver coil. Applying ZCD to the series capacitor voltage, $v_{cs}(t)$, as has been demonstrated in [14], increases immunity to switching noise, as under resistive loading the zero-crossings of $v_{cs}(t)$ are 90° separated from the switching commutation.

A. PLL Modeling

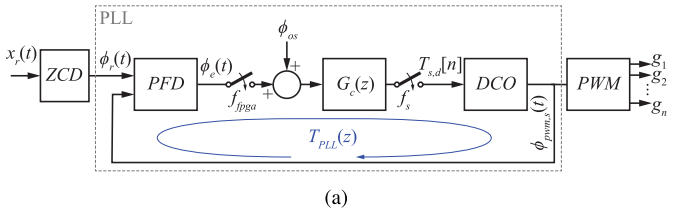
Regardless of the sensed signal, an expanded block diagram of the synchronization hardware shown in Fig. 1 is given in Fig. 8(a), assuming an all-digital FPGA-based implementation. The sensed signal x_r is passed through a ZCD to obtain a binary phase reference signal ϕ_r. This signal is then compared to the PLL output using an phase-frequency detector (PFD) to generate an output signal ϕ_e whose average value over one switching period is proportional to the phase error between the PLL output and the sensed signal. Any desired control offset ϕ_{os} is added to ϕ_e to control the phase alignment of the rectifier operation; if $v_{cs}(t)$ is sensed, a phase shift of 90° is required to obtain resistive loading. A digital compensator $G_c(z)$, operating at the FPGA clock frequency, is used to drive the error between the sensed phase and the offset ϕ_{os} to zero, while stabilizing the feedback loop. The output of $G_c(z)$ is used to adjust the frequency of an oscillator which drives the PLL output. In traditional implementations, a voltage-controlled oscillator (VCO) is used with linear gain from the input signal to the output frequency. In digital implementations, a digitally-controlled oscillator (DCO) may be more suitable, implemented as a clocked counter whose maximal value T_s, d is set by the compensator output. Because switching signals will be directly derived from the output of the DCO, a lockout circuit, such as a sample-and-hold aligned to the end of the period, may be required to prevent additional switching actions in the rectifier. Circuit implementations used in this work for the ZCD and PFD are shown in Fig. 9.

A small signal model of the PLL is shown in Fig. 8(b). The two samplers are neglected under the assumption that the bandwidth of the loop gain $T_{PLL}(z)$ is well below f_s, and $f_{fpga} \gg f_s$. Note that the model in Fig. 8(b) begins with ϕ_r as its input; the nonlinear behavior of the ZCD will be absorbed into the power stage modeling detailed in the following section.

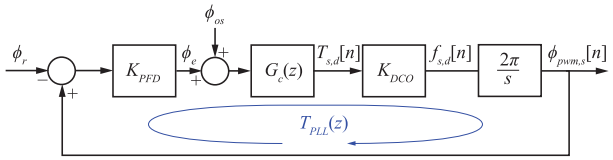
As long as the PLL is nearly in-lock, the PFD has gain

$$K_{PFD} = \frac{1}{2\pi}, \tag{11}$$

which is the gain from the input phase difference (in radians) to the output digital value, averaged over one period. High frequency dynamics, or behavior when out-of-lock have more complicated nonlinear behavior [24], which will be neglected here under the same assumption regarding the bandwidth of $T_{PLL}(z)$ and neglecting initial synchronization during startup.

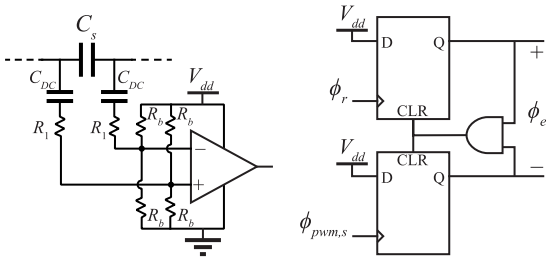


(a)



(b)

Fig. 8. Block diagram of the physical PLL loop (a) and its small-signal model (b)



(a) (b)

Fig. 9. Schematic diagrams of circuits used for (a) ZCD and (b) PFD

The gain of the DCO is

$$K_{DCO} = \frac{-{f_s}^2}{f_{fpga}}, \tag{12}$$

which is operating-point dependent, due to the presence of the steady-state frequency f_s. Additionally, K_{DCO} is negative, which must be accounted for in the overall loop gain. One approach to doing so is to configure PFD inputs as shown in Fig. 9(b), which results in the model as shown in Fig. 8(b) wherein the feedback of $\phi_{pwm,s}$ is summed with positive polarity at the input.

Following the DCO, the gain of $2\pi/s$ represents the conversion from DCO output frequency to instantaneous phase of the output signal, in radians. The presence of integral dynamics in the loop, in addition to the presupposition of integral low-frequency behavior in $G_c(z)$ to achieve zero steady-state error, requires that $G_c(z)$ introduce phase lead in the vicinity of the crossover frequency of $T_{PLL}(z)$ for stability. However, with the present model, the loop can be stabilized with arbitrary bandwidth, subject only to limitations from the averaged model of K_{PFD} and the sampling behavior of the DCO. As is shown next, the bandwidth is additionally limited by the outer-loop dynamics of the power stage.

B. Converter Phase Dynamics

The analysis of the previous section considered the PLL in isolation, having an open-loop independent input ϕ_r. In the WPT converter application, ϕ_r is sensed from power stage signal x_r, which, as detailed in Section II, is determined by both the transmitter and receiver switching actions. The result is a modification of the synchronization loop shown in Fig. 10.

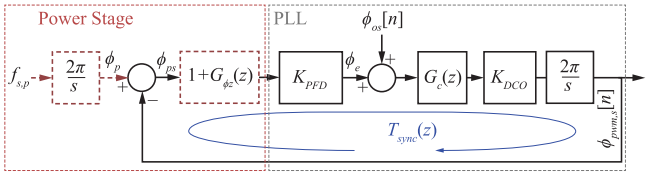


Fig. 10. Block diagram of the PLL loop including power stage dynamics.

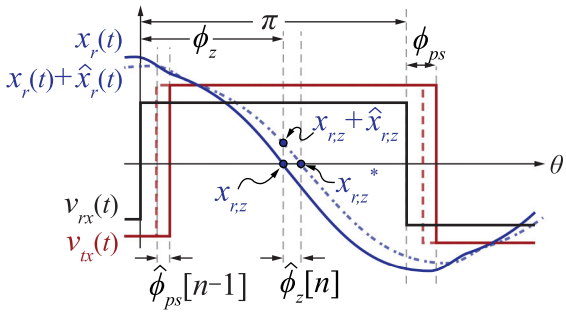


Fig. 11. Example waveforms showing converter ZCD output response to a perturbation in ϕ_{ps}

The presence of the converter results in an additional term in the synchronization loop, $G_{\phi z}(z)$ which is the result of feedback from $\phi_{pwm,s}$, through the power stage, to ϕ_r.

Fig. 11 shows example converter waveforms under the same perturbation to ϕ_{ps} that was previously considered, but now highlighting how the zero-crossing of x_r is altered. Because the zero-crossing moment is generally asynchronous to the discrete time model previously developed, x_z is used to represent the value of $x_r(t)$ at the point where it crosses zero. While $x_r[n]$ was the discrete value of $x_r(t)$ synchronous with the rectifier switching actions, $x_{r,z}[n]$ is its value at time $t_z = \phi_z T_s/2\pi$. In steady-state, $x_{r,z} = 0$. However, after perturbation to ϕ_{ps}, $x_{r,z}(t_z) = x_{r,z} + \hat{x}_{r,z}$. The objective of this analysis is to then find (or approximate) the location of the new zero-crossing $x_{r,z}{}^*$ in order to determine the change in the phase detected by the ZCD, $\hat{\phi}_z = \hat{\phi}_r$.

The discrete time modeling of Section II is extended to derive this transfer function as follows. The discrete time formulation of (7)-(9) gives the small-signal states at the beginning of the half-period. These states are then propagated through the same system dynamics to obtain the states at time t_z,

$$\hat{\mathbf{x}}_z[n] = \mathbf{H}\hat{\mathbf{x}}[n-1] + \mathbf{J}\hat{\phi}_{ps}[n-1], \tag{13}$$

where

$$\mathbf{H} = -e^{\mathbf{A}t_z},$$

$$\mathbf{J} = e^{\mathbf{A}(t_z - t_{\phi ps})}\mathbf{B}(\mathbf{u}_1 - \mathbf{u}_2)\frac{T_s}{2\pi}.$$

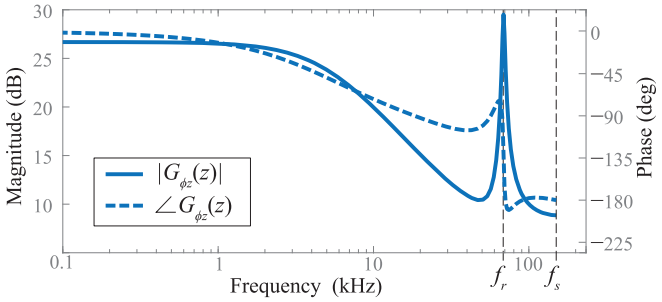


Fig. 12. Bode plot of $G_{\phi z}$

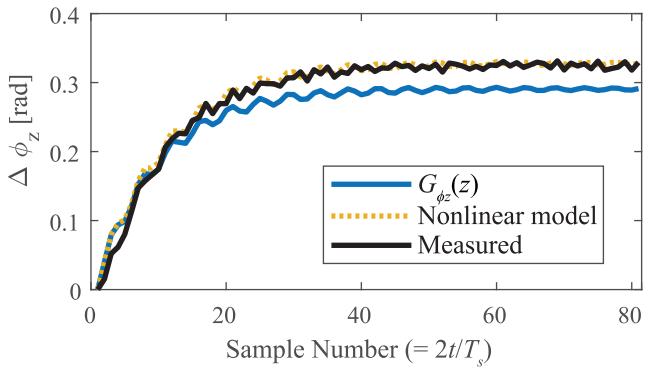


Fig. 13. Experimental change in ϕ_z vs. the predictions of of $G_{\phi z}$ and the nonlinear model

$\hat{x}_{r,z}[n]$ is then be extracted from $\hat{\mathbf{x}}_z[n]$ by use of

$$\hat{x}_{r,z}[n] = \mathbf{C}\hat{\mathbf{x}_z}[n]. \tag{14}$$

In the case of $x_r = v_{cs}$, and for the state space description in (2), $\mathbf{C} = [0\ 0\ 0\ 1]^T$.

As long as small signal assumptions apply, and t_z does not coincide with any switching action, the new zero-crossing point is approximated as a linear projection of $\hat{x}_{r,z}[n]$ using the waveform slope at time t_z

$$\hat{\phi}_z[n] = \frac{\hat{x}_{r,z}[n]}{\dot{x}_{r,z}[n]}\frac{2\pi}{T_s}, \tag{15}$$

where

$$\dot{x}_{r,z}[n] = \mathbf{C}\left[\mathbf{A}\left(x_z + \hat{x}_z[n]\right) + \mathbf{B}\mathbf{u}_2\right], \tag{16}$$

which results in a nonlinear model due to the division of signals in (15). In order to obtain a transfer function, (15) is approximated by replacing $\dot{x}_{r,z}[n]$ with its steady-state value, $\dot{X}_{r,z}[n]$. With this approximation, the complete transfer function is

$$G_{\phi z}(z) = \frac{\hat{\phi}_z}{\hat{\phi}_{ps}} = \mathbf{C}\left[\mathbf{H}(z\mathbf{I} - \mathbf{F})^{-1}\mathbf{\Gamma} + \mathbf{J}\right]\frac{2\pi}{T_s\dot{X}_{r,z}}. \tag{17}$$

A bode plot of $G_{\phi z}(z)$ for the component values given in Table I (with $C_s = 175$ nF) is given in Fig. 12. Note that there is a high-Q resonance at $f_r = 69$ kHz.

This transfer function is validated using the same experimental measurements of an open-loop step response to ϕ_{ps} shown in Fig. 6 and Fig. 7. The oscilloscope measurements are imported into MATLAB to find the phase $\phi_z[n]$ in each half period following the step in ϕ_{ps}. The measurements are compared to both (17) and an iterative numerical evaluation of the nonlinear system without replacing $\dot{x}_{r,z}[n] \approx \dot{X}_{r,z}[n]$. The results are shown in Fig. 13. Note that in addition to the low-frequency dynamics, the measured and modeled waveforms show oscillations with a period of nearly five samples, which corresponds to a frequency of $f_r \approx {}^2/_{5T_s} = 60$ kHz, as predicted in Fig. 12.

IV. Experimental Validation

A prototype, 150 kHz, 20 W WPT converter is used to validate the proposed modeling. The converter uses a full-bridge transmitter and multilevel switched capacitor rectifer (MSC) with 3-levels [5]. The MSC is operated at maximum modulation index such that v_{rx} is a two-level squarewave with amplitude $3V_o$. Prototype components are listed in Table II and parameter values are given in Table I.

TABLE I
Prototype Circuit Parameters

Parameter	Value	Parameter	Value
f_s	150 kHz	V_g	15 V
P_o	20 W	V_o	0-5 V
		k	0.5
L_{tx}	10.75 μH	L_{rx}	12.1 μH
C_p	235 nF	C_s	175 nF / 95 nF
R_p	155 mΩ	R_s	390 mΩ

TABLE II
Prototype Circuit Components

Component	Part
MOSFETs	BSZ0910ND
L_{tx}	Wurth 760308141
L_{rx}	Abracon AWCCA-26R26H08-C01-B
FPGAs	DE-0 Nano, Clyclone IV
ZCD comparator	LTC6752

The transmitter and receiver are controlled by two separate FPGAs with no direct communication between them. The transmitter operates in open-loop, generating 150 kHz switching signals for the full bridge. If the rectifier FPGA is programmed with identical clocking structure, the phase between the rectifier and transmitter switching signals is observed to roll continuously with a beat frequency of a few Hz. Despite using identical controller hardware, synchronization cannot be achieved in open loop without communication.

The PFD, DCO, PWM, and $G_c(z)$ are implemented in the FPGA. The PFD is implemented using combinational logic, the DCO has clock frequency 150 MHz, and $G_c(z)$ has clock frequency 20 MHz, reduced from 150 MHz to ensure timing constraints. A lockout circuit feeds the output of $G_c(z)$ into

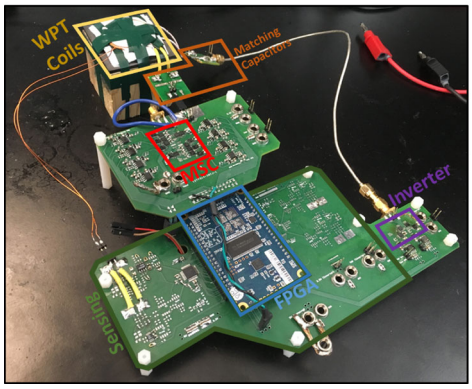


Fig. 14. Experimental WPT converter prototype

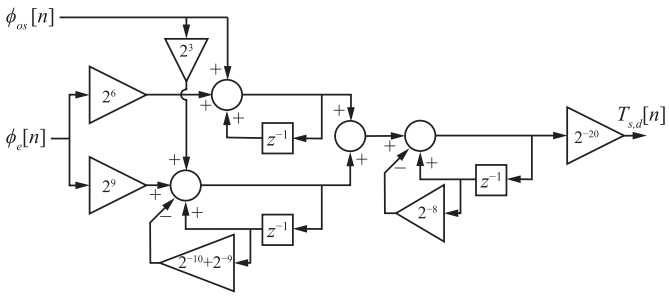


Fig. 15. Block diagram of $G_c(z)$, as implemented in the FPGA

the PWM modulator once per switching period, while also handling data transfer between clock domains. Based on the complete model of Fig. 10, the compensator is designed as shown in Fig. 15. The compensator additionally has saturation of the output period between 135 kHz and 165 kHz, and anti-windup feedback; the saturation is not operating in any of the transient test results shown in this work.

Transfer function $G_c(z)$ for this compensator, along with $G_{v\phi}(z)$ for 15 V input, 15 W output with 1.5 Ω load and the resulting loop gains $T_{PLL}(z)$ and $T_{sync}(z)$ are shown in Fig. 16, for operation with $C_s = 95$ nF. Note that, with this capacitance, $G_{v\phi}(z)$ now exhibits resonances at both 35 kHz and 57 kHz. The compensator design results in a synchronization loop crossover frequency of $f_c = 1.1$ kHz with phase margin 37° at this operating point.

The synchronization loop is able to achieve stable synchronization from $V_g = 1$ V and $P_{in} = 10$ mW to full voltage and power. The measured dc-to-dc efficiency at $V_o = 5$ V, $V_g = 16$ V, $R_L = 1.5$ Ω is 82%. Fig. 17 gives measured waveforms for the converter operating with $V_g = 5$ V, $R_L = 1.5$ Ω, and a recurring step transient between a reference phase offset of $\phi_{os} = 84°$ and $\phi_{os} = 112°$. The transient is stable and well-behaved with dynamics matching those predicted by the modeled transfer functions in Fig. 16. In steady-state, the synchronization loop continuously alters the digital value of the DCO period $T_{s,d}[n]$ by ±1 bit to maintain synchronization. Fig. 18 shows the value of $T_{s,d}[n]$ over 500 periods of operation in steady-state. Because the

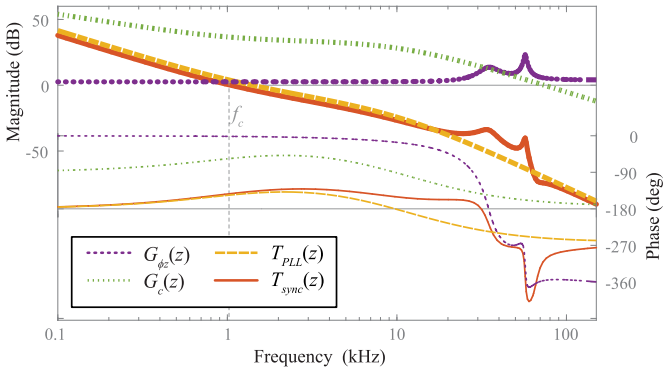
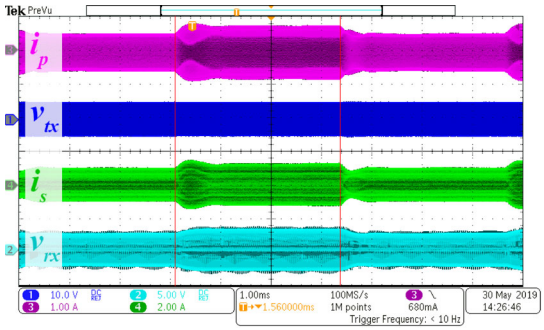
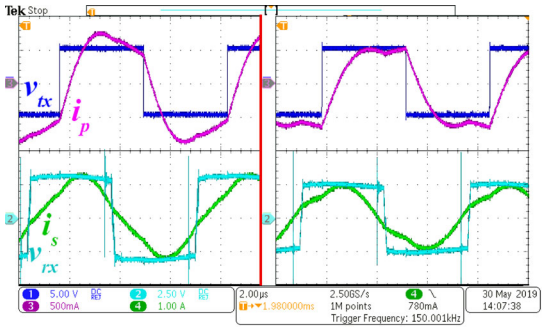


Fig. 16. Transfer functions and loop gain of implemented synchronization control loop. Thicker lines are magnitude, and thinner lines are phase.



(a)



(b)

Fig. 17. Measured waveforms during a repeating transient between $\phi_{os} = 84°$ and $\phi_{os} = 112°$ (a) and zoomed-in waveforms of steady-state operation with $\phi_{os} = 84°$ (left) and $\phi_{os} = 112°$ (right)

system is designed with $f_s = 150$ kHz and $f_{fpga} = 150$ MHz, $T_{s,d} \approx 1000$, with small differences to account for minor discrepancies between the transmitter-side f_s and the actual f_{fpga}.

V. Conclusion

Synchronization is required in order to leverage the benefits of active rectifiers in WPT systems, including increased efficiency, impedance regulation, and output regulation. Because the transmitter and receiver are isolated in WPT applications, synchronization must be accomplished with respect to locally-sensed signals in the receiver power stage. This paradigm results in an inherent feedback loop which impacts the design

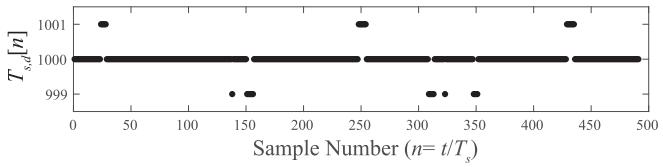


Fig. 18. Experimental values for $T_{s,d}[n]$ over 500 periods of steady-state operation.

of the synchronizing control loop. As synchronization modifies the rectifier switching signals, all voltages and currents in the power stage are modified, thereby altering the sensed reference signal. This work analyzes the dynamics of this feedback, and uses the developed model to design and implement a stable synchronization loop in a 150 kHz, 20 W WPT converter designed for consumer electronics applications. The technique developed requires only modest additional hardware and is therefore suitable for integration. Results demonstrate that robust and stable synchronization can be achieved so long as the power stage dynamics are sufficiently attenuated.

Future work will leverage this synchronization control to provide dynamic impedance tuning for the active rectifier. As implemented, the loop directly controls the phase between the capacitor voltage and rectifier voltage. This is approximately a fixed 90° different from the phase between rectifier current and voltage, resulting in near-direct regulation of the rectifier impedance, which can be used to dynamically tune the WPT converter for optimal system efficiency.

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REFERENCES

[1] A. Berger, M. Agostinelli, S. Vesti, J. A. Oliver, J. A. Cobos, and M. Huemer, "A wireless charging system applying phase-shift and amplitude control to maximize efficiency and extractable power," *IEEE Transactions on Power Electronics*, vol. 30, no. 11, pp. 6338–6348, Nov 2015.

[2] S. Cochran, F. Quaiyum, A. Fathy, D. Costinett, and S. Yang, "A GaN-based synchronous rectifier for WPT receivers with reduced THD," in *2016 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer (WoW)*, Oct 2016, pp. 81–87.

[3] S. Cochran and D. Costinett, "Modeling a 6.78 MHz synchronous WPT rectifier with reduced THD," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2017, pp. 1–8.

[4] E. Ozalevli, N. Femia, G. D. Capua, R. Subramonian, D. Du, J. Sankman, and M. E. Markhi, "A cost-effective adaptive rectifier for low power loosely coupled wireless power transfer systems," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 7, pp. 2318–2329, July 2018.

[5] C. Zhao, D. Costinett, and S. Yang, "A seven-level switched capacitor ac-dc rectifier for fast wireless charging," in *2018 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer (Wow)*, June 2018, pp. 1–6.

[6] Y. Sun, C. jin Jeong, S. kyun Han, and S. gug Lee, "A high speed comparator based active rectifier for wireless power transfer systems," in *2011 IEEE MTT-S International Microwave Workshop Series on Intelligent Radio for Future Personal Terminals*, Aug 2011, pp. 1–2.

[7] C. Huang, T. Kawajiri, and H. Ishikuro, "A near-optimum 13.56 mhz cmos active rectifier with circuit-delay real-time calibrations for high-current biomedical implants," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 8, pp. 1797–1809, Aug 2016.

[8] F. Gardner, "Charge-pump phase-lock loops," *IEEE Transactions on Communications*, vol. 28, no. 11, pp. 1849–1858, November 1980.

[9] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Dynamics assessment of advanced single-phase PLL structures," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 6, pp. 2167–2177, June 2013.

[10] R. Zhao, D. T. Gladwin, and D. A. Stone, "Phase shift control based maximum efficiency point tracking in resonant wireless power system and its realization," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Oct 2016, pp. 4541–4546.

[11] R. Mai, Y. Liu, Y. Li, P. Yue, G. Cao, and Z. He, "An active-rectifier-based maximum efficiency tracking method using an additional measurement coil for wireless power transfer," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 716–728, Jan 2018.

[12] D. J. Thrimawithana, U. K. Madawala, and M. Neath, "A synchronization technique for bidirectional IPT systems," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 1, pp. 301–309, Jan 2013.

[13] S. Cochran and D. Costinett, "Frequency synchronization and control for a 6.78 MHz WPT active rectifier," in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2018, pp. 1–7.

[14] X. Liu, N. Jin, X. Yang, T. Wang, K. Hashmi, and H. Tang, "A novel synchronization technique for wireless power transfer systems," *Electronics*, vol. 7, no. 11, 2018. [Online]. Available: http://www.mdpi.com/2079-9292/7/11/319

[15] Y. Tang, Y. Chen, U. K. Madawala, D. J. Thrimawithana, and H. Ma, "A new controller for bidirectional wireless power transfer systems," *IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 9076–9087, Oct 2018.

[16] D. Costinett, R. Zane, and D. Maksimović, "Discrete-time small-signal modeling of a 1 MHz efficiency-optimized dual active bridge converter with varying load," in *2012 IEEE 13th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2012, pp. 1–7.

[17] D. Maksimovic and R. Zane, "Small-signal discrete-time modeling of digitally controlled PWM converters," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2552 –2556, nov. 2007.

[18] A. R. Brown and R. D. Middlebrook, "Sampled-data modeling of switching regulators," *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, p. 349 –369, 1984.

[19] D. J. Packard, "Discrete modeling and analysis of switching regulators," Ph.D. dissertation, California Institute of Technology, Nov. 1976.

[20] G. C. Verghese, M. E. Elbuluk, and J. G. Kassakian, "A general approach to sampled-data modeling for power electronic circuits," *IEEE Trans. Power Electron.*, vol. PE-1, no. 2, pp. 76 –89, april 1986.

[21] D. Costinett, R. Zane, and D. Maksimovic, "Discrete time modeling of output disturbances in the dual active bridge converter," in *Proc. Appl. Power Electron. Conf. (APEC)*, March 2014, pp. 1171–1177.

[22] W. X. Zhong and S. Y. R. Hui, "Maximum energy efficiency tracking for wireless power transfer systems," *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 4025–4034, July 2015.

[23] M. Fu, H. Yin, X. Zhu, and C. Ma, "Analysis and tracking of optimal load in wireless power transfer systems," *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3952–3963, July 2015.

[24] R. Y. Chen and Z. Yang, "Modeling the high-frequency degradation of phase/frequency detectors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 5, pp. 394–398, May 2010.