Proposal and Realization of Vertical GaN Nanowire Static Induction Transistor

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***Abstract*— Vertical gallium nitride (GaN) nanowire static induction transistors (SITs) are proposed and realized for micro display for the first time. A top-down dry etch was employed to form the GaN nanowires with height of ~1.5 μm and diameter of ~350 nm, followed by the SIT fabrication with the gate-all-around design which benefits are better gate control, combined with reduced surface area consumption for improved scaling and integration. Relatively low voltages are required for controlling the vertical current from source to drain. The I_{on} to I_{off} ratio is measured as 2×10^6, which is ~900 times larger than the previous reported GaN fin SIT. These results demonstrated that vertical nanowire SITs by the use of undoped GaN which is typically the template layer for light-emitting diodes (LEDs) will enable voltage-controlled components for new integration schemes and opportunities in micro display technology.**

***Index Terms*— GaN, static induction transistor, Schottky gate, nanowires, vertical devices.**

I. Introduction

GALLIUM Nitride based semiconductors are emerging materials for power electronics and light-emitting diodes (LEDs). The development of high-efficiency LEDs and micro-LEDs (μLEDs) are opening doors for a number of important applications such as backlight for liquid crystal display [1], visible light communication with light modulation up to several hundred MHz [2], [3], as well as display system for Augmented Reality (AR) and Virtual Reality (VR) technologies [4], [5]. To enable those novel applications, voltage-controlled μLEDs [6]–[8] are highly desirable for simplified control loop and flexible driver circuit design compared to Si-CMOS controlled LEDs [9]. Therefore, there is a strong motivation on exploring potential promising electronic candidates based on the same material system that can be integrated with such μLEDs to achieve voltage-controlled component.

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To fulfill this goal, AlGaN/GaN High Electron Mobility Transistors (HEMTs) have been investigated to be laterally integrated with InGaN/GaN LEDs due to low on-resistance and faster switching speed [6], [7]. However, there are several key challenges with the HEMT-LED lateral integration: 1) most of the integration schemes require complex growth techniques such as selective epi removal or selective area growth [6], [7] which often lead to leakage through the shared GaN buffer layer; 2) the lateral configuration leads to interconnect parasitics; and 3) scaling and heat dissipation are limited. To solve these issues, GaN-based vertical transistors will be of great interest to investigate.

A transistor, which fits into these fabrication requirements, is the Static Induction Transistor (SIT). The SIT is a vertical power device which was invented in the 1970s and utilized in Si, SiC, and GaAs materials [10], [11]. GaN fin SIT has been realized recently through self-aligned process [12]. The SIT can be compared to a Metal Semiconductor Field Effect Transistor (MESFET), though with important differences. In an SIT the structure of the gate is very small and does not extend close to the source or drain, as is typical in a MESFET. Additionally, current flows vertically in an SIT with no need for a semi-insulting layer commonly used in MESFETs. Due to the short gate length, punch through occurs in the device to produce triode-like curves, in contrast to pentode-like curves of a MESFET.

The SIT is a normally 'on' device similar to the HEMTs investigated for use with LEDs [6], [7]. In the SIT the gate forms a depletion region, with the gate bias modulating the depletion width. Correspondingly, a reverse bias extends the depletion region pinching-off the current flow. Conversely, applying a forward bias to the gate shrinks the depletion region increasing current flow. As the drain to source bias increases, the current can punch-through the pinched-off depletion regions caused by the gate, this allows current to flow again. In order to stem the punch-through current the gate must be further reverse biased [12].

In this letter, vertical nanowire structures are chosen to fabricate the SIT due to the gate-all-around benefits for better control, combined with reduced surface area consumption for improved scaling and integration. The nanowire approach additionally allows for diameter scaling to further merge the gate depletion regions for the potential of normally 'off' operation. Unintentionally doped GaN (u-GaN), which is the common template of InGaN LEDs, is utilized to form the vertical wires to enable integration. For the source and drain of the nanowires, Ti is deposited and annealed to increase the doping on the top and bottom of the wires. A TiN layer is

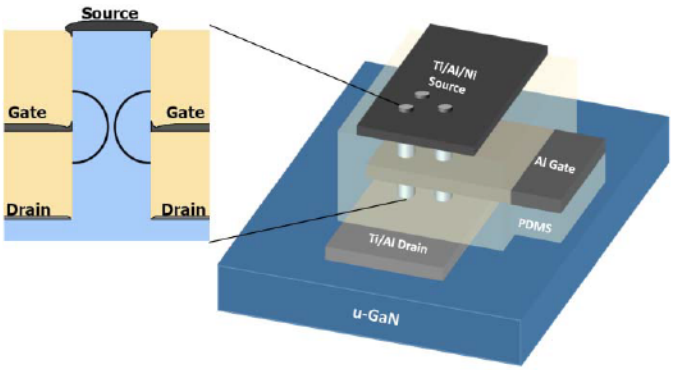

Fig. 1. Schematic of vertical GaN nanowire SIT combined with insert showing the depletion regions formed by the gate metal.

formed during the anneal which creates Nitrogen vacancies from the GaN [13], [14]. These Nitrogen vacancies act as donors, creating highly n-type regions on the top and bottom of the wires that form an n-i-n structure. The vertical GaN nanowire SIT will be suitable in enabling voltage-control, fast switching, seamless integration without interconnect parasitics, and better scaling for μLEDs.

II. Device Fabrication

Here, GaN nanowire SITs are proposed and fabricated, as illustrated schematically in Fig. 1. Several SITs are in parallel for ease of fabrication. A top down etch to form the nanowires, and a layer by layer fabrication process are utilized to build the complete structure. Layers of metal are put down with layers of dielectric, polydimethylsiloxane (PDMS), in-between to create the separations. The final device is pictured in Fig. 1 showing the complete architecture with a cutaway view. The gate-all-around design creates a controllable depletion region shown as the solid black lines in cutaway of Fig. 1.

The proposed fabrication flow of the SIT is shown in Fig. 2 with corresponding Scanning Electron Microscope (SEM) images. The starting material used for the SIT device was u-GaN grown on a sapphire substrate. The layer of u-GaN was 6.2 μm thick with a background n-type doping of low to mid 10^{16} cm^{-3}. Silica nanospheres with 700 nm in diameter were spin coated to provide the masking pattern for the nanowire etch [15]. These nanospheres formed a close-packed hexagonal array which uniformly coated the surface. The coated spheres were then Reactive Ion Etch (RIE) etched with SF_6 and O_2 in order to radially shrink the sphere diameter from 700 nm to 550 nm which correspondingly shrinks wire diameter. The spheres provide the hard mask for the chlorine based RIE etch which forms the initial shape of the nanowires. The chlorine RIE etch operates at 150W with a pressure of 65 mTorr, 30 Standard Cubic Centimeters per Minute (sccm) of Cl_2, 25 sccm BCl_3, 2 sccm $CHCl_3$, and 30 sccm of Ar. After the chlorine RIE etch, the nanowires are treated in KOH in order to both shrink the diameter and remove damage from the dry etch [16]. Fig. 2(a) shows the results of the fabricated GaN nanowires from a less dense area. The nanowires height and diameter are measured as ~1.5 μm and ~350 nm, respectively. The spacing between the nanowires is ~350 nm. Smaller diameter wires can lead to positive threshold voltages as the

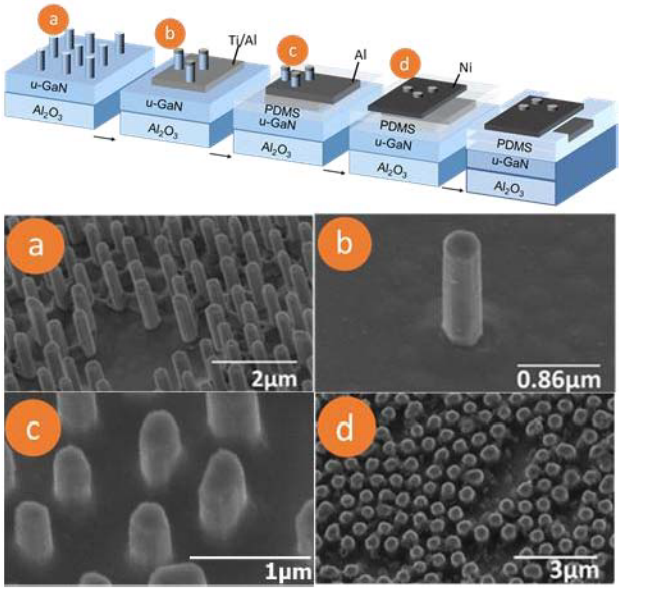

Fig. 2. (a) RIE and KOH Wet etch of nanowires, (b) Ti/Al metal evaporation and anneal, (c) PDMS coat with etch-back and 30nm Ni gate evaporation, (d) PDMS coat with etch-back and Ni top metal gate.

depletion regions caused by the gate metal work function can form a complete barrier to prevent current flow.

With the nanowires formed, 20 nm of Ti and 10 nm of Al are deposited through evaporation and lifted-off in order to form the source and drain. Fig 2(b) shows the Ti/Al coating the top and base of a wire in an uncommonly sparse region to highlight the deposition. To ensure the top and bottom of the devices are coated with metal but not the sidewalls, the samples are placed flat directly above the source metal with no sample rotation during deposition. The samples are then annealed in a two-step process, 10 min at 600 °C followed by 20 s at 900 °C in an N_2 atmosphere. The anneal causes nitrogen vacancies as TiN forms which creates an n-i-n structure in the nanowire [13], [14].

Following the metal deposition, a layer of PDMS is spin-coated. PDMS is chosen as the inter-metal dielectric due to the property of resistance to chemical removal [17], [18]. The PDMS is etched back through an RIE with SF_6 and O_2 to reveal half the wire height. During the PDMS etch back, the top metal is pulled back slightly, removing the slight overhang which could form during evaporation. 30 nm of Al is then evaporated and lifted-off to create the gate of the device, as shown in Fig. 2(c). The SEM image shown in Fig. 2(c) shows the nanowires after gate metal deposition, illustrating how the PDMS supports the metal and how the metal wraps around the wire. Here the deposited metal thickness defines the SIT gate length instead of lithography due to the horizontal nature of the evaporation. With the gate metal deposited, another PDMS layer is spin-coated and etched back to expose the top tips of the nanowires. The top metal of 90 nm of Ni is then deposited and lifted-off in order create a contact for probing. A final patterning and PDMS etch step is performed to uncover the buried metal contacts for electrical testing, as shown in Fig. 2(d).

The presented process flow includes less complexities and better integration potential compared with alternative works on vertical GaN nanowire Metal Oxide Semiconductor Field

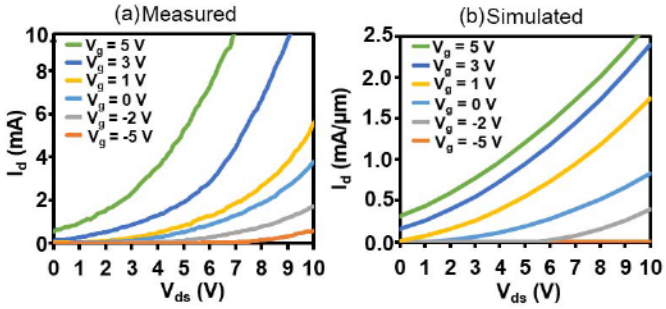

Fig. 3. (a) Measured SIT family of curves, (b) Silvaco simulated single nanowire SIT family of curves.

Effect Transistors (MOSFETs) [19], [20]. These nanowire MOSFETs typically rely on Atomic Layer Deposition to form a gate dielectric, combined with an added etch to remove the dielectric from the top and bottom of the nanowires. Sputtering is also used for the gate deposition which provides less control over the gate length [19], [20]. Use of u-GaN as a starting material for an SIT also opens door to many possible integration schemes for micro display.

III. Results and Discussions

Device characterizations are performed on the fabricated SITs. Devices of $150\mu m^2$ are fabricated which are composed of up to 1,600 wires. The electrical results for the family of curves are shown in Fig. 3(a) with the gate voltage varying from 5 V to −5 V. Current flows under no gate bias ($V_g = 0$ V), and can be pinched-off through a negative gate bias or increased by applying a positive gate bias. Similar trends are found in the 2D Silvaco Atlas simulations of a single nanowire SIT in Fig. 3(b). Note that drain current levels are lower from simulation which is due to the use of a single nanowire versus multiple nanowires in parallel from experiments. The non-linear and non-saturating behavior from both simulation and measurements is common to SITs, and is caused by punch through due to the short gate length. The SIT exhibits triode-like behavior, in contrast to pentode-like experienced by MESFETs and other devices due to punch through.

Fig. 4(a) shows the drain current vs. gate voltage (I_d-V_g) behavior of the device. Looking at the on/off characteristics in Fig. 4(a), the device shows the ability to support moderate current with low leakage. The off current is at 5×10^{-11} A while the device on current reaches a level of 1×10^{-4} A showing an I_{on}/I_{off} of 2×10^6. The on to off ratio is promising for a preliminary device and the gate-all-around design shows an improvement over GaN SIT fin designs which have an on/off ratio of 2.2×10^3 [12]. The device is normally 'on' until pinched off by a reverse gate bias which occurs around −1 V. A substhreshold slope (SS) of 126 mV/dec is extracted from the curve. This value is slightly higher than the ideal of 60 mV/dec due to slight variations in the nanowire diameters, where larger diameter nanowires in parallel require more negative voltage to fully pinch off. Measurements of the gate leakage are also recorded and shown in Fig. 4(b). The SIT device conventionally operates at low reverse biases on the gate to pinch off the channel. Schottky gates inherently suffer additional leakage compared with capacitive gates, as the

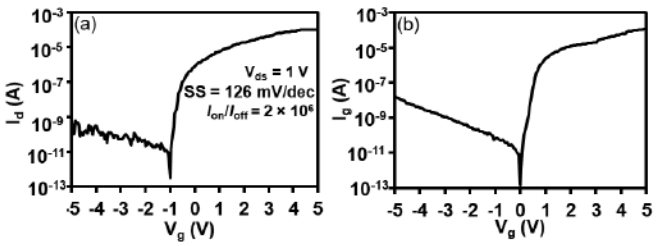

Fig. 4. (a) V_g vs. I_d curve showing the on and off current at $V_{ds} = 1$ V, and subthreshold slope (SS), (b) SIT schottky gate leakage.

further reverse bias allows electron tunneling from the metal. The SIT shows leakage current as low as 10^{-11} A at low negative voltages.

IV. Conclusion

In summary, GaN nanowire SITs were purposed and fabricated for the first time. These devices employ a top down nanowire formation combined with a layer-by-layer fabrication approach to form vertical structures. Use of u-GaN followed by annealing allows for the fabrication of an n-i-n structure. An I_{on}/I_{off} ratio of 2×10^6 is obtained from these initial devices which is due to the gate-all- around design. These initial results demonstrated that vertical nanowire SITs by the use of u-GaN which is typically the template layer for LEDs will enable voltage-controlled components for new integration schemes and opportunities in micro display technology.

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