Monolithic Integration of GaN Nanowire Light-Emitting Diode With Field Effect Transistor

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***Abstract*— Gallium nitride (GaN)-based light-emitting diodes (LEDs) are being investigated for the next generation display technology. The persistent issue, however, has been the lack of ability to integrate transistors with LEDs for control. Here, a novel vertical integration scheme is utilized to fabricate nanowire LEDs with nanowire field effect transistors (FETs) for the first time. This approach utilizes the unintentionally doped GaN template layer which is common to LED growth for the fabrication of nanowire FETs. The demonstrated voltage-controlled light-emitting unit provides area savings, scaling, and easier fabrication due to the vertical integration. For these initial nanowire devices, light modulation is demonstrated with LED turn OFF at −10 V. Due to the nanowire approach, these devices show over two times improvement in the I_{ON} to I_{OFF} ratio compared with the alternative integration schemes.**

***Index Terms*— LED, GaN, nanowire LED, LED display, nanowire FET, static induction transistor.**

I. Introduction

CURRENT display technology is reaching limitations as the thin-film transistors (TFTs) used for liquid crystal displays or solid state light-emitting diodes (LEDs) are struggling to be reduced in size, and to be increased in efficiencies [1]–[4]. To solve these issues and introduce the next generation of display technology, power electronics combined with LEDs based on GaN are being pursued [5]–[7]. GaN based LEDs offer higher efficiencies of up to 80%, improved long-term reliability, and the ability to be manufactured at the nanoscale [8]–[10]. The emergence of micro-LEDs (μLEDs) and nanowire LEDs are opening doors to have LEDs directly compose individual pixels, removing conversion losses [11]–[13]. A number of important display applications will be significantly improved such as virtual reality (VR) and augmented reality (AR), due to the efficiency, nanoscale pixels, and transparent nature of GaN LEDs. Both μLEDs and nanowire LEDs provide these solutions, though the persistent problem is the lack of FETs in order to control these LEDs. To address the lack of integration there is potentially promising electronic candidates based on the same material system that can be integrated with such μLEDs to achieve the voltage-controlled component.

To provide the voltage control, AlGaN/GaN high electron mobility transistors (HEMTs) have been initially investigated to be laterally integrated with InGaN/GaN LEDs [13], [14]. The integration with the HEMT-LED presents a number of issues: 1) the presented integration makes use of etch back and high temperature regrowth [13], [14] which often leads to defect incorporation and added cost; 2) interconnects are required between the LED and HEMT which introduce resistance; and 3) LED display area is lost to the HEMTs. Alternative approaches include integration of TFTs with LEDs, though these displays are limited in both performance and scaling [15]. To address these issues, vertical GaN FETs are presented, removing the reliance on regrowth, eliminating interconnects, and erasing LED area consumption.

Novel to this work, a nanowire GaN gate-all-around (GAA) FET is monolithically integrated at the base of a nanowire InGaN/GaN LED for the first time. The nanowire FET makes use of the u-GaN layer common to InGaN/GaN LED growth. The vertical integration allows individual nanowire LEDs to be addressed with none of the issues experienced by previous approaches. Ti is deposited at the base of the wire and annealed to induce nitrogen vacancies which act as donors [16], [17]. The Ti annealing combined with the higher conductivity of the initial buffer layer [18]–[20] creates a bottom n-type region. The generated bottom n-type region at the base of the wire, combined with the u-GaN layer and the n-type GaN from LED, make an n-i-n structure for a FET.

The initial nanowire FET chosen to be integrated with the nanowire LED is the static induction transistor (SIT). More details on the characteristics of the SIT can be found from Ref. 21. Multiple types of FETs such as the conventional metal oxide semiconductor field effect transistor (MOSFET) can alternatively be integrated. The SIT though is a straightforward vertical power device that offers easier manufacturing without need for atomic layer deposition (ALD) [21]–[24]. A schottky gate is used to modulate the depletion region in the nanowire in order to pinch off current. Triode-like curves are produced

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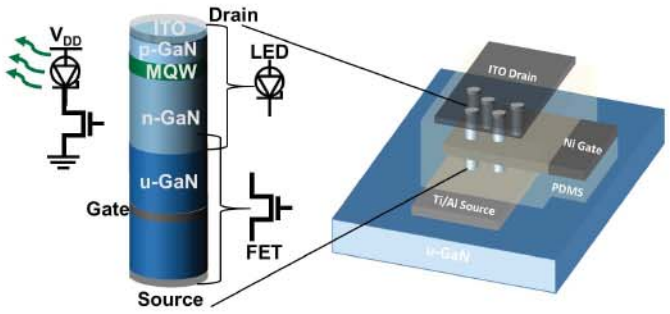

Fig. 1. Schematic of the vertical GaN nanowire LEDs with the nanowire FETs, inset showing a single wire and series connection.

in the SIT device due the short gate length [21]–[24]. This preliminary work offers an advantageous alternative approach to integrate nanowire LEDs with nanowire FETs for displays without sacrificing display area or performance.

The presented approach makes use of a top-down etch in order to form the nanowires. The top-down approach allows for use of conventional LED wafers in order to readily integrate LEDs with FETs. Previous works have demonstrated the ability to fabricate multiple-color nanowire LEDs, which are needed for displays, through top-down approaches [25], [26]. Top-down approaches leverage existing fabrication facilities for large scale device manufacturing. Alternatively, a bottom-up growth technique can be utilized to grow unique colored nanowires [27]. The nanowire growth techniques utilize methods such as molecular beam epitaxy (MBE), which has limitations for large scale manufacturing due to single-wafer growth and uniformity issues [27]. Nevertheless, the presented device fabrication to introduce LEDs and FETs can similarly be accomplished through both top-down and bottom-up created nanowires.

II. Device Fabrication

For the first time GaN nanowire FETs have been vertically integrated with nanowire LEDs. The integration scheme has been both proposed and fabricated, shown by Fig. 1. Avoiding the need for advanced lithography, an average of 45 wires are fabricated in parallel for each device. A multilayer fabrication approach was utilized, forming the wires through a top-down dry etch, while the contacts are build up through dielectric and metal layers. Metal is evaporated to avoid sidewall coatings, with polydimethylsiloxane (PDMS) spin coated and etched back to provide the transparent spacers. Fig. 1 illustrates the nanowire FET and nanowire LED integration, with a single wire showing the series connection.

A conventional InGaN/GaN green LED on sapphire is used here which composes a 20 nm GaN buffer, ~3 μm of u-GaN (10^{16} cm^{-3} background doping), 3 μm of n-GaN, InGaN/GaN multiple quantum wells (MQWs), 150 nm of p-GaN, and 1 nm of p-InGaN. Silica nanospheres with 3 μm diameter diluted in de-ionized (DI) water are spin coated to provide a sparse coating to mask the nanowire etch [28]. Nanosphere lithography used in this work provided a cost-effectively alternative over conventional lithography for patterning. The coated spheres are radially shrunk in 10:1 buffer oxide etch (BOE) from 3 μm to 1.6 μm, which correspondingly shrank the final

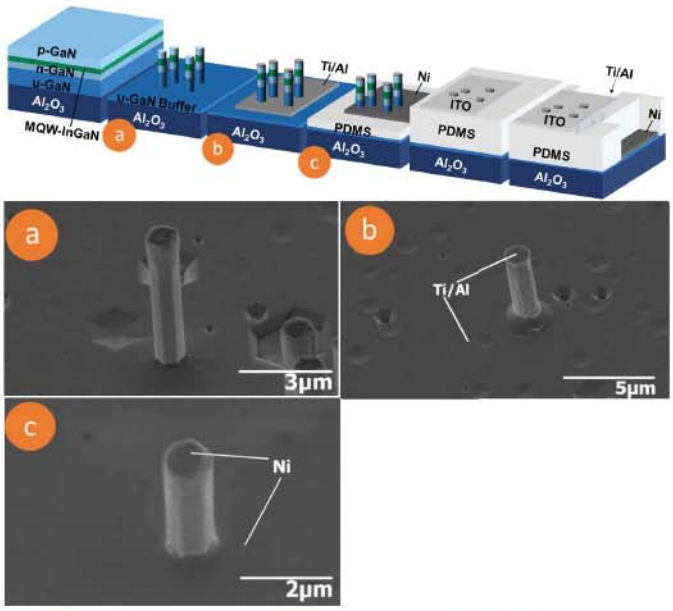

Fig. 2. (a) RIE and KOH etching of InGaN/GaN nanowires, (b) Evaporation and anneal of Ti/Al source and drain, (c) 40 nm Ni GAA on PDMS.

nanowire diameter. SiO_2 spheres provide high selectivity over the chlorine reactive ion etch (RIE) and set the wire diameter. The RIE etch recipe developed uses 225W of power at a pressure of 65 mTorr, flowing 30 standard cubic centimeters per minute (sccm) of Cl_2, and 20 sccm of Ar, leading to an etch rate of ~225 nm/min. Following the RIE etch, a 10:1 BOE etch is done in order to remove the nanospheres. To remove etch damage from the RIE and further reduce the wire diameter, a KOH wet etch is performed [29]. The KOH etches select crystal planes corresponding to the wire diameter, while leaving the top surface of the wires untouched [29]. Fig. 2(a) shows the results of this process in the scanning electron microscope (SEM). The dry etching created nanowire heights of 5.5 μm, with the KOH shrinking the diameters down to ~1 μm. The depletion regions formed by the schottky gate at this diameter are not enough to pinch-off the device under no gate bias. Decreasing the nanowire diameter further can merge these depletion regions providing normally off behavior.

Following the dry etch and KOH wet etch, lift-off resist (LOR) and photoresist are coated and patterned. 20 nm of Ti and 10 nm of capping Al then are evaporated. Lift-off is performed in PG-Remover in order to remove the metal on the photoresist, leaving Ti/Al on the tops and base of the wires which act as the source and drain, Fig. 2(b). An anneal is next done to cause the formation of nitrogen vacancies as TiN is formed [16], [17]. The anneal is done at 600 °C for 10 min then 900 °C for 20 s.

PDMS is then spin coated which provides the spacer between the metal layers, and planarizes the surface. PDMS is optically transparent and will not be removed in common chemistries such as developers [30], [31]. After spin coating, the PDMS is RIE etched with CF_4 and O_2 to reveal about half of the u-GaN region. For the gate metal, patterning is performed and 40 nm of Ni is evaporated followed by an

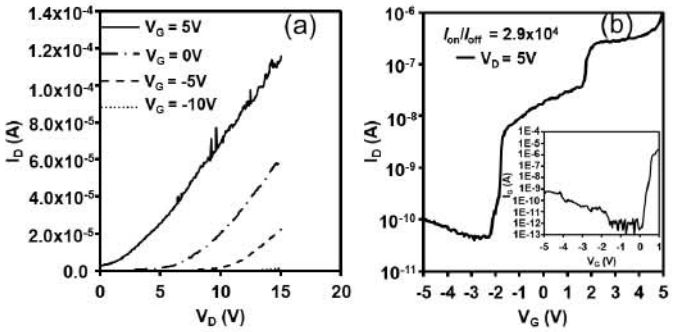

Fig. 3. (a) I_D vs. V_D with varying gate bias, (b) I_D vs. V_G at $V_D = 5$V, inset: gate leakage V_G vs. I_G.

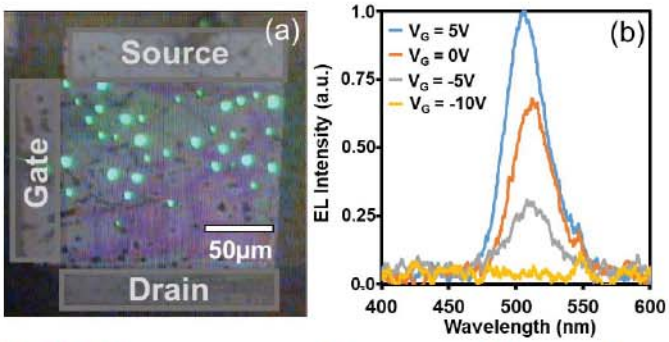

Fig. 4. (a) Nanowire LEDs with FETs lighting up. (b) EL spectra with gate modulation.

additional lift-off, Fig. 2(c). The gate metal forms a schottky GAA contact with wire, which can be seen in Fig. 2(c). Making use of a vertical FET allows the gate length to be set by the metal thickness instead of conventionally lithography, allowing for the fabrication of small gate length devices.

Following the gate evaporation more PDMS is spin coated and etched to reveal the tops of the wires. To allow for light emission, indium tin oxide (ITO) is utilized due to the high transparency. 80 nm of ITO is sputtered, followed by lift-off. Patterning and PDMS etching is done as a final step to uncover the gate and source contacts which have been buried.

Making use of a layered approach with evaporation allows for device planarization which is not present in previous works on vertical GaN MOSFETs [32], [33]. Previous works on vertical GaN nanowire devices also utilized ALD for the gate dielectric, with subsequent etches, which is not needed for a schottky gate [32], [33]. A sputtered gate has conventional been used, though evaporation here is found to provide the ability to fabricate small gate lengths [32], [33].

III. Results and Discussions

Electrical measurements have been performed on the fabricated nanowire LEDs with integrated FETs. For ease of fabrication an average of 45 wires are in parallel to compose each device. First the I_D-V_D results are recorded with the gate bias set from 5 V to −10 V in 5 V steps, Fig. 3(a). For use of the SIT in this preliminary device, the 1 μm diameter for the wires is not small enough to pinch off current at ($V_G = 0$ V). The SIT is a depletion mode device with negative gate biases used to pinch off current, or alternatively, positive gate biases to increase current. The triode-like results are the expected behavior for an SIT device [22]–[24]. The I_{on}/I_{off} performance showing the drain current vs. gate voltage (I_D-V_G) is shown in Fig. 3(b) with a forward bias of 5 V. Due to the SIT, the device is in depletion mode, where the LEDs are "on" until switched off at a gate voltage of −2.2 V. The device shows an I_{on}/I_{off} ratio of 2.9×10^4 at V_D of 5 V which is a 2.4x improvement over the HEMT-LED integration [14]. The step behavior observed in the I_D-V_G curve indicates the presence of trap states [34]. A gate dielectric could be utilized to decrease the I_{off} and lower interface trap states. On the other hand, thicker gate metal would provide a larger gate barrier to also prevent leakage. The gate leakage levels are recorded between the gate and source, shown by the inset of Fig. 3(b). Gate leakage as low as 10^{-12} A is seen for the device.

Fig. 4(a) shows the ∼45 individual nanowires lighting up at 10 V. Due to the intentional sparse and random spin coated distribution, individual nanowires in close proximity show up brighter. The largest spots in Fig. 4(a) are three individual wires in close proximity that appear as one nanowire when turned on, due to the level of brightness. The smallest spots in Fig. 4(a) are isolated wires. Spin coating a close packed array or use of photolithography would allow high densities of ordered wires. Electroluminescence (EL) measurements were performed to view the spectra under various gate biases for modulation, as shown in Fig. 4(b). A bias of 24 V was applied in order to drive the 45 nanowire LEDs to produce excess light for the detection setup. Under zero gate bias current flows in the SIT to turn "on" the LEDs. Increasing the gate bias creates additional current flow for the LED that correspondingly increases the brightness. Conversely, applying a negative gate bias extends the gate depletion regions to pinch off current flow. The LED brightness decreases and turns off with negative gate biases. The LED is observed to fully turn off at a −10 V gate bias. These results match up with the recorded family of curves in Fig. 3(a).

IV. Conclusion

In summary, GaN-based nanowire FETs and nanowire LEDs were vertically integrated together for the first time. This novel integration makes use of the previously unused u-GaN layer to fabricate a GAA FET. Vertical integration allows for individually addressable nanowires for displays, removes the issue of lateral area consumption, and eliminates parasitic interconnects. As a preliminary demonstration, nanowire SITs are chosen to be integrated with the InGaN/GaN nanowire LEDs due to ease of fabrication. A planarized approach to fabrication is utilized making use of metal layers and transparent PDMS. Control over the nanowire LEDs is exhibited with classical SIT performance recorded. The nanowire LEDs can be modulated, turning off at −10 V. This work can open the door to next generation of GaN-based LED displays for electronics, VR, AR, and more.

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