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Effect of varying the gate voltage scan rate in a MoS_2/ferroelectric polymer field effect transistor

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ABSTRACT

A ferroelectric FET using MoS_2 and PVDF-TrFE was fabricated, and the effects of varying the gate voltage scan rate from 200 mV/s to 4 mV/s investigated. Charge mobility, sub-threshold voltage swing and the memory window width depended on the scan rate. Prior to switching on, a negative trans-conductance was observed for all scan rates, followed by a rapid increase in the channel current to the on state. A model based on nucleation of ferroelectric domains and unrestricted domain growth was used to explain these results. By lowering the scan rate, the performance of polymer based FE-FET's can be improved.

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KEYWORDS
MoS2; PVDF-TrFE; FE-FET; gate scan

1. Introduction

MoS_2 is a transition metal dichalcogenide composed of atomically thin covalently bonded S-Mo-S planar layers stacked vertically via weak van der Waals bonding between layers [1]. Exfoliation [2–5] or chemical vapor deposition (CVD) [6–10] are two methods to obtain MoS_2 thin films. The latter technique can be tuned to grow single crystals of varying sizes at pre-determined locations on a substrate [11]. MoS_2 is an n-type semiconductor with a band gap that varies from 1.2 eV in the bulk to 1.8 eV in the monolayer limit [1, 12]. Using linear dielectrics (like SiO_2) as the gate insulator in a field effect transistor (FET) configuration, MoS_2 can be used in on/off switching applications [13]. Employing a non-linear ferroelectric (FE) with permanent dipoles as the gate insulator has the additional advantage of charge storage, and therefore, write/erase functionality [14, 15]. A unique feature of a FE-FET is the ability to remain on(off) even after the gate voltage is removed.

Both organic [14] and inorganic [16, 17] FE materials have been used as the gate insulator in FE-FET's. Organic FE polymers when used as the gate insulator add flexibility, light weight, non-toxicity, low temperature and inexpensive processing techniques to fabricating such devices. One such room temperature FE copolymer is poly(vinylidene fluoride-trifluoroethylene), $(\text{-}CF_2\text{-}CH_2\text{-})_n\text{-}(CF_2CHF\text{-})_m$ (PVDF-TrFE) [18]. Rapid dipole orientation (polarization) and direction reversal, which determines how fast a device can operate,

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are essential for practical use. Molecular chain dynamics are typically slower in polymers compared to single crystals due to their large size. Since polarization of the insulator is gate controlled in a FET, choosing the right gate voltage scan rate is important for optimized transistor performance. While there are few reports on exfoliated multilayer MoS_2/FE polymer FET's [14, 19–25], no study has been done on the effect of gate voltage scan rate in these devices.

In this paper, we fabricated transistors using chemical vapor deposition (CVD) grown MoS_2 monolayers and PVDF-TrFE as the gate insulator. The effects of varying the scan rate from 200 mV/s down to 4 mV/s were investigated. Our results revealed a narrowing in the memory window (MW), an order of magnitude increase in the mobility (μ) and a decrease in the sub-threshold voltage swing (SS) at slow scans. These parameters appear to stabilize at lower scan rates suggesting an asymptotic limit to their values. A model based on nucleation and unrestricted domain growth was used to explain these results. By lowering the gate voltage scan rate, which in turn optimizes MW, μ and SS, the performance of polymer based FE-FET's can therefore be improved.

2. Experimental

Monolayer MoS_2 flakes were grown directly on a 300 nm SiO_2/Si substrate by CVD. First, a 1% sodium cholate solution, known to act as a growth promoter for MoS_2, was spin coated at 4000 rpm for 60 s onto the SiO_2 substrate. A droplet of a saturated solution of ammonium heptamolybdate in deionized (DI) water was deposited onto the substrate and left to dry in air, providing the molybdenum feedstock. The substrate was placed in the center of a 1 in. CVD tube furnace, and 15 mg of solid sulfur was placed 15 cm upstream from the substrate. Growth occurred at atmospheric pressure in a flow of 750 sccm of nitrogen gas (99.999% purity). The furnace temperature was ramped up to 750 °C at a rate of 70 °C min^{-1}. While the Mo source and SiO_2 growth substrate reached 750 °C, the maximum temperature of the sulfur was ∼150 °C. After a 15 min growth period, the furnace was opened, and the sample rapidly cooled to room temperature in 1000 sccm flowing nitrogen. Figure 1a shows the selected area electron diffraction (SAED) pattern and it displays one set of strong single crystal diffraction spots, attributed to the good crystallinity of MoS_2 with a hexagonal structure. Figure 1b shows a high magnification TEM image of a section of the crystal. The atoms are ordered in a hexagonal pattern characteristic of the MoS_2 structure [1], confirming the high-quality, low-defect growth of this crystal. Figure 1c shows an atomic force microscope (AFM) image of an isolated as grown single MoS_2 crystal together with a height profile along the black scan line. The inset to Figure 1c shows that the crystal is ∼1 nm thick, as expected for monolayer MoS_2. Figure 1d shows a representative Raman spectra of the MoS_2 crystals used in this study. The peak at 384 cm^{-1} corresponds to the in plane E^1_{2g} mode and the peak at 405 cm^{-1} corresponds to the out of plane A_{1g} mode [25]. Peak separation is 21 cm^{-1}, again confirming that the MoS_2 crystal was one layer thick [26].

Single domain MoS_2 monolayers were transferred from the Si/SiO_2 growth substrate to avoid possible detrimental effects of current leakage through the oxide. The substrate was first spin coated with a thin film of poly(methyl methacrylate)-PMMA and immersed in a 0.1M KOH solution. Slow oxide dissolution separates the PMMA layer

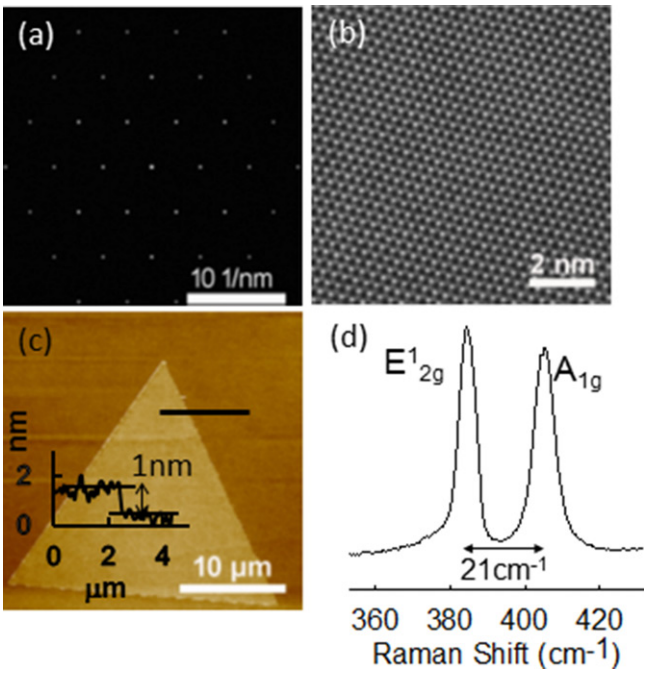

Figure 1. (a) Selected area electron diffraction (SAED) pattern of MoS_2. (b) High resolution TEM image showing the hexagonal symmetry of the atomic arrangement in MoS_2. (c) AFM image of a single MoS_2 flake together with the height profile along the black scan line. (d) Raman spectrum of MoS_2 showing two peaks characteristic of MoS_2 single crystals.

and adhered MoS_2 flakes from the substrate. The free-standing film was washed with deionized water to remove any trace amounts of KOH and placed on clean Si^{+}/SiO_2 substrates with pre-fabricated electrode pairs. After drying in an oven at 70 °C for 15 mins, the PMMA film was dissolved in acetone leaving MoS_2 monolayers lying over the substrate, some of which bridged the gap between the pre-fabricated electrodes. Figure 2a shows a top view optical microscope image of one such substrate with several MoS_2 monolayers transferred on to the surface. The black arrow indicates a monolayer MoS_2 channel connecting two electrodes (drain-D and source-S) that are separated by 4µm. The substrate was then annealed in air at 70 °C for 24 hrs. to improve the contact between MoS_2 and the electrodes. PVDF-TrFE (75/25) purchased from Kureha, Japan (KF W# 2200) was 99.9% pure and was used as received. A 9 wt% of this polymer was dissolved in N,N-dimethylformamide-DMF and spin coated at 4000 rpm for 45s onto the substrate. A hot air gun placed 20 cm away was used to pre-dry the film during spinning. The substrate was once again placed in an oven at 70 °C for 24 hours to further remove trace amounts of DMF in the film. Figure 2b shows the same substrate as seen in Figure 2a after annealing. The film thickness was ∼ 800 nm. Using a thin slit in an Al foil as a template, the gate electrode (G) made of Ag was thermally evaporated to cover the drain-source gap of the device as seen in Figure 2c. A small section of the polymer was scratched to expose the S/D electrodes and the device was hard wired with silver epoxy and gold wire. Figure 2d shows a schematic cross-sectional view of the device with the various components labeled. Figure 2e shows the chemical structure of

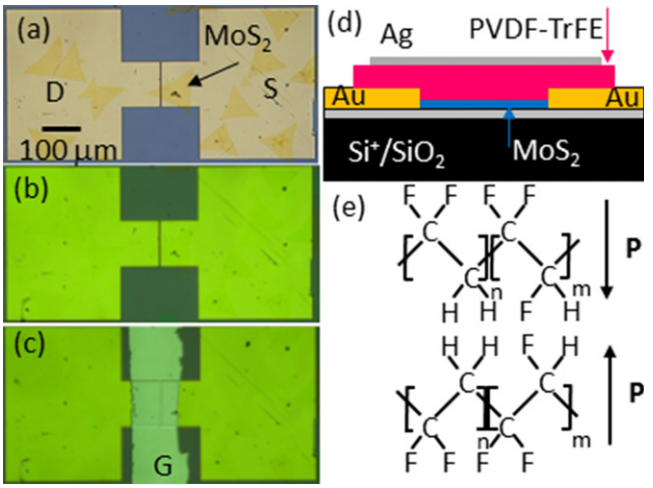

Figure 2. (a) Optical microscope image of the pre-patterned Si/SiO_2 substrate with MoS_2 single crystal flakes transferred on to it. The drain (D) and source (S) electrodes are separated by a gap of 4µm. The black arrow indicates a MoS_2 crystal bridging the gap between the S/D electrodes. (b) Same substrate as in (a) but with a spin coated thin film of PVDF-TrFE. (c) Same as in (b) after the Ag gate (G) electrode was thermally evaporated to cover the S/D channel. (d) Schematic cross-section of the device showing the important components. (e) Chemical structure of the basic unit of PVDF-TrFE in the FE phase. The up and down polarization (**P**) configurations result from a 180° rotation of the polymer chain.

PVDF-TrFE with the up and down polarization chain conformations. The average polarization (**P**) in PVDF-TrFE points from the negative F to the positive H atom perpendicular to the polymer chain [19].

Drain/source currents (I_{DS}) and voltages (V_{DS}) were measured with a Keithley Model 6517A electrometer and the gate voltage (V_{GS}) was supplied via a Keithley Model 2400 source meter. Capacitance measurements were made with an Agilent Technologies 4294A impedance analyzer with a 50 mV AC exciting signal. All measurements were made at room temperature under a vacuum of 10^{-2} Torr provided by a roughing pump to reduce effects of adsorbed moisture.

3. Results and discussion

The capacitive coupling between the gate and MoS_2 electrostatically dopes it in a FET configuration. Figure 3a shows the PVDF-TrFE capacitance as a function of frequency measured between gate and the drain electrodes with the source left open. The effective area of the capacitor, determined by the gate electrode overlap with the drain was roughly 100 µm × 60 µm as seen in Figure 2c. The capacitance approached 50 pF at 40Hz while at higher frequencies the capacitance gets smaller [18]. In order to confirm ferroelectric properties in PVDF-TrFE, the capacitance was measured with a DC voltage (supplied by the impedance analyzer) superimposed over the exciting AC frequency at 10 kHz. With the impedance analyzer Hi terminal connected to the gate and the Lo terminal to the drain (source left open), the dc voltage was scanned from inversion to accumulation at different scan rates. The scan sequence was 0V → +30V → 0V→ −30V → 0V. At the

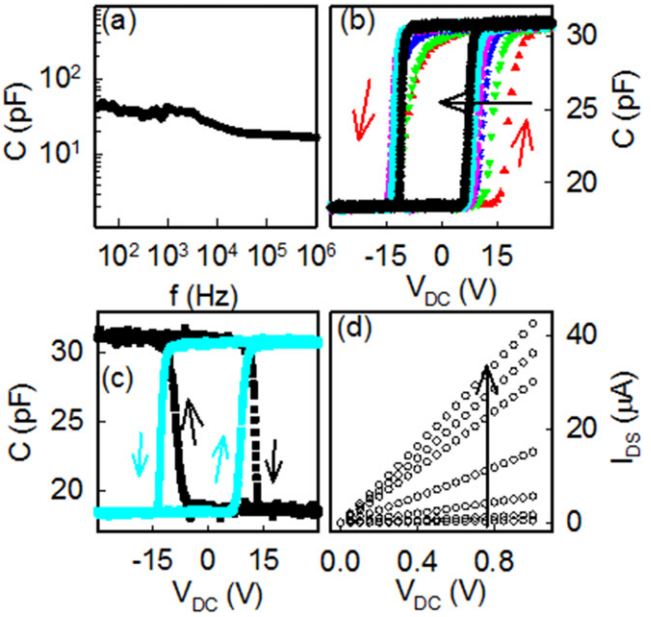

Figure 3. (a) Small AC signal (50 mV) capacitance as a function of frequency measured between the gate and the drain terminals of the device with the source terminal open. (b) Small signal (50 mV, 10 kHz) capacitance as a function of DC voltage (V_{DC}) superimposed over the AC signal, taken at different voltage scan rates of (in mV-s^{-1}) 200 (red), 100 (green), 40 (blue), 20 (pink), 10 (cyan), 4 (black). The black arrow points from the fastest (red) to the slowest (black) scan rate. In these measurements, the impedance analyzer Hi terminal was connected to the gate and Lo to the drain electrodes of the device. Each DC voltage scan was as follows: 0V→ +30V→ 0V → −30V → 0V. (c) Same as in (b) at a constant scan rate of 10 mV/s applied in the same direction as in (b) but with the impedance analyzer Hi terminal connected to the drain and Lo terminal connected to gate electrodes of the device (black curve). The cyan color curve is reproduced from (b) and corresponds to the sweep speed of 10 mV/s. (d) Drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) for voltages 0 → 30V in steps of 5V applied to the gate as indicated in the direction of the black arrow.

end of each scan, the capacitance returned to its original value as seen in Figure 3b. The polarization intensity at the beginning and end of each scan therefore coincide. The change in the capacitance from inverted to accumulated mode was ∼13 pF as seen in Figure 3b for all scan rates. This suggests that the charge accumulated on the capacitor reaches a constant value as long as the dc voltage exceeds a lower limit. For all scans, the C-V measurements show counter clockwise rectangular-shaped hysteresis curves and confirm the characteristic FE feature of PVDF-TrFE [27]. The MW (measured horizontally at 25 pF) got narrower for slower scan rates, and was therefore dependent on the FE polarized state of the gate insulator [28]. The voltage corresponding to this width was 26V for a scan rate of 200 mV/s and approached 17V for a scan rate of 4 mV/s. The change in the capacitance during the transition from inversion to accumulation and vice versa got steeper for slower scan rates. Interchanging the impedance analyzer terminals in the same device and maintaining the same scan sequence, resulted in a clockwise hysteresis curve of similar shape for the same scan rate as seen in Figure 3c. This re-confirmed that the polymer film was ferroelectric and that it was symmetric with respect to the contacts with the gate and drain electrodes.

Figure 3d shows I_{DS} versus V_{DS} for different V_{GS} voltages. V_{DS} was varied at 100 mV/s during the measurement. A linear I_{DS}-V_{DS} curve for zero gate voltage indicates Ohmic contact at the metal electrode/semiconductor interface [14]. In addition, we see that a positive gate voltage increased the channel current. This demonstrated that the device operated as an n-type FET and the majority carriers were electrons [7]. The device was turned on by applying a gate voltage of 30V and the on state resistance was 24 kΩ at $V_{DS} = 1V$. This is comparable to other monolayer MoS_2 transistors in the on state [29] and implies a low contact resistance in our device. Comparing the rate of increase in I_{DS} with V_{GS} at $V_{DS} = 1V$ in Figure 3d with the change in the capacitance in Figure 3b we noticed a strong correlation. The largest changes occurred around $V_{GS} \sim 15V$ and it was precisely when the capacitance underwent the most rapid change (green curve-Figure 3b). This strongly indicates a FE field effect driven current increase. To further study the effects of varying the gate voltage scan rate on device performance, the trans-conductance curves were investigated in greater detail.

Figure 4 shows the trans-conductance I_{DS} versus V_{GS} curves at fixed V_{DS} of +1V for various top gate voltage scan rates. The gate voltage was swept from $-30V \rightarrow 0V \rightarrow +30V \rightarrow 0V \rightarrow -30V$ in each scan. Consistent with Figure 3d, the channel current increased with increasing $(+)V_{GS}$. We also saw that the channel current remained high (on state) even when V_{GS} was reduced to 0V for each scan rate. With the gate voltage at +30V, the electric field across the FE polymer was large enough to polarize it down (see Figure 2e). This resulted in a net positive bound charge at the interface with MoS_2 enhancing channel conduction. Reducing the gate voltage to zero still left a remanent polarization in the polymer that maintained the channel current in the on state. As the gate voltage was made more negative and exceeded the coercive voltage, the polarization changed direction. Now, a net negative bound charge at the interface with MoS_2 reduced channel conduction by depleting it of electrons and turned the device off. Increasing V_{GS} above 0V once again caused electrons to be injected into MoS_2. When V_{GS} exceeded the coercive voltage, the polarization switched direction again and the device was turned on.

As seen in Figure 4, as V_{GS} is made more positive, and prior to the device switching on, the channel current decreased even as V_{GS} increased (negative trans-conductance) and then increased abruptly to a value several orders of magnitude higher. At this point the device had turned on. The initial decrease in the current could be related to the negative capacitance effect that occurs in the gate insulator during polarization reversal [22]. Once turned on, relative current changes are smaller with increasing V_{GS}. The effects of a negative trans-conductance are not observed when the device was turned off. This most likely was due to insufficient charge in the depleted MoS_2 channel. The counter clockwise hysteresis confirmed that the device operated as a FE-FET [14] and the MW was dependent on the gate voltage scan rate. The transistor response was consistent with the capacitance-voltage response curves of Figure 3b. The abrupt changes in I_{DS} when the device switches from off to on and vice versa follow similar changes in the capacitance as the DC voltage was varied from inversion to accumulation and vice versa. Slower scan rates reduced the MW. The gate leakage current in all scans was in the range $-2nA < I_{GS} < 2nA$ and hence did not influence device operation except for minor contributions to the off state current. From Figure 4 we also see that the MW

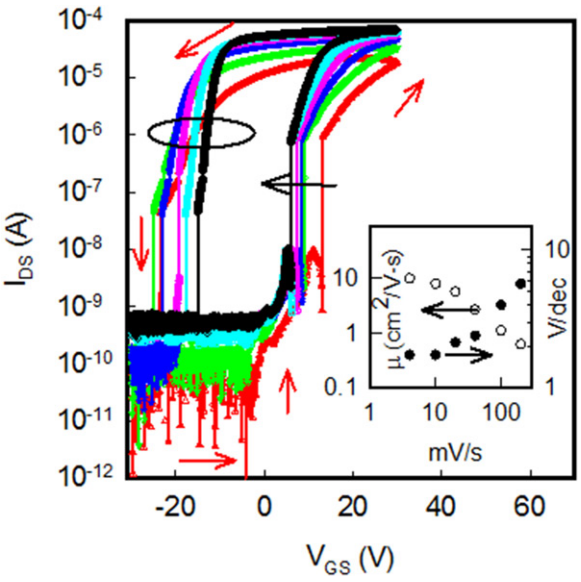

Figure 4. (a) Drain-source current (I_{DS}) as a function of gate-source voltage (V_{GS}) with the drain-source voltage (V_{DS}) fixed at +1V. The gate voltage was scanned in the following sequence for each scan rate: −30V → 0V → +30V → 0V → −30V. The scan rates were (in mV-s^{-1}) 200 (red), 100 (green), 40 (blue), 20 (pink), 10 (cyan), 4 (black) and correspond to each run measured consecutively as indicated in the direction of the black arrow (red: 200 mV-s^{-1} → black: 4 mV-s^{-1}). Red arrows indicate the counterclockwise direction of each of the device trans-conductance curves. **Inset:** Carrier mobility (○) and sub-threshold swing (●) in V/decade calculated from the slopes of the data taken at the left side of the plots (shown within the oval) and plotted as a function of scan rates.

was reduced from 37V at 200 mV/s to 21V at 4 mV/s. The device on/off ratio was ~10^5 for all scan rates.

From the linear portion of the I_{DS}-V_{GS} curve on the left side (within the black oval) the device trans-conductance ($g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$) and electron mobility ($\mu = \frac{g_m L}{W C_i V_{DS}}$) were extracted. Where L is the channel length (4 μm), W is the channel width (10 μm), C_i (830 nF/cm^2) is the gate insulator specific capacitance, calculated from the capacitance value at 40Hz in Figure 3a, and V_{DS} =1V is the fixed drain-source voltage. The SS measured along the steepest straight line section of the curve within the oval was also calculated. The lower inset to Figure 4 shows the variation of μ and SS as a function of scan rate. The mobility was seen to increase from 0.6–10 cm^2/V-s as the scan rate decreased from 200 mV/s to 4 mV/s respectively. Lowering the gate voltage scan rates led to an increase in μ by one order of magnitude and a lowering of SS. An asymptotic value for μ and SS are seen to be approached for slower scan rates. The MW also appears to stabilize around 21V for low scan rates. A narrower MW is more important for this FE-FET compared to higher μ and steeper SS, however all three parameters are improved with slower gate voltage scan rates.

In order to confirm the negative trans-conductance effect seen in Figure 4 [16], the device was characterized with a smaller V_{DS} to reduce large voltage gradients in the channel and across the gate insulator. Figure 5 shows the trans-conductance I_{DS} versus V_{GS} curve for V_{DS} = 0.1V, exhibiting an on/off ratio of ~10^4. Just as in Figure 4, the

gate voltage was swept from −30V → 0V → + 30V→ 0V → −30V in each scan. There is clear evidence of the negative trans-conductance effect prior to the device switching on, and it is therefore independent of V_{DS} over the tested range. The mobility was slightly reduced while SS increased slightly as compared to when $V_{DS} = 1V$. A smaller V_{DS} results in an increase in the MW for similar scan rates compared to Figure 4. The MW however decreased from 41V at 200 mV/s to 25V at 4 mV/s. The inset to this Figure shows the variation of mobility and SS as a function of gate voltage scan rates. The mobility was seen to increase from 0.02–0.6 cm^2/V-s as the scan rate decreased from 200 mV/s to 4 mV/s respectively. These values also appear to level off as the scan rate was made slower. The dotted curve in Figure 5 was taken at 200 mV/s with a back gate voltage (i.e. SiO_2 gate dielectric) after all top gate measurements were completed. The absence of counterclockwise hysteresis with back gate voltage scan re-confirmed the FE-FET operation of the device with a top gate voltage scan.

Useful FE-FET operation depends on the charge storage capability of the gate insulator as seen in Figures 4 and 5. The FE state in turn was controlled by the gate voltage and its scan rate. We used a model based on nucleation and unrestricted growth of domains applicable to FE polymers [30, 31] to explain our results. Figure 6 shows a schematic of the polarizing stages in the gate insulator upon application of a gate voltage. It proceeds via nucleation sites whose domain grows forward (energetically favored) rapidly in the direction of the applied electric field. Sideways growth via kink nucleation is a slower process. Eventually the FE domains coalesce and polarize the entire film. Nucleation sites are presumed to result from remanent polarization clusters or stimulated by a gate voltage. For rapid scan rates, we propose that the initial density of nucleation sites is small. Once the forward domain growth was complete across the gate insulator, further polarization proceeded via slower sideways domain wall growth. For few nucleation sites, the domains needed a large sideways growth before reaching and coalescing with other domains. This required a higher gate voltage. The top three panels from left to right show this process at a high scan rate. If the scan rate is very high, it is possible that a portion of the film may still remain un-polarized at the highest applied gate voltage prior to the scan reversing direction. The result of this effect was seen in Figures 3b, 4 and 5. In Figure 3b, the increase in capacitance and in Figures 4 and 5, the increase in I_{DS} are gradual for fast scan rates. In addition, the saturation on state currents in Figures 4 and 5 are also lower for higher scan rates due to incomplete film polarization and hence lower poling field. When the scan rate was slow, a larger amount of nucleation sites were able to form polar clusters. Sideways domain growth now quickly encountered other domains to polarize the entire film as seen in the lower three panels to Figure 6. This state can be reached at smaller gate voltages leading to a narrowing of the MW. Lower scan rates also yield higher saturation currents due to more complete film polarization and hence larger poling field. The higher electric field due to increased film polarization at slow scan rates results in higher transcondutance and hence higher mobility and steeper sub-threshold swing as seen in Figures 4 and 5. Lowering the scan rate even further does not lead to significant changes in the I_{DS}-V_{GS} curves since the entire gate insulator is likely completely polarized at low scan rates. The leveling out of the μ and SS as seen in the insets to Figures 4 and 5 shows that they approach some asymptotic limit to their values. This allows one to choose a voltage

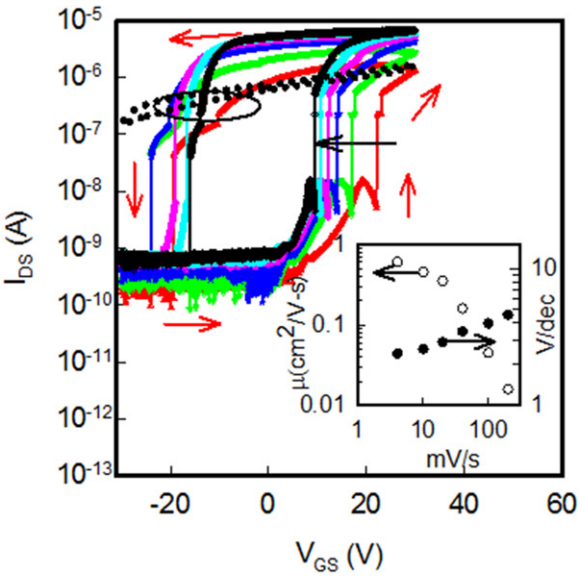

Figure 5. (a) Drain-source current (I_{DS}) as a function of gate-source voltage (V_{GS}) with the drain-source voltage (V_{DS}) fixed at +0.1V. The gate voltage was scanned in the following sequence for each scan rate: −30V → 0V → +30V → 0V → −30V. The scan rates were (in mV-s^{-1}) 200(red), 100 (green), 40 (blue), 20 (pink), 10 (cyan), 4 (black) and correspond to each run respectively as indicated in the direction of the black arrow (i.e. red: 200mV-s^{-1} → black: 4 mV-s^{-1}). Red arrows indicate the counterclockwise direction of each of the device trans-conductance curves. The dotted line is the trans-conductance curve taken with a voltage applied to the Si^{+} back gate (SiO_2 dielectric) after all top gate measurements were completed. The scan rate was 200 mV-s^{-1} **Inset:** Carrier mobility (○) and sub-threshold swing (●) in V/decade calculated from the slopes of the data taken at the left side of the plots (shown within the oval) and plotted as a function of scan rates.

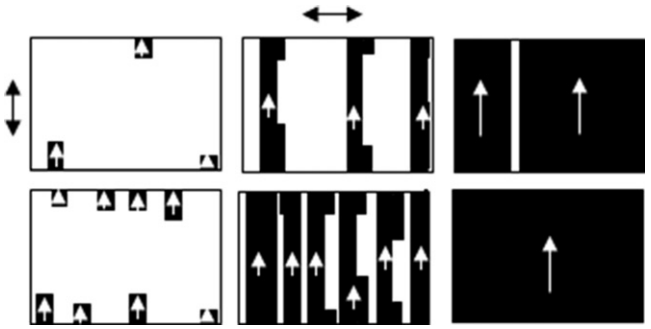

Figure 6. Schematic panels showing the progress of polarization in the FE film, beginning via nucleation, forward domain growth (↕) and then sideways domain growth (↔) until the film is polarized. The white arrow indicates the direction of polarization (external electric field not shown) within each domain. The top three panels show the same film and how polarization grows when the gate voltage scan rate is fast, and the bottom three panels show the same at slow scan rates. The rectangle represents a cross-section of the film.

scan rate that is rapid while still maintaining satisfactory device performance. In our device, we saw that a scan rate near ∼ 15 mV/s was acceptable with little additional improvement in μ and SS for slower scans.

4. Conclusions

Monolayer CVD grown MoS_2 was used as the semiconducting channel in a FE-FET with PVDF-TrFE as the gate insulator. The effects of varying the gate voltage scan rate from 200 mV/s down to 4 mV/s were investigated. Our results revealed a narrowing in the MW, an order of magnitude increase in the mobility and a decrease in the sub-threshold voltage swing at slow scans. These parameters appear to stabilize at lower scan rates suggesting an asymptotic limit to their values. They are also independent of V_{DS} although a lower V_{DS} offers the advantage of reducing overall power dissipation while maintaining satisfactory device performance. Our results were qualitatively explained by the nucleation and unrestricted domain growth model suitable for FE polymers. By lowering the gate voltage scan rate, which in turn optimizes MW, μ and SS, it should thus be possible to improve the performance of polymer based FE-FET's.

Funding

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