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Wave Propagation and Channel Modeling in Chip-Scale Wireless Communications: A Survey From Millimeter-Wave to Terahertz and Optics

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ABSTRACT The miniaturization of transceivers and antennas is enabling the development of Wireless Networks-on-Chip (WNoC), in which chip-scale communication is utilized to increase the computing performance of multi-core/multi-chip architectures. Although the potential benefits of the WNoC paradigm have been studied in depth, its practicality remains unclear due to the lack of a proper characterization of the wireless channel at the chip scale and across the spectrum, among others. In this paper, the state of the art in wave propagation and channel modeling for chip-scale communication is surveyed. First, the peculiarities of WNoC, including the design drivers, architecture, environment, and on-chip electromagnetics are reviewed. After a brief description of the different methods to characterize wave propagation at chip-scales, a comprehensive discussion covering the different works at millimeter-wave (mmWave), Terahertz (THz) and optical frequencies is provided. Finally, the major challenges in the characterization of the WNoC channel and potential solutions to address them are discussed, providing a roadmap for the foundations of practical WNoCs.

INDEX TERMS Electromagnetic propagation, millimeter wave propagation, Terahertz radiation, optical propagation, system-on-chip, multiprocessor interconnection networks.

I. INTRODUCTION

Constant downscaling of Radio-Frequency (RF) and optical circuits has recently opened the door to the design of transceivers and antennas that can be integrated within CMOS chips [1]–[4]. Although higher integration was initially driven by a need to lower fabrication costs, recent times have seen the emergence of new wireless applications where the size of the RF front-end plays a critical role. These applications are enabled by advances in nanotechnology that continue to push the limits of miniaturization, leading to very compact wireless systems in the millimeter-wave (mmWave) (30–300 GHz), Terahertz (THz) (0.3–3 THz) and optical (infrared, 187-400 THz/750-1600 nm, and visible, 400-770 THz/390-750 nm) bands.

RF technology has indeed reached a point where tens or even hundreds of transceivers and antennas can be integrated within a computing system. This allows to establish wireless links between the modules within a data center [5], [6], the different components of a printer [7] or a desktop computer [8], and even the processors and memory within a single chip [9]. In the extreme downscaling cases, the Wireless Network-on-Chip (WNoC) paradigm stands out [10] where low-latency broadcast-capable chip-scale links are established to distribute data shared among the processor cores of a multiprocessor. Beyond RF technology, major progress in the field of integrated silicon photonics [11]–[14] has similarly led to miniature

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lasers [15], [16], photodetectors [17], [18] and optical antennas [19]–[22] that enable on- and off-chip optical wireless interconnects. As an intermediate step between RF and optics, the THz band is also being considered as an enabling technology for WNoC. While the technology is not as mature as RF or silicon photonics, the THz technology gap is progressively being closed through complementary electronic, photonic and plasmonic approaches [23]–[25].

Obviously, the adoption of wireless communications in such highly integrated environments poses significant challenges in diverse aspects including transceiver front-end integration, optimal antenna placement, interference management, or data modulation and coding, in addition to protocol design. Furthermore, such aspects are highly dependent on the chosen frequency of operation. For example, the much longer communication distance of RF links and their intrinsic ability to support information broadcasting comes with the cost of higher multi-user interference and lower data-rates, whereas the higher data-rate of optical links comes with the cost of challenging broad- and multi-casting and the need for relaying. Interestingly, beyond the technology, many of these aspects arise from the nature of the wireless channel. Surprisingly, though, a proper characterization of the wireless channel at the chip scale and across the spectrum is missing.

Several fundamental differences between traditional wireless networking scenarios and WNoC motivate a tailored study of wave propagation and channel modeling [26]. Compared to the majority of wireless networking scenarios, in which usually the communication nodes and/or the scenario are mobile or change through time, in WNoC, the entire communication environment is static. As a result, the channel can be deterministically characterized and then utilized to guide the design of optimized communication solutions. For example, waveforms can designed to overcome the fixed frequency-selective response resulting from multi-path propagation through lossy medium, or spatial multiplexing strategies can be designed to minimize multi-user interference.

In this paper, we perform a comprehensive survey of existing channel modeling efforts at the chip scale. We first review the most common chip package environments in single and multi-chip configurations and the fundamental electromagnetics at the chip scale in Section II. The common methodologies and approaches to channel modeling for chip-scale networks are reviewed in Section III. Then, we survey the different works in the literature that have been aimed at studying wireless channel at the chip scales, differentiating between mmWave approaches in Section IV, THz band efforts in Section V, and optical-wireless models in Section VI. Then, we present a summary of main challenges and prospects for the field of channel characterization in chip-scale environments in Section VII and finally conclude the paper in Section VIII.

II. WIRELESS COMMUNICATIONS AT THE CHIP SCALE

Wireless chip-scale communications emerge from the need to tightly couple processing elements and memory within complex computing packages. Specifically, the wireless paradigm has been proposed as a complement to the wired interconnects to (i) improve the communication between far-apart processors, (ii) alleviate existing bandwidth bottlenecks caused by I/O pin limitations, and (iii) implement global channels. These are possible thanks to the inherent low latency, broadcast capability, and lack of path infrastructure of the wireless technology.

As illustrated in Figure 1, wireless chip-scale communications broadly refer to the implementation of intra-chip or inter-chip links with integrated antennas. In general terms, any of the components within a multiprocessor architecture (e.g. CPUs, GPUs, accelerators, memory) may be provided with a wireless transceiver that would serialize, modulate and radiate outgoing information. Electromagnetic waves propagate through the processor package until reaching the intended destinations, where they are demodulated and deserialized. Therefore, understanding the propagation process is crucial to determine the potential performance and cost of the wireless chip-scale communication.

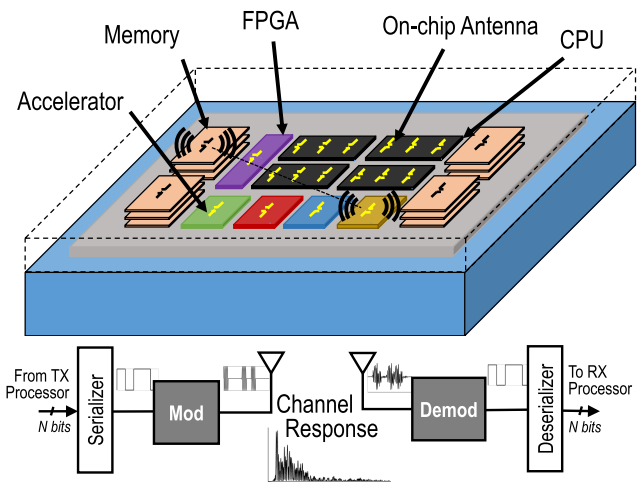
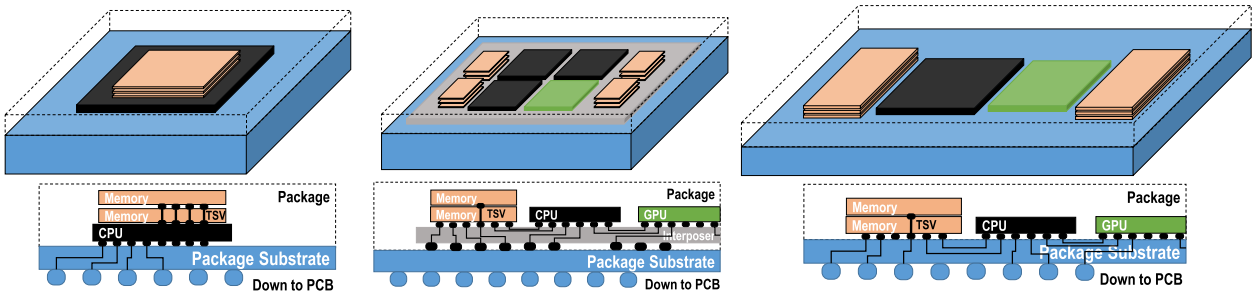


FIGURE 1. A general view on wireless communications at the chip scale within a heterogeneous computer architecture (top) with detail on the wireless transmission process (bottom).

Next, we provide background on the chip-scale environment in an attempt to gain insight on the particularities of the scenario independently of the frequency band of interest. First, in Section II-A, we review the main design drivers of multiprocessor interconnects to better understand their performance and efficiency requirements. In Section II-B, we explain the physical landscape for both single-chip and multi-chip architectures within different package flavors. Finally, in Section II-C, we discuss the fundamentals of chip-scale antennas and propagation.

A. DESIGN DRIVERS

The wireless chip-scale scenario has a unique blend of requirements and constraints that have been driving the proposals in this area and, by extension, also affect the aspects



(a) 3D integration (b) Silicon interposer (c) Multi-chip module

FIGURE 2. Different heterogeneous integration techniques in examples with CPUs, GPUs, and memory. In the wireless approach, selected components would be equipped with one or several integrated antennas to establish wireless communication links within the computing package.

related to channel modeling and characterization. We next summarize them in three main points: high performance, resource awareness, and monolithic system.

1) HIGH PERFORMANCE

Computing systems generally require very fast and reliable communications at the chip scale for two main reasons: (i) the latency introduced by communication essentially delays the progress of the computation, lagging the system, and (ii) seemingly minor errors may corrupt an entire computation. Most WNoC proposals consider wireless speeds over 10 or even 100 Gb/s to implement chip-wide latencies below 10 ns, whereas it is widely accepted that the error rate should be in the order of $\sim 10^{-15}$ [10]. Thus, an accurate characterization of the wireless channel in both the frequency and time domains becomes critical in order to achieve such stringent performance requirements.

2) RESOURCE AWARENESS

Nodes in wireless networks are typically mobile and hence have a limited battery, rendering communication largely energy-constrained. In chip environments, energy availability is guaranteed, yet energy cannot be considered unlimited since heat dissipation is expensive. Actually, power has become a driver of multiprocessor design, suggesting the use of power-gating techniques to increase the overall efficiency [27]. Similarly, chip real state is a precious resource in the scenario at hand, prompting WNoCs to employ simple and low-power transceivers that support only low-order modulations [2]. From the perspective of the channel, this forces architects to minimize path loss while increasing the frequency and looking for wide spectral bandwidths to accommodate the high requirements of data rate. Moreover, this situation also limits the signal processing techniques that could be used to combat dispersion, therefore making time-domain characterization critical.

3) MONOLITHIC SYSTEM

The propagation of electromagnetic waves takes place in a confined space. This physical landscape, including the network topology, the chip layout, and the characteristics of the employed materials, is fixed and known beforehand [26]. This represents one of the main uniquenesses of the WNoC scenario, since nodes in other wireless networks generally move within a propagation environment that can also be dynamic. The chip-scale channels, in fact, become quasi-deterministic at the data-link layer and can be accurately characterized by exploiting *a priori* knowledge of the physical landscape. This implies that the impact of decisions such as the antenna positioning or the package design can be known with high accuracy at design time. We expect that the stringent high performance and efficiency requirements of the scenario, discussed above, will only be met by introducing the wireless chip-scale network within the design loop of the complete architecture.

B. ENVIRONMENT DESCRIPTION

Diverse possible architectures and environments of chip-scale wireless communications are surveyed as follows. First, without accounting for packaging, propagation occurs in two regions: (i) the *intra-chip region*, in which the waves radiated by the antenna travel through several layers of the chip; and (ii) the *inter-chip region*, in which the waves that have left the chip travel through the inter-chip space until they reach the boundaries of another chip. The layers and materials most relevant to propagation in both regions will eventually depend on the antenna position, frequency band, and choice of package.

Second, multi-chip integration alternatives need to be considered as they impact inter-chip propagation. Currently, the integration of multiple chips can occur both vertically and horizontally. The former, *3D integration*, consists on the stacking of thinned-down chips [28]. Once stacked, the chips are generally interconnected through a forest of vertical Through-Silicon Vias (TSVs) with very fine pitch as shown in Figure 2(a). This provides a huge bandwidth density and efficiency, yet at the cost of heat dissipation issues and low available interconnect area. The *2.5D integration*, instead, takes a co-planar approach and interconnects chips through a common platform [29], [30], generally either a silicon

TABLE 1. Summary of integrated antennas amenable to the intra-/inter-chip communication scenario.

Antenna Type	Direction	Position	Characteristics	Frequency [Ref]
Printed Dipole	Horizontal	Within insulator	Easy to manufacture, but has an end-fire null	15 GHz [51], 60 GHz [50], 150 GHz [52]
Meander/zig-zag	Horizontal	Within insulator	More complex, but more compact than dipole	15 GHz [53], 25 GHz [54], 60 GHz [55]
Circular antenna	Horizontal	Within insulator	Better omnidirectionality at the chip plane	60 GHz [56], 100 GHz [34]
Vivaldi antenna	Horizontal	Within insulator	Broadband and directional, but also complex	180 GHz [57], 200 THz (optical) [58]
Bond-wire antenna	Vertical	Off-chip	Reuses bond-wiring process, but is hard to tune	20 GHz [43], 43 GHz [59], 200 GHz [60]
Vertical monopole	Vertical	Through Silicon	Coplanar radiation, embedded in lossy silicon	60 GHz [61], 120 GHz [62]
		Through dielectric	Coplanar radiation, extra packaging steps	20 GHz [63], 150 GHz [52], 160 GHz [64]
Folded monopole	Both	Through and on top	Uses vertical dimension to shorten the footprint	60 GHz [32], 77 GHz [65]

interposer [Fig. 2(b)] or the package substrate in a more classical Multi-chip Module (MCM) approach [Fig. 2(c)]. Such an arrangement alleviates the heat dissipation issue of 3D stacking and also increases the available area, as the limit is now set by the interposer or the system substrate. Due to the coarser pitch, the solution is cheaper but offers less interconnect bandwidth.

Third, system-level packaging is tightly coupled to the multi-chip integration scheme and also impacts the inter-chip propagation. The lateral space among chips may be filled with materials providing mechanical stability and the complete system may be enclosed with a common package lid or a metallic heat sink, for better thermal performance [29].

Fourth, it is crucial to understand packaging options at the chip level as they are relevant to the intra-chip propagation. Traditionally, *flip-chip packaging* and *wire bonding* have been the most common, although multiple custom variants and alternatives exist depending on the final application [31], [32]. Flip-chip packaging is generally preferred in the multiprocessor context due to its lower inductance and higher power/bandwidth density [33]. In this configuration, chips are turned over and carefully connected to the system substrate or interposer through a set of solder bumps. The packaged chip then takes the canonical form presented in Fig. 3, with the system heat sink and spreader material on top and a low-resistivity silicon substrate. The chip metallization layers are surrounded by an insulator, often silicon dioxide, which is located below the silicon [34]. In wire bonding, the insulator is left facing up (open chip) and connected to the underlying package with bond wires.

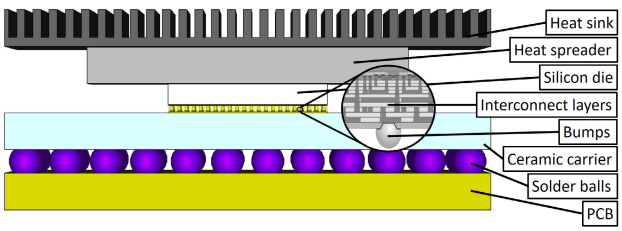


FIGURE 3. Schematic of the layers of a flip-chip package.

It is worth noting that the environment description given above is amenable to other similar scenarios such as embedded systems for intelligent metasurfaces [35], but not generalizable to all wireless scenarios within computing systems. For instance, several works have proposed models for the mmWave wireless channel within a rack [36], between racks [37]–[39] or at the cabinet scale [40] in data centers. Some papers have also covered the channel at the motherboard scale in desktops or laptops [8], [41]–[49]. Although there are structural resemblances with the wireless chip-scale environment, such models are not directly applicable here due to substantial differences in dimensions, materials, and antenna placement restrictions.

C. ON-CHIP ELECTROMAGNETICS

While the fundamental electromagnetic concepts and principles affecting antenna design and electromagnetic wave propagation are still valid in this paradigm, the chip-scale environment introduces unique requirements on the design of wireless communication systems, as we describe next.

1) ANTENNAS

The miniaturization of the largest dimension of an antenna to meet the chip-scale size requirements imposes the use of very high communication frequencies [1], [50]. In broad terms, an antenna becomes resonant at a frequency at which its length corresponds to half of the wavelength. For example, a 1-mm-long antenna is expected to resonate at approximately 150 GHz, whereas a 150-μm-long antenna would do so at 1 THz. Moreover, while traditionally it had been very challenging to fabricate structures with sub-micrometric dimensions and nanometric precision, major progress in nanotechnologies has enabled the development of precise structures comparable to the optical wavelengths and, thus, enabled for the first time the fabrication of antennas that allow us to control the radiation of light in a similar way as traditional antennas for lower frequencies have done [19]–[21]. Other aspects, both related to the antenna building material (e.g., conductivity) as well as their geometry (e.g., the proximity of a ground plane), further factor in the design of the antennas –especially in an environment as highly integrated as WNoC. Table 1 summarizes the main characteristics of common on-chip antennas for free-space applications that have been proposed for its use in the inter-/intra-chip communications domain.

Moving to higher frequencies usually opens the door to also communicating over much larger bandwidths.

Traditional narrow-band antenna designs (e.g., dipole and patch antennas) commonly exhibit a bandwidth approaching 1% of their resonant frequency. Therefore, a few GHz of bandwidth are expected for a mmWave antenna and communication system, whereas tens or hundreds of GHz are supported by a THz antenna and even more by an optical nano-antenna. Moreover, ultra-broadband antenna designs (e.g., bowtie, lognormal, spiral) offer bandwidths in excess of 10% of the carrier frequency. However, again in broad terms, the effective area of an antenna, i.e., its ability to capture the power of an incoming propagating electromagnetic wave into an electrical current in reception, decreases quadratically with the signal wavelength. Interestingly, despite being an antenna-only phenomenon, this result is in fact many times inaccurately described as a propagation loss and captured in the so-called free-space path-loss or Friis equation. There are ways to increase the effective area of an antenna, for example, by increasing its size directly (e.g., utilizing a length which is an odd multiple of half wavelength) or indirectly (e.g., through lenses or reflectors), but such increase in effective area, besides going against the original design criteria, i.e., the miniaturization of the antenna, leads to an increase in the antenna directivity, i.e., the antenna will only efficiently receive an incoming EM wave in a given direction. This again has traditionally been inaccurately reported in many works by implying that "higher frequency antennas are always directional."

2) PROPAGATION

The propagation of electromagnetic waves in chip-scale environments is governed by the same phenomena affecting those in larger scale scenarios, but with the caveat that, as in any system governed by the Maxwell's equations, we need to reconsider the entire system in light of the now much smaller wavelength of the frequency bands of interest.

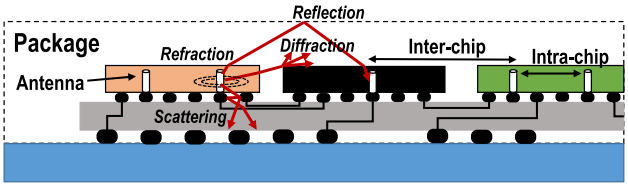


FIGURE 4. Schematic representation of wave propagation in an interposer system with flip-chip package excited with vertical monopole antennas, distinguishing between intra- and inter-chip regions, and exemplifying different propagation phenomena.

Beyond the free-space path-loss and its antenna-induced frequency-dependence, electromagnetic waves on-chip can suffer from reflections, refraction, diffraction and absorption as illustrated in Figure 4. More specifically, *reflections* will appear both when a wave reaches an obstacle (e.g., another chip or core) as well as at the interface between different material layers within one chip. The latter depend on the exact material composition and the frequency and, depending on the smoothness of the surface/obstacle (measured relative to the wavelength), can be specular (as defined by the Snell's law) or scattered. In addition, when transitioning from a medium to another, *refraction* of the electromagnetic wave will occur again depending on the change in the refraction index. *Diffraction* or bending of the wave around the (sharp) edges of chips will further determine the propagation of signals in the scenarios under study. Last but not least, mainly relevant at the higher frequencies (THz, optical bands), the *absorption* of the electromagnetic wave energy by the material needs to be taken into account. The absorption coefficient measures the distance photons (i.e., the dual particles of electromagnetic waves) travel within a material before being absorbed, and depends on the radiation frequency.

All these phenomena ultimately depend on the environment and the frequency of operation. In the following sections, after describing the different methods utilized to characterize the chip-scale wireless channel, the existing works tailored to each frequency band are described.

III. METHODS

In this section, we discuss the different methods and approaches utilized to model the chip-scale channel. We first broadly describe the methods in Sections III-A to III-D, to then analyze the main particularities and challenges when applied to the chip-scale scenario in Section III-E.

A. MEASUREMENT

Measurement-based approaches are adopted to characterize wireless propagation and generate empirical and statistical models. On the one hand, frequency-domain measurements sweep a spectrum band and record the channel transfer function. The time domain characteristic, i.e., the channel impulse response, is then obtained by inverse Fourier transform of the channel transfer function. The time resolution is determined by the measurement bandwidth while the maximum excess delay is determined by the sampling interval in the frequency domain. On the other hand, a time-domain measurement usually correlates the received sequence with the transmitted random sequence at the receiver to obtain the channel impulse response.

B. FULL-WAVE SOLVER

Full-wave electromagnetic solvers, including High Frequency Structure Simulator (HFSS), COMSOL Multiphysics, Computer Simulation Technology (CST), IE3D and FEKO, among others, involve one or more than one computational electromagnetic (CEM) methods to solve Maxwell equations with boundary conditions for computing the EM fields in a propagation medium. The CEM methods are divided into time-domain methods and frequency-domain methods, as well as integral methods and differential methods depending on the solving domain and the form of Maxwell's equations. The memory and time cost of full-wave solving increase with the simulation scale in number of wavelengths, but it varies from method to method. For WNoC, the largest dimension of the environment is up to 100 millimeters, which

is comparable with dozens of times of the wavelength of the mmWave wave and is hundreds and even thousands of times of the wavelength of THz and optical waves. As a result, the CEM method should be properly chosen according to the frequency of interest.

C. ELECTROMAGNETIC FIELD ANALYSIS

Exact mathematical solutions to Maxwell's equations can be derived under specific system considerations. The EM fields radiated by an antenna can be calculated through the Green's function of the radiation space, which we call the analytical EM evaluation. The intra-chip environment is extracted as a stratified media, and the expressions for the EM fields are the Sommerfeld integration. It should be noted that the lateral dimension of the stratified media is infinite. Therefore, the effect of the chip edge is ignored in this method. For example, the electric field of a y-directed dipole only contains the x-direction component, $E_x(\rho, z)$, which is given by [66],

$$\begin{aligned} E_x(\rho, z) = &\int_{SIP} \frac{jk_{0,z}}{\zeta^2 \rho}[A_0^h \exp(jk_{0,z}z) - B_0^h \exp(-jk_{0,z}z)] \\ &\cdot H_1^{(1)}(\zeta\rho)d\zeta \\ &+ \int_{SIP} \frac{j\omega\mu_0}{\zeta}[C_0^h \exp(jk_{0,z}z) + D_0^h \exp(-jk_{0,z}z)] \\ &\cdot H_1^{(1)\prime}(\zeta\rho)d\zeta, \end{aligned} \tag{1}$$

where ρ and z are the horizontal distance from the source to the observation point and the relative height of the observation point to the dipole. Besides, ω denotes the angular frequency of the wave. $H_1^{(1)}(\cdot)$ denotes the first-order Hankel function of the first kind, whose real part is the Bessel function of the first kind, and the imaginary part is the Bessel function of the second kind. $H_1^{(1)\prime}$ is the first-order derivative of the function, $H_1^{(1)}(\cdot)$. If ζ denotes the radial wave number in the $x - y$ plane, $k_{l,z}$ represents the wavenumber of the lth layer in the z direction, given that $k_{l,z} = \sqrt{k_l^2 - \zeta^2}$ where $k_l = \omega\sqrt{\epsilon_l \mu_l}$ is the wavenumber in the lth layer. To be specific, $k_{0,1}$ denotes the 0th layer where antennas are placed. The *SIP* denotes the Sommerfeld integral path, which runs from $-\infty$ to ∞ along the real axis, slightly above the negative real axis ($\zeta < 0$) and slightly below the positive real axis ($\zeta > 0$). In addition, A_0^h, B_0^h, C_0^h, and D_0^h are the coefficients determined by the stratified media.

D. RAY-TRACING TECHNIQUES

As a compromise between accuracy, mathematical tractability and complexity, ray-tracing techniques originated from geometric optics approaches can be utilized. As the WNoC environment consists of lossy media, the wave propagation and reflection in lossy media need to be addressed. As illustrated in Fig. 5, when transmitting in the lossy medium, the EM waves are in-homogeneous because the normals to the planes of constant phase and to the planes of constant amplitude no longer coincide. We denote direction vectors of the two normals as $\vec{e}_N$ and $\vec{e}_K$, and the angle between the two normals as γ, which equals to zero in lossless medium and larger than zero in lossy medium as shown in Fig. 5. By denoting the complex wave vector $\vec{k}$ is $\vec{k} = k_0(N\vec{e}_N + jK\vec{e}_K)$ where $k_0 = 2\pi f/c$ and c is the speed of light in vacuum, a key formula for the electric field $\vec{E}(\vec{r}, t)$ in the lossy mediums is given by [67]

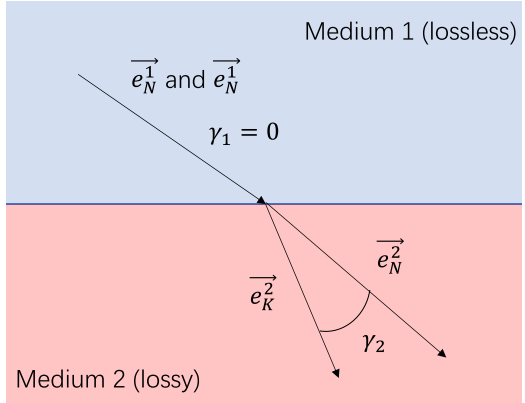


FIGURE 5. Wave propagation from lossless medium to lossy medium.

$$\begin{aligned} \vec{E}(\vec{r}, t) &= \vec{E}e^{j\vec{k}\cdot\vec{r} - j2\pi ft} \\ &= \vec{E}e^{-k_0 Kr\cos\gamma} e^{jk_0 Nr - j2\pi ft}. \end{aligned} \tag{2}$$

The complex refractive index of dielectric medium is defined as $\tilde{n} = n + jk$ with $\tilde{n}^2 = \varepsilon + j\frac{\sigma}{\varepsilon_0\omega}$, where ε and σ are the dielectric constant and conductivity of the medium respectively, and ε_0 denotes the dielectric constant of vacuum. The real and imaginary parts of the wave vector, N and K, are given by,

$$N = \sqrt{\frac{1}{2}(n^2 - k^2 + \sqrt{(n^2 - k^2)^2 + 4(nk/\cos\gamma)^2})}, \tag{3}$$

$$K = \frac{nk}{N\cos\gamma}. \tag{4}$$

The reflection coefficient R and the transmission coefficient T for TE waves are given by,

$$R = \frac{p_i - p_t}{p_i + p_t}, \tag{5}$$

$$T = \frac{2p_i}{p_i + p_t}, \tag{6}$$

where $p_i = N_i\cos\theta_i + jK_i\cos\psi_i$ and $p_t = N_t\cos\theta_t + jK_t\cos\psi_t$.

E. METHODOLOGY COMPARISON

All the channel modeling methods discussed in this section are deterministic methods. While this would be a major shortcoming for the modeling of traditional wireless networks, in which the users and the environment are generally mobile and not static, it is acceptable in chip-scale networks, in which everything is static. A comparison of the methodologies is summarized in Table 2 and detailed as follows.

TABLE 2. Methodologies channel modeling at chip-scales.

Methodology	Measurement	Full-Wave Solver	EM Field Analysis	Ray Tracing
Accuracy	High	High	Medium	Low
Computational Complexity	Low	High	Low	Medium
Examples	[68]	[69]	[70]	[71]

The channel measurement shows the highest accuracy among all the channel modeling methodologies as it characterizes the channel parameters in the real world while, in the other methodologies, the channel environments are more or less simplified under certain assumptions. However, the current channel measurements of WNoC are conducted with the transmitter and receiver antennas being exposed in the open air (without chip package) due to physical limitations. In addition, measurement results are distinct for the antenna types. Moreover, the channel measurement has requirements on the manufacturer of the chip and devices for measuring, which may not be applicable if we want to evaluate prospective intra-chip channels. Therefore, an open challenge is the development of compact probes to conduct accurate channel measurements without disrupting the chip-scale environment itself, the complexity of which further increases with frequency.

Full-wave simulations can be used to develop channel models with very high accuracy, at the cost of equally high computational demand. In broad terms, the solution provided by CEM methods is accurate if the space in which Maxwell's equations need to be solved is sampled with a resolution of approximately a fifth of the wavelength corresponding to the highest frequency of interest. While this would have been computationally intractable a few years ago, major progress in computing research and the availability of large computing clusters has facilitated this path to channel modeling.

Ray tracing, as a geometric-optical approximation method, is widely utilized for the modeling the large-scale environments, e.g., indoor WiFi scenarios and outdoor cellular networks, since it shows low computational complexity but gives reasonable results. It has been proved that ray tracing can be regarded as the first-order approximation of the theoretic solution derived from Maxwell's equations by using the saddle-point method in the stratified medium. It may converge very slow if the source and the observation point are very close to the interference between two layers. At the downside, the accuracy of ray tracing is the lowest among all the methods. Nevertheless, its accuracy increases as we move towards ray-like signal propagation, which is the case when moving towards the higher end of the spectrum (e.g., infrared and visible optics). This can be justified since ray-tracing is essentially a geometric optics (GO) method that traces the launched rays. As a far-field approach, the ray-tracing technique needs further integration of the surface wave, guided waves and lateral waves, which are the critical components in the intra-chip propagation channel.

Since the intra-chip channel can be regarded as a simple structure, e.g., a stratified medium or a micro-reverberation chamber, the expressions for the channel model can be derived analytically. For example, the green's function is a Sommerfeld integration in the planar stratified medium, while the RMS delay spread has a closed-form expression for a micro-reverberation chamber. Analytical EM analysis can provide accurate channel characteristics, and its computational complexity is lower than the full-wave simulation. Therefore, it shows advantages in the intra-chip channel analysis when changing the channel parameters, e.g., the thickness of each layer, the EM properties of each layer, or the positions of antennas, to name a few. However, small objects like solder bumps in the underfill layer and irregular metal lines of the digital circuits make the exact solution of the Green's function in the real WNoC environment an interesting challenge to address. Additionally, edge effects are intrinsically excluded in the field analysis that assumes infinitely large plane of propagation. This leads to inaccuracy of analysis results and needs to be corrected.

IV. CHANNEL MODELS FOR MILLIMETER WAVES

The study of the wireless channel at the chip scale has mostly raised interest in the last decade with the advent of mmWave integrated antennas and compact transceivers. However, the works that provided the first rudimentary chip-scale channel models dating back from the early 2000s explored the use of lower frequencies. More specifically, Kenneth K. O's group from University of Florida pioneered the field by unveiling the first measurements between integrated antennas located within the same chip at the 6–18 GHz band [51], [53], [72]. Those works not only showed the relatively high loss introduced by the channel (around 60 dB), but also discussed the potential effects of the chip package or the role of the dielectrics used for thermal aspects. The latter two aspects, however, have not been investigated again until recently.

Table 3 shows a comprehensive summary of the efforts that followed the pioneering efforts from [51], [53], [72]. It can be observed that progress in mmWave integrated antennas [50], [84] and pioneering works in WNoC [85] in the late 2000s renewed the interest in this area. Some works appeared in the 2007–2013 period, followed by a significant surge of papers from 2017 to date. Most efforts have been centered in the more mature bands between 20 GHz and 60 GHz [32], [54], [56], [59], [63], [69], [70], [73], with some forays into frequencies over 100 GHz [52], [55], [64], [79].

TABLE 3. Works containing data for the channel modeling of mmWave intra-chip and inter-chip communications.

Ref.	Year	Frequency	Method	Antenna Type	Package	Scope	Domain
[72]	2001	6–18 GHz	Measurements Ray tracing	Printed dipole	Open chip Flip-chip	Intra-chip	Frequency
[51]	2002	10–18 GHz	Measurements	Printed dipole	Open chip	Intra-chip	Frequency
[53]	2005	15 GHz	Measurements	Printed dipole	Flip-chip	Intra-chip	Frequency
[68]	2007	10–110 GHz	Measurements	Printed dipole	Open chip	Intra-chip	Frequency, time
[59]	2009	30–55 GHz	Measurements	Bond-wire antenna	Bond wires	Inter-chip	Frequency
[54]	2009	16–30 GHz	Measurements	Printed meander	Open chip	Intra-chip	Frequency
[70]	2009	15–140 GHz	EM Field Analysis	Dipole (model)	Open chip	Intra-chip	Frequency
[32]	2013	50–70 GHz	Measurements	Folded monopole	Custom over flip-chip	Inter-chip	Frequency
[73]	2015	55–60 GHz	Full-wave solver	Printed Dipole	Open chip	Intra-chip	Frequency
[63]	2016	17–27 GHz	Full-wave solver	Vertical monopole	Flip-chip	Inter-chip	Frequency
[74]	2016	10–90 GHz	Full-wave solver	Vertical monopole	Custom over flip-chip	Intra-chip	Frequency
[75]	2017	0–80 GHz	Full-wave solver	Zig-zag monopole	Custom open chip	Inter-chip	Frequency
[76]	2017	60 GHz	Full-wave solver	Loop antenna, PLPA	Open chip	Intra-chip	Time
[52]	2017	130–170 GHz	Full-wave solver	Vertical Monopole	Custom enclosing	Intra-/Inter-chip	Frequency, time
[64]	2017	155–165 GHz	Measurements	Vertical Monopole	Custom enclosing	Intra-/Inter-chip	Frequency
[77]	2018	55–65 GHz	Full-wave solver	Folded dipole, PLPA	Open chip	Intra-chip	Frequency, time
[55]	2018	155–165 GHz	Measurements	Vertical Monopole	Custom open chip	Intra-chip	Frequency
[69]	2018	60 GHz	Full-wave solver	Patch, vertical monopole	Flip-chip	Intra-chip	Frequency
[78]	2018	60–120 GHz	Full-wave solver	Vertical Monopole	Flip-chip	Intra-/inter-chip	Frequency
[79]	2018	60–120 GHz	Full-wave solver	Vertical Monopole	Flip-chip	Intra-chip	Frequency, time
[56]	2018	56–67 GHz	Measurements	Dipole, circular patch	Custom over flip-chip	Inter-chip	Frequency
[80]	2018	26–50 GHz 150–250 GHz	Measurements Full-wave solver	Dipole Vertical monopole	Open chip	Intra-chip	Frequency
[81]	2019	40–60 GHz	Measurements	Dipole	Open chip	Intra-chip	Frequency
[82]	2019	50–60 GHz	Measurements	Printed dipole	None (surface-wave)	Inter-chip	Frequency
[61]	2019	60–70 GHz	Full-wave solver	Vertical monopole	Custom	Intra-chip	Frequency
[35]	2019	60–180 GHz	Full-wave solver	Vertical monopole	Custom	Intra-/inter-chip	Frequency, time
[83]	2019	10–40 GHz 50–70 GHz	Measurements Full-wave solver	Zig-zag monopole	Custom open chip Flip-chip	Intra-/inter-chip	Frequency

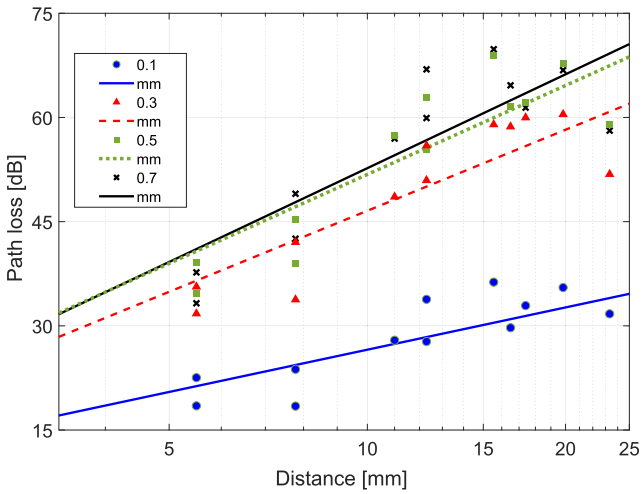


FIGURE 6. Path loss due to intra-chip propagation within a flip-chip package at 60 GHz with variable silicon thickness, heat spreader of 0.2 mm, and heat sink on top (reproduced from [79]).

A. FREQUENCY DOMAIN

Frequency domain analysis has driven most of the efforts, highlighting the importance of path loss in the feasibility of chip-scale links. The pioneering works of [51], [72] clearly showed that wireless links within standard chips and packages have very large attenuation on the order of 50 dB or more for several millimeters distance, which is a clear roadblock. Full-wave simulations of a standard flip-chip package, reproduced in Figure 6, confirmed that path loss can exceed 70 dB for a few centimeters distance. To put such figures in context, recent on-chip mmWave transceivers with reasonable efficiency (2 pJ/bit in [2]) considered an attenuation of 26.5 dB between transmitter and receiver.

Subsequently, Zhang *et al.* [68] tested high-resistivity silicon as a way to reduce losses induced by the lossy substrate. This method achieved improvements of around 20–30 dB and has been adopted by Yan and Hanson [70] or El-Masri *et al.* [80], [81]. It was further learnt from [68] that metallic interferent structures in the form of normal or parallel strips located between the transmitter and receiver can enhance the band pass characteristic of the intra-chip propagation channel, reducing losses by a few dB.

Non-standard packages have been also proposed in an attempt to minimize or eliminate the impact of lossy silicon. For instance, the authors in [73] reduce attenuation to 15–30 dB using a layer of undoped silicon below the die substrate. Further, the works in Melde's group at University of Arizona [32], [56] resort to metamaterial-like structures in open chip schemes to enhance the coupling of surface-waves and reduce amount of energy radiated away from the chip and into the silicon. Similarly, several variants of a vertical monopole partially or completely inserted within a dielectric waveguide have been proposed [35], [61], [74], achieving outstanding results with less than 10 dB losses at times. Notably, Wu *et al.* [64] propose a 3D-printed optimized dielectric attempting to jointly optimize several links within a single package.

Most of the efforts to reduce the path loss have achieved their objective resorting to non-standard processes. The improvement of high-resistivity silicon comes at the cost of worse performance in digital circuits, whereas the use of some proposed waveguiding techniques adds several manufacturing and custom packaging steps, which is undesirable. Thus, there has been also a renewed interest in solutions compatible with standard packages. In this direction, Timoneda *et al.* have evaluated the impact of optimizing the silicon and thermal interface material thicknesses in TSV-based links within a flip-chip package [78], taking chip-wide losses close to 30 dB (see Figure 6 for partial results). In that work, it was also discussed that the metallization layers within the chip or the interposer would likely block the signals due to the small pitch of such layers when compared to the transmission wavelength. Related to this, it has been demonstrated that the path loss exponent in the optimized cases is between 1 and 1.4, which confirms the waveguiding effect of the whole flip-chip package. Finally, it is worth noting that other aspects such the antenna orientation or placement also have an impact [77] in ways compatible to standard packaging.

B. TIME DOMAIN

While it seems that the path loss has reached levels ensuring a reasonable efficiency, little has been reported about the dispersive nature of the intra-/inter-chip wireless channels. This is of crucial importance as dispersive channels limit the symbol rate used in the transmissions which, coupled to the simple low-order modulations expected for this scenario, could be a hard constrain in the achievable data rate.

In their theoretical work, Matolak *et al.* predicted worst-case values of several nanoseconds using the micro-reverberation chamber model at mmWave and THz frequencies [26]. First measurements of the power-delay profile of open chip schemes, on the contrary, yielded delay spread figures on the order of 100 ps for transmissions at 30–60 GHz [68]. This is because the reverberation chamber model assumes full encasement and does not take dielectric losses into account, thus increasing the importance of the reflections. For flip-chip and custom packages, which fall in between these two extremes, the simulated delay spread has been of a few hundreds of picoseconds [35], [52] (see Figure 7 for a partial reproduction of data from [79]). In this context, it may not be possible to provide the speeds of several tens of Gb/s promised in several works [10], since the coherence bandwidth would be around a few GHz at most.

Since the channel is quasi-static and quasi-deterministic, time-domain results deliver insight on the chip-scale propagation mechanisms. For instance, the measurement results from [68] on an open chip show that the first signal peak is found significantly later than that of free-space propagation, which suggests the surface waves along the air-wafer interface dominate. Within flip-chip structures, it can be proven that most dispersion comes from the reflections that signals suffer at the different interfaces within the package.

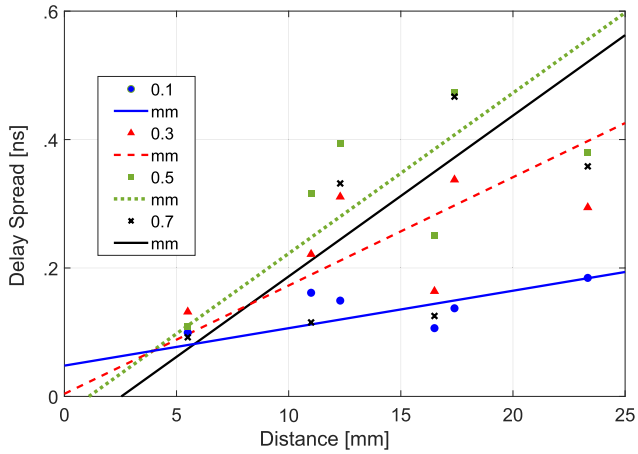


FIGURE 7. Delay spread in the intra-chip channel at 60 GHz within a flip-chip package with variable silicon thickness, a heat spreader of 0.2 mm, and heat sink on top (reproduced from [79]).

Therefore, waveguide-like and enclosed structures are equally crucial to minimize delay spread just as they are indispensable for path loss. Having this in mind, Timoneda *et al.* proposed to optimize the flip-chip package taking dispersion into account [79]. For instance, it was shown that thinning down the silicon can have a positive effect on the delay spread, as shown in Figure 7. With more exhaustive explorations, the authors were able to reduce the worst-case delay spread below 100 ps while maintaining a reasonable path loss, ensuring a chip-wide coherence bandwidth over 10 GHz.

C. CHANNEL MODELING METHODS

From the perspective of the channel modeling method, EM field analysis has been only utilized in the work by Yan *et al.* [70]. With numerical methods over field integrals, the authors obtained the field distributions of a Hertzian dipole over an open chip at 15–90 GHz. Moreover, different combinations of layers emulating the thermal dissipation material or a custom dielectric waveguides were analyzed following the discussions from [51], [72]. It was concluded that, depending on the frequency, the surface-wave mode could be important and that the waveguiding layers can deliver important enhancements. Besides this and the micro-reverberation and two-ray models proposed in [26], most works have focused on full-wave solving and actual measurements. Due to the relatively reduced size of the environment at mmWave frequencies, there have been no serious attempts at using ray tracing in this band [62].

From the perspective of the considered antenna, there has been a shift from printed dipole and its variants [68], [75] aiming to facilitate the fabrication and measurement of samples, to a set of research groups that have considered vertical monopoles through-silicon [61], [69] or through other dielectrics [52] in full-wave simulation studies. Package-wise, open chip or custom packages have been evaluated most frequently [54], [68], [76] for the same reason and despite of the pioneering remarks on flip-chip package compatibility made in early stages of this research area [51]. However,

there has been a recent surge of works considering schemes compatible with flip-chip packages [63], [79], [83], which have been mostly based on full-wave simulation due to the cost of instrumenting flip-chip packages. Finally, bond-wire antennas/packages [59] have been less relevant given the widespread use of the flip-chip.

V. CHANNEL MODELS IN THE TERAHERTZ BAND

Compared to RF and mmWave technology, THz technology is still at its infancy. More specifically, despite the major progress in the recent decade, the development of on-chip, compact and energy efficient THz signal modulators and detectors and ultra-broadband modulators and demodulators is still an open challenge. Nevertheless, beyond traditional electronic and photonic approaches [23], [24], the utilization of new materials such as graphene [86] and the exploitation of new physics including plasmonics [87] is enabling the development of miniature on-chip direct THz sources and detectors [88], [89], modulators and demodulators [90], [91] and antennas [92], [93] that can be utilized in WNoC. Motivated by these results, there has been a raising interest in the concept of on-chip THz communications and, as a result, a few pioneering works on channel modeling can be found in the related literature.

Lee *et al.* simulate the intra-chip channel where antennas are placed in a polyimide layer in an open chip scheme, by using a full-wave solver, HFSS, at 300 GHz [94]. The authors report an attenuation of around 40 dB at 1 cm distance, and argue that, compared with a conventional on-chip antenna over silicon, the on-chip antenna placed in the low-loss dielectric polyimide layer improves the channel loss by 20-30 dB.

As one of the first attempts for THz chip-scale propagation modeling, Chen *et al.* analyze the EM fields by using the Sommerfield integration method in the CMOS chip, and the results are validated with the full-wave solver HFSS [95]. As main observations, the path loss is highly frequency-selective due to the surface wave and guided wave propagation, as presented in Fig. 8. The path loss is periodically oscillating in the THz band, for which the period is corresponding to the frequency between two adjacent surface wave modes. In this work, the impact of the chip design is analyzed, and chip design guidelines with the potential to improve the WNoC channel are provided. The thinner underfill layer and inserting a bottom layer between the silicon substrate and the heat sink are able to enhance the path gain. In addition, the thickness of the silicon substrate has a great impact on wave propagation, and it needs to be selected carefully according to the operating frequency.

In [26], a two-ray model is utilized to estimate the path loss in an intra-chip channel, which includes the line-of-sight path and the path reflected from the plane where the transmit and receive antennas are located. Below the breakpoint $d_b = 2\pi h_T h_R/\lambda$ where h_T and h_R are the heights of the transmit and receive antennas, the path loss exponent is 2. Beyond the breakpoint, the path loss exponent increases to 4.

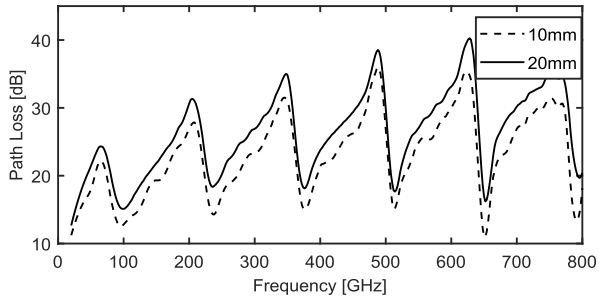


FIGURE 8. Path loss of the THz chip-scale wireless channel (reproduced from [95]).

On the one hand, the path loss is linearly proportional with the transmission distance in the log scale for frequencies under 10 THz and antenna heights smaller than 100 μm. On the other hand, when the frequency increases to 100 THz, the log-scale path loss is highly distance-selective over the range from 10^{-5} to 10^{-2} m. The validity of this model, however, needs to be confirmed for different packaging schemes other than open chip.

Recently, Chen *et al.* developed a multi-ray model by using the ray-tracing method for intra-chip channels within flip-chip packaging structures in the THz band (0.1-1 THz) [71]. Based on the developed channel model, observations can be drawn as follows. First, the intra-chip channel is highly frequency-selective due to the multi-path effect, although the molecular absorption does not exist in the chip. Second, the high-resistivity substrate results in a large delay spread, and thus narrow coherent bandwidth. This is owing to the fact that paths with longer time of arrivals suffer less attenuation in the substrate. Third, the capacity of the intra-chip channel can reach 150 Gbps and 1 Tbps with BER below 10^{-14} when the transmit power is 1 dBm and 10 dBm, respectively, and the transmission distance is 40 mm.

VI. CHANNEL MODELS IN THE OPTICAL SPECTRUM

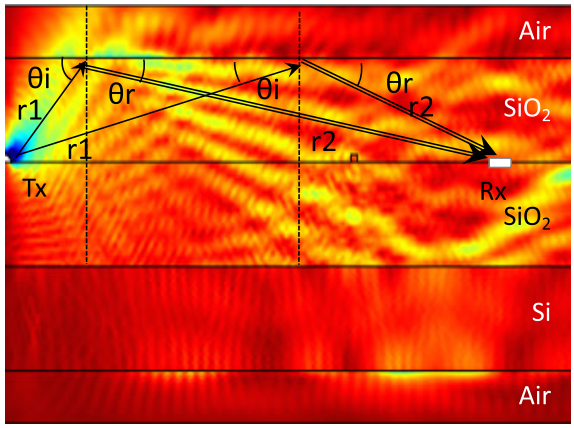
Moving up in the spectrum, the optical frequency bands, namely, infrared, visible and, to a lesser extent, ultra-violet frequencies, enter into consideration. Compared to THz technology, the wide adoption of fiber optical systems in wired telecommunication networks has led to the development of compact and energy efficient silicon-compatible lasers and photodetectors [11], [12]. In the last decade, the field of silicon photonics has further led to non-traditional ways to modulate light on-chip (e.g., on-chip Orbital Angular Momentum laser [96]) and even to fully optical processors [11]. Given that light is already utilized for intra-chip and inter-chip wired communications, the possibility to reuse some of the existing components to enable wireless optical communications in WNoC has recently been considered.

In [97], a wireless optical link for inter-chip communication is designed by means of full-wave electromagnetic simulations. The focus of the paper is on designing optical Yagi-Uda directional antennas and their matching network to an optical waveguide and on studying the benefits of

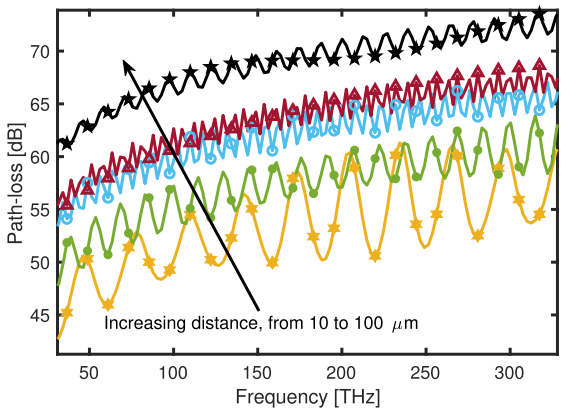
directional optical wireless links when compared to both waveguided modes and omnnidirectional optical links. The distance considered in the analysis is in the order of tens of µm. The work does not include a channel model *per se*, and the peculiarities of chip-scale communications, with the exception of the size of the antennas, are not taken into account. Similarly, in [98], a nano-patch antenna fed by a plasmonic waveguide is designed for broadband operation at near- and mid-infrared. Full-wave electromagnetic simulations are utilized to numerically optimize the design. In [99], an on-chip plasmonic horn nano-antenna is designed and its performance in terms of radiation efficiency and broadband nature is evaluated through full-wave electromagnetic simulations. Still in the context of optical nano-antenna design, but instead by following a fully analytical approach, in [22], the performance in transmission and reception of optical nano-antennas is studied. Fundamental limits on the radiation efficiency and effective area of optical dipole nano-antennas are derived, and the impact of optics-only properties, such as the complex-valued electrical conductivity of metals at optical frequencies, on the generation of Surface Plasmon Polariton waves and, ultimately, on the achievable radiation efficiency, is explored. Other antenna-focused works include [100], where waveguide-fed Vivaldi antennas are designed and their performance in an optical wireless link on chip is investigated through full-wave numerical simulations.

The first attempt at analytically modeling the intra- and inter-chip optical wireless channel was conducted in [101]. In this work, the channel response in the frequency domain was analytically derived and numerically validated through full-wave simulations by taking into account the impact of absorption by silicon, reflection and refraction at the chip material layers, and reflection and diffraction around the edges of the optical transmitters and receivers [Figure 9(a)]. The results show path-loss approaching 100 dB for distances in the order of 100 µm [Figure 9(b)]. Longer communication distances could be achieved, for example, by means of the aforementioned directional optical antenna designs [97], [99]. As opposed to analytical and full-wave numerical models, a ray-tracing approach is followed in [102], showing similar results and performance bounds.

Another aspect that has been recently given attention to is the role of multi-user interference and spatial multiplexing of directional optical links. Compared to the mmWave and, to a lesser extent, the THz band, the much smaller size of the antennas allows multiple of them being integrated per chip and potentially utilized simultaneously over different spatial beams. In [103], [104], the authors investigate both mutual coupling between neighboring optical antennas as well as the impact of interference on the achievable bit error rate. As we discussed in Sec. II-B, optical antennas can be designed to behave as directional or omnidirectional radiators, depending on the target communication distance in the specific application on-chip. While mainly theoretical for the time being, the fundamental understanding and models are ready for the communication and networking protocol designers to leverage.



(a) Full-wave electromagnetic simulation of a wireless link on-chip



(b) Path-loss for different distances between transmitter and receiver

FIGURE 9. On-chip optical channel modeling (reproduced from [101]).

VII. CHALLENGES AND PROSPECTS

In this section, we discuss the main challenges and prospects relative to the channel characterization of wireless chip-scale networks.

The first outstanding challenge refers to the availability of affordable methods for the probing of chip-scale environments to measure the chip-scale channels. Experimental results are limited to the lower part of the spectrum and assuming planar antennas in open chip configurations that are easier to manufacture and access, with few notable exceptions [64]. Testbeds for the measurement of THz and optics channels or within flip-chip packages are not publicly available at the time of this writing, thus rendering the existing simulation campaigns incomplete.

At the mmWave bands, one of the main impairments for communication is the presence of a thick layer of lossy silicon. Unacceptable attenuation over 50 dB has been measured even for distances of a few centimeters. To address this issue,

the research community will need to leverage the monolithic nature of the system beyond existing works that optimize the package dimensions as functions of path loss or delay spread objectives [79], introduce additional layers of undoped silicon [73], metasurface-like absorbers [63], or directly adds a custom dedicated channel for wireless propagation [35]. Another way to combat losses is through increasing the directivity, even if that means loss of the broadcast advantage. In this respect, antenna arrays are prohibitive due to the relatively large wavelength, unless opportunistic solutions are found [105]. Compact directive antennas such as planar log-periodic antennas have been also proposed [106], but also with limited improvement in directivity. Related to this aspect, the modeling of the interference between directional antennas remains relatively unexplored in the mmWave band.

As we approach the THz band, channel characterization via measurements becomes challenging due to the scarcity of dedicated testbeds for THz wireless communications. While the field has largely evolved since the very first THz communication testbed at 300 GHz [107] to the state-of-the-art platforms at 1 THz [108], the latest being now able to transmit user-defined bits in custom frame structures with a myriad of modulations over a 40 GHz bandwidth, the overall size of transmitter and the receiver make on-chip channel characterization very challenging. Even though test chips and equipment of THz imaging can be partially re-used for wireless channel sounding, the usable bandwidth in this case is relatively small. More critically, by considering the size of a THz spectroscopy platform, the sub-millimeter wavelength and the propagation distance in the chip environment, near-field effects become rather challenging to be measured and separated from antenna responses. Furthermore, as the effective area of the antenna diminishes, finding THz signal over the noise floor becomes difficult especially in a challenging environment such as the chip. In light of these issues, computation methods are required. However, since the chip scale is relatively large in terms of THz wavelengths, full-wave solving can be very computationally intensive, thereby highlighting the need for robust ray tracing methods that account for the particularities of the scenario. One problem that can be worth exploring, for instance, is the potential leakage of THz signals through the space between solder balls that connect the chips with the outer world. This could be seen as not only a transmission efficiency loss, but also a security threat as nearby attackers could eavesdrop or introduce signals.

At optical frequencies, measurements of the transmission channel may be possible thanks to recent advances in the fabrication and integration of optical devices with light sources at the chip scale [109]. Although these works target optical NoC based on integrated waveguides and ring resonators, the coupling of such devices with optical antennas is feasible. Beyond the feasibility of experimental setups, however, the modeling of the environment is an open challenge in the characterization of the optical wireless channel. The antennas are located within the insulator, close to the rest of metallization layers that make up the processor circuits. Even assuming clear line of sight between the antennas and directional radiation, part of the antenna energy will be beamed to slightly tilted directions and impact on the metallization layers. At mmWave/THz frequencies, the radiation wavelength is larger than the pitch of the metallization layers and, thus, they could be modeled as solid blocking elements. At optical frequencies, though, the radiation wavelength is commensurate to the pitch of the metallization layers and, therefore, scattering/diffraction phenomena are bound to occur. The main challenge here is how to model the maze formed by the wires routed through the different layers. Post-layout simulations of the processor chip, if such information is available, or X-ray imaging of actual fabricated chips [110] can provide inputs for such model. Although this simulation method does not scale well due to the computational cost of recreating such an environment at a micrometer granularity, the results at very short distances can be useful when incorporated to interference models that currently do not evaluate the scattering/diffraction phenomena [103], [104].

VIII. CONCLUSION

In this paper, we have first reviewed the fundamentals of on-chip electromagnetics across the spectrum, from mmWave and THz band to optical frequencies, and surveyed the state of the art in wave propagation and channel modeling for WNoC. This allows the research community to better identify the challenges and propose potential solutions towards channel modeling in WNoC, which is a necessary step on the quest to realizing this transformative computing paradigm. We have argued that while the starting point is the same, i.e., Maxwell's equations, there are fundamental differences in the resulting channel models when changing the carrier frequency/wavelength over four orders of magnitude (from 30 GHz up to 300 THz or, equivalently, from 10 mm down to 1 μm). At mmWave frequencies, the relatively much larger size of antennas limits the number of antennas that can be integrated per chip. In addition, while much higher propagation distances lead to seamless interconnection across chips, node multiplexing across time and frequency is needed to overcome interference. On the opposite end of the spectrum, the need for directional optical antennas to close a link beyond one chip enables spatial multiplexing of nodes. However, the impact of every element in the chip (from the material layers to the imperfections) on signal propagation, leads to predictable but still unwanted multi-user interference. As a trade-off between the two, the THz band, if properly accounted for, can lead to the best of the two realms, by allowing spatial multiplexing while advantageously propagating on-chip compared to optics.

A similar discussion can be held when comparing the available bandwidth and potential data-rates across the spectrum. The much lower available consecutive bandwidth at mmWave frequencies (up to 10 GHz) and the need for time/frequency

multiplexing of users can limit the performance of the network, except for those cases in which highly parallelized computations are conducted and, thus, as opposed to interference, advantageous propagation is leveraged for broad- and multi-casting of information. The THz band channel, instead, offers bandwidths in excess of 100 GHz, drastically increasing the information capacity of WNoC. While it is true that at optical frequencies the bandwidth is even larger, currently, there are no efficient ways to leverage it due to mainly the relatively low speed of optical modulators (able to support modulation bandwidths of up to tens of GHz), which is limiting not only the achievable data-rates on chip, but also that of any wired (fiber optical) link. Therefore, once again, the THz band appears as a reasonable trade-off between size of the antennas, propagation distance and capacity. Of course, the challenge that the THz band has to overcome is the technology gap itself, which has traditionally discouraged the communication community to enter the field. However, as highlighted throughout the paper, THz technology is drastically evolving and is only a matter of time to have compact on-chip THz transceivers and antennas.

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