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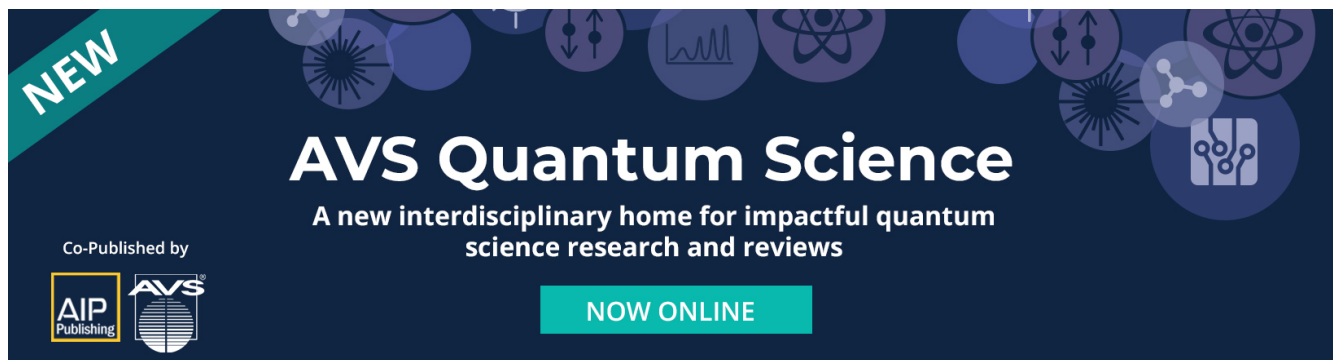
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High-yield fabrication method for high-frequency graphene devices using titanium sacrificial layers

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The authors present a fabrication process for the development of high-frequency (>30 GHz) on-wafer graphene devices with the use of titanium sacrificial layers. Graphene patterning requires chemical processes that have deleterious effects on graphene resulting in very low yield. The authors prevent delamination of the delicate graphene from the substrate during the fabrication steps by depositing a blanketing 30 nm titanium layer at the beginning of the process. Additionally, titanium is a low cost, hazardless, and well-established material in the semiconductor industry and, therefore, constitutes an attractive solution for graphene protection. With the proposed blanketing approach, the authors obtain more than 90% device yield, allowing the development of graphene-based reconfigurable, large-area, high-frequency topologies such as antenna arrays. Without the use of this titanium sacrificial layer, they show that the expected yield plummets. In addition, they validate the proposed fabrication procedure through on-wafer measurements in the 220–330 GHz range. *Published by the AVS.* <https://doi.org/10.1116/1.5098324>

I. INTRODUCTION

A significant research effort has been devoted to developing dynamically reconfigurable millimeter-wave/terahertz (mmW/THz) devices (operating in the 30 GHz to 1 THz frequency range) that has led to various novel configurations for both imaging and communication applications.^{1–17} In general, reconfigurability is achieved using tunable capacitors,¹ diodes,² and tunable materials^{3,4} (e.g., indium tin oxide). In recent years, an increased research effort has been steered toward reconfigurable switches and other devices that exploit the tunable electromagnetic properties (e.g., conductivity) of 2D materials, including graphene and molybdenum disulfide (MoS₂).^{5,6} These materials exhibit reconfigurable properties that are regulated with the use of external biasing, as in the case of field-effect-transistors.⁶ Moreover, these materials are very attractive for broadband applications, since their tunable properties are expected to be uniform across the electromagnetic spectrum.^{6–11} Nonetheless, most of the works concerning the development and fabrication of radio-frequency (RF) graphene devices are either limited to low frequencies (<100 GHz)^{6–8} or used for terahertz “out-of-plane” propagation^{9–11} applications. Furthermore, the graphene sheet resistances reported in these works reflect either single frequency responses or averaged values, thus concealing the actual graphene properties over a broad range of frequencies.

Herein, we focus on “in-plane” topologies where electromagnetic waves travel across the devices (e.g., transmission lines), in contrast to “out-of-plane” devices where waves travel through the structure (e.g., lenses). In-plane devices are commonly integrated into antenna arrays’ RF-front-end networks and are used to feed the antennas using a complex network of components including switches, phase-shifters,

and power dividers.¹⁶ To achieve reconfigurability of these components, topologies including graphene have been proposed;^{17,18} however, they are predominantly studied using full-wave simulations and theoretical models, due to the challenges in the fabrication and on-wafer characterization. Specifically, to implement graphene-loaded, large-scale reconfigurable antenna arrays of hundreds or even thousands of elements, high-yield fabrication processes are needed. However, the delicate nature of graphene often leads to its delamination from the substrate during standard nanofabrication processes, including development and lift-off. Therefore, the proliferation of large-scale graphene devices for RF applications is hindered.

Another important challenge toward developing on-wafer RF graphene devices is metal losses. Namely, to achieve low losses in these wavelengths, the metal thickness should be larger than the skin depth.¹⁶ Specifically, in the case of RF-front-end networks that are used to feed antenna arrays, the circuitry can extend up to a few millimeters; therefore, to obtain high-frequency, low-loss reconfigurable devices, we need to use thick metallic layers. For example, at 300 GHz the skin depth of gold (Au) is 140 nm; hence, the Au thickness for a 300 GHz transmission line should be at least 280 nm to avoid excess ohmic losses. However, developing thick metal layers (>0.3 μm) with integrated graphene patches is nontrivial, due to the compatibility of graphene with the chemicals used during the fabrication steps. To fabricate thick metal layers, it is preferable to use double layer lift-off photoresists to achieve fine resolution with higher yield and easier processes;¹⁹ however, the chemicals used during this process (e.g., PG Remover or 400 T) significantly increase the risk of graphene delamination.

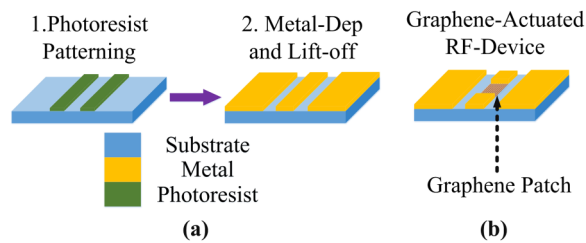


Fig. 1. (a) Steps for fabricating a metal CPW line using standard nanofabrication procedures. (b) Graphene-actuated RF-switch.

In Fig. 1(a), we depict the steps for the fabrication of coplanar-waveguide (CPW) transmission line using thick metal layers: (1) spin coat a double layer photoresist (3–4 times the metal thickness), pattern it using photolithography followed by development and (2) deposit a metal layer using electron-beam evaporation deposition (EVD) and pattern it using lift-off. The aforementioned process is a well-known procedure used for the development of high-frequency passive RF devices. On the contrary, in Fig. 1(b), we present a graphene-actuated RF-device configuration with a graphene patch intersecting the center conductor of the CPW. To develop this configuration, we have to cover the substrate with a delicate graphene sheet and then pattern the metal topology using the aforementioned steps. However, the wet processes of development and lift-off used for metal patterning often lead to graphene delamination due to its delicate nature.^{20,21} This becomes a significant roadblock for large-format arrays of devices, including reconfigurable metasurfaces and phased arrays (e.g., Refs. 2, 3, 14, and 15), where yield is crucial.

In this work, we propose a high-yield fabrication procedure that uses titanium (Ti) sacrificial layers to cover graphene during the fabrication procedure and prevent delamination. In addition, using Ti layers cleans the graphene monolayer leading to intrinsic performance.²⁰ Hence, we are able to develop large-scale mmW/THz graphene reconfigurable devices using a high-yield fabrication process. A similar procedure using yttrium (Y) sacrificial layers has been proposed recently;²¹ although this previous work presents promising results, the use of a rare element like Y is not compatible for the development of a high-yield, high-throughput standardized process. Namely, such processes demand low-cost materials, but Y is typically six times more expensive than Ti. In addition, Ti is a well-known material used in industrial procedures; hence, no adaptation is needed for the existing equipment to the new material properties (melting point, sputtering profiles, etc.). Moreover, the fabrication residues of Y and its oxides are damaging to human health and the environment in contrast to Ti.^{22,23} Hence, we selected Ti instead of Y as a sacrificial layer for our high-yield fabrication process.

II. PROPOSED FABRICATION METHOD

The fabrication process we follow to develop the graphene devices is illustrated in Fig. 2. Initially, we clean the high resistivity ($>10\,000\,\Omega\,\text{cm}$) silicon wafer that serves as the substrate and is commonly used in high-frequency RF

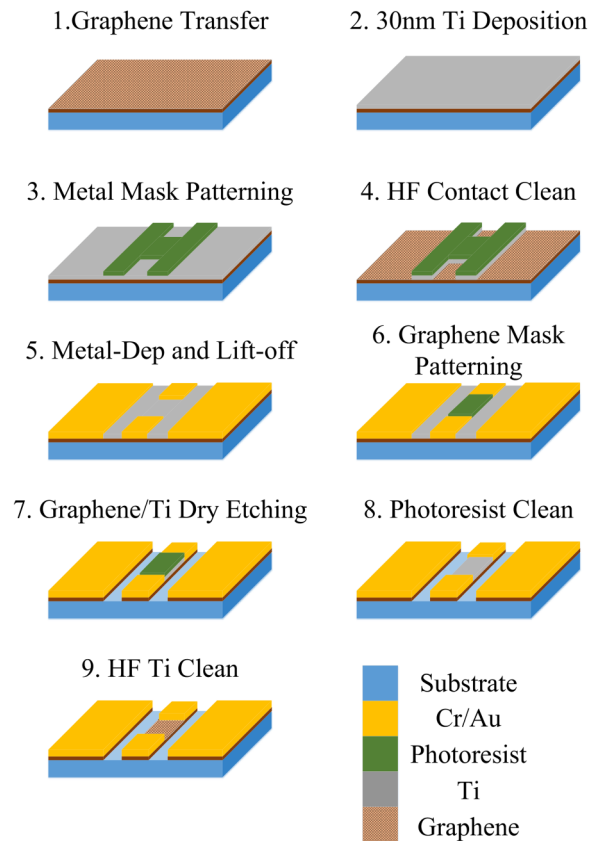


Fig. 2. Proposed fabrication procedure for the development of on-wafer mmW/THz graphene devices with a Ti sacrificial layer to protect the graphene.

applications, using a 1:10 hydrofluoric acid (HF):deionized (DI) water solution. In this step, we remove the native oxide layer of the silicon surface before the graphene transfer and passivate the silicon surface with hydrogen (H) atoms. The advantages of this clean are twofold. Firstly, the H-passivated surface minimizes the effects of the graphene-silicon interaction leading to intrinsic graphene performance.²⁴ Secondly, the native oxide of silicon is hydrophilic;²⁵ hence, by removing and replacing it with a hydrophobic H-passivated surface, we minimize the risk of delaminating the transferred graphene monolayer during the wet processes. In addition, transferring the graphene onto a hydrophobic surface hinders doping and other effects that undermine the graphene performance.²⁶ After the cleaning is completed, we transfer a graphene monolayer onto the silicon substrate using wet transfer²⁷ (this step was carried out by ACS Materials²⁸). The full processing steps in our new method are illustrated in Fig. 2. The Raman spectrum of the graphene monolayer on high resistivity silicon is shown in Fig. 3 (acquired on a WITec alpha300R system with 532 nm excitation laser) and shows the clear G and 2D peaks for monolayer graphene, and no D peak suggesting that there are very few defects. After the processing steps, both the 2D and G peaks are slightly shifted toward lower wavenumbers, suggesting a lower degree of doping.²⁹ In addition, the widths of both peaks have slightly increased, which can be associated with an increase in the spatial variation of doping.²⁹

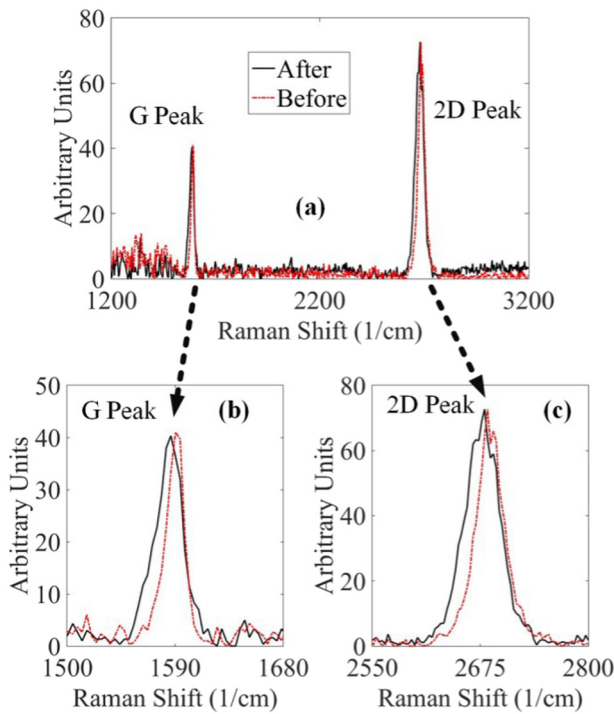


FIG. 3. (a) Raman spectra of the graphene monolayer acquired before and after the fabrication procedure focusing on the (b) G and (c) 2D peaks (60 s total accumulation time).

Even though the wet transfer procedure is robust, due to the use of poly(methyl methacrylate), residual polymer, and other particles tend to adhere to the graphene monolayer leading to deteriorated performance.²¹ Hence, using a Ti sacrificial layer also helps remove those residual contaminants and achieve intrinsic performance.²⁰ After the transfer is completed, we deposit a 30 nm Ti sacrificial layer using EVD at a rate of 1 Å/s (chamber pressure less than 5×10^{-7} mTorr). We used a reasonably thick (>20 nm) blanketing layer to ensure uniform coverage, thus minimizing graphene exposure to the strong chemicals used during the fabrication procedure that might lead to its delamination. This step could also be carried out at the beginning of the process, before the graphene monolayer transfer.³⁰ Then, we spin coat the double layer photoresist (MIR-701 and LOR-10A) for the metal mask on the wafer, expose at 63 mJ/cm^2 using 365 nm light, and develop using AZ-300MIF (45–60 s). The two layers of the photoresist develop in different rates in the base solution, creating an undercut that is necessary to perform the lift-off process that follows.¹⁹ Afterward, to clean the Ti from the metal contact areas, we submerge the wafer in a 1:72 HF:DI water solution for 2 min.

Next, we deposit the Cr/Au (10 nm/300 nm) metal layer with a rate of 1 and 1.4 Å/s, respectively (chamber pressure less than 5×10^{-7} mTorr). After the deposition, we lift-off the metal mask using heated Remover PG at 80 °C. Thereafter, we spin coat the double layer photoresist (MIR-701 and LOR-10A) with the mask to pattern the graphene into rectangular patches, expose at 63 mJ/cm^2 using 365 nm light, and develop using AZ-300MIF (45–60 s).

After the dry etching, the hardened fluorinated single layer photoresist cannot be removed completely without the use of 400 T, which is an aggressive tetramethylammonium hydroxide based chemical that delaminates graphene even when covered with a 30 nm Ti layer. Therefore, instead of using a single layer of photoresist, which is common in dry etching procedures, we decided to use a double layer photoresist,³¹ which is easily removed by Remover PG. After the development of the graphene patch mask, we use dry etching with SF_6/Ar (20/5 sccm) plasma (75 W, 10 mTorr) for 7 min. In Fig. 2 (step 6), we show that the photoresist covers only the graphene patches, since the Cr/Au layer is not etched by the plasma, hence acting as a self-aligned hard mask. In addition, the DC-bias of the dry etching procedure was optimized to minimize the resputtering of the gold, while retaining an acceptable etching rate. After the dry etching is completed, we clean the remaining photoresist using a fast (less than a minute) O_2 plasma dry-etch and heated Remover PG at 80 °C. Finally, we remove the Ti sacrificial layer by submerging the wafers in a 1:36 HF:DI water solution for 2 min. In Fig. 3, we depict a representative Raman spectrum of the monolayer graphene pieces on the final devices, establishing the fabrication process. The G and the 2D peaks before and after the full fabrication process are similar in height and position, indicating no significant changes in doping, while there is no D peak, indicating that the graphene remains intact and free of defects.³²

We transfer the graphene at the beginning of the process, to increase the overlapping metal-graphene area achieving good ohmic contact and providing mechanical rigidity by

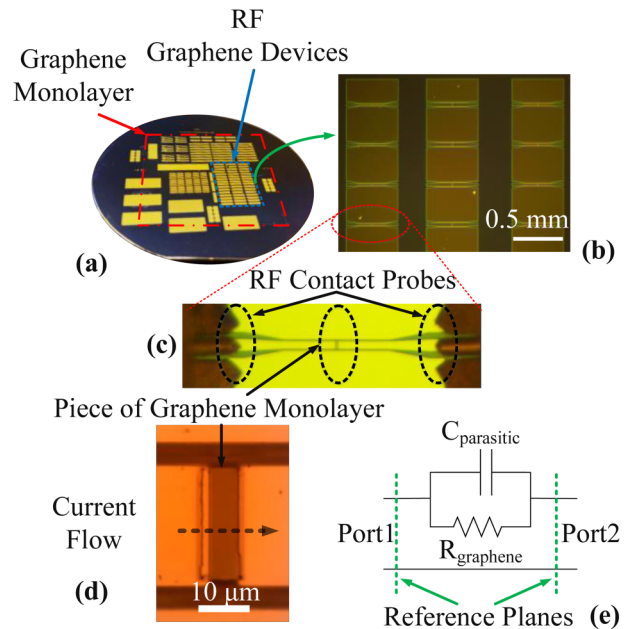


FIG. 4. (a) Photograph of the fabricated on-wafer RF devices. (b) An optical microscope image of the wafer depicting an array of the developed graphene-based devices. (c) An optical microscope image of a single graphene device during the high-frequency RF-measurements. (d) An optical image of a single graphene patch with dimensions $5 \times 20 \mu\text{m}^2$ (four squares for the current flow). (e) The equivalent R-C model of the graphene devices.

robustly anchoring the graphene on the substrate. The final wafer is shown in Fig. 4(a), where the total graphene dimensions are $2 \times 2 \text{ cm}^2$ and the wafer has more than 280 graphene RF devices. Also in Figs. 4(b)–4(d), we depict a fabricated on-wafer CPW transmission line that has a small piece of monolayer graphene ($5 \times 20 \mu\text{m}^2$) intersecting the center conductor. These devices are used to characterize the graphene properties (namely, the sheet resistance as a function of frequency) in the 220–330 GHz band and provide an estimate of the yield of the proposed fabrication process.

To demonstrate the severity of graphene delamination during the standard no-Ti nanofabrication process, in Fig. 5(a) we depict the resulting wafer where the lift-off solution (Remover PG) clearly delaminates the graphene monolayer [Fig. 5(c)], leading to a nearly 0% yield.

III. HIGH-FREQUENCY GRAPHENE MEASUREMENTS

To validate the outcome of our procedure, we carry out on-wafer, in-plane measurements of the graphene sheet resistance at the 220–330 GHz band for the first time. The acquired data are compared with related works that either measure the graphene characteristics in lower frequencies using in-plane topologies (transmission lines) or characterize the out-of-plane properties using quasi-optical setups.^{7–10} However, none of the aforementioned studies presents the graphene sheet resistance (or conductance) over a wide frequency range as in our present work. Specifically, the previously published measurement results are obtained over wide frequency ranges, but the reported data refer to either single frequency responses or averaged values (over frequency). These comparisons are summarized in Table I.

To characterize the in-plane graphene sheet resistance, we devised the topology shown in Figs. 4(c) and 4(d), consisting of a CPW line with a piece of monolayer graphene, embedded as the device-under-test.

The measurements were carried out using a Rohde & Schwarz network analyzer that probed two Virginia Diodes

TABLE I. Reported graphene sheet resistances.

Sheet resistance (Ω/\square)	Frequency range (GHz)	Measurement configuration	Reference
1100	1–20	In-plane	8
1260	DC–110	In-plane	7
1307	220–330	In-plane	This work
1600	200–1000	Out-of-plane	9
1490	250–2000	Out-of-plane	10

Inc. frequency extenders covering the 220–330 GHz band. The RF signal was then coupled on the CPW line using GGB contact probes [Fig. 4(c)]. To accurately extract the graphene sheet resistance without including the errors from the contact probes, mismatches, etc., we performed a

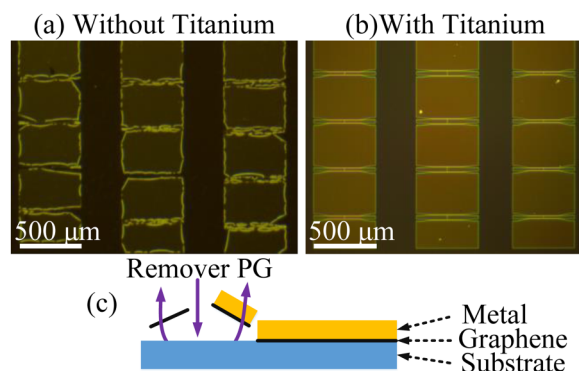


FIG. 5. (a) Optical microscope images of an array of graphene devices for the standard no-Ti wafer after the lift-off procedure and (b) the final wafer with the use of Ti sacrificial layer. (c) Graphene delamination during lift-off in Remover PG solution (metal patterning), leading to excessive deformation of the metal layer.

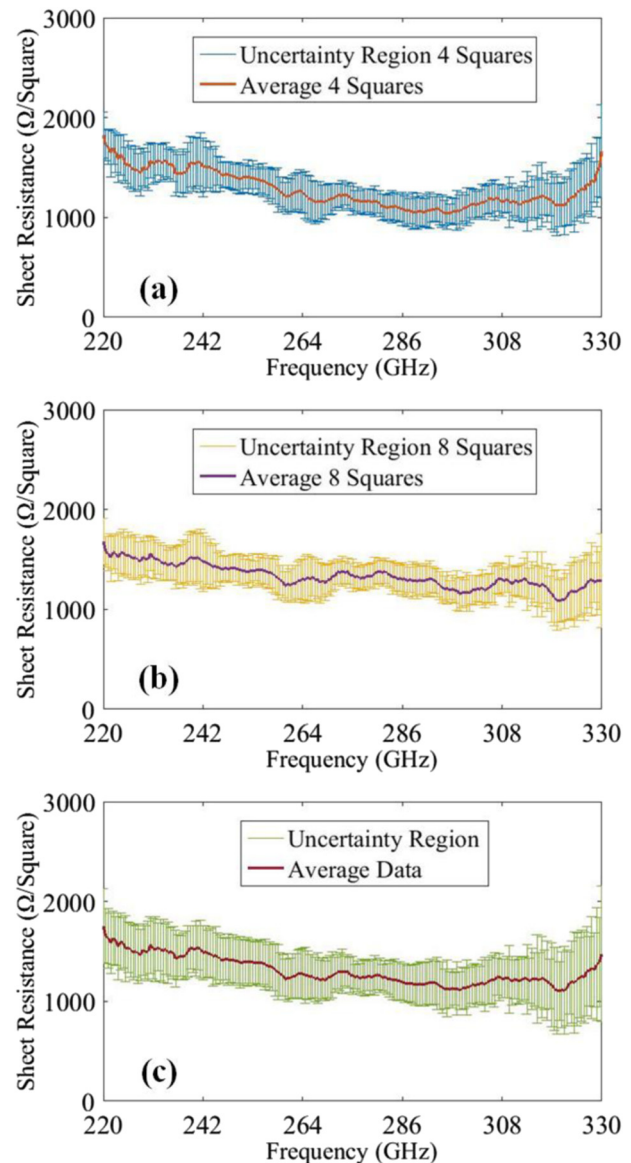


FIG. 6. Acquired sheet resistance of graphene in the 220–330 GHz range: (a) four squares, (b) eight squares, and (c) averaged data. The uncertainty region in all figures includes both the measurement error and the device variability.

wideband thru-reflect-line calibration across the 220–330 GHz region.³³ In addition, we measured the device without including the graphene to extract the parasitic capacitance [Fig. 4(e)]. Namely, we model the device as a parallel circuit consisting of a resistance that represents the monolayer graphene sheet and a capacitor that accounts for the high capacitive coupling [Fig. 4(e)]. Two different sets of devices were developed with four ($5 \times 20 \mu\text{m}^2$) and eight ($3 \times 24 \mu\text{m}^2$ and $5 \times 40 \mu\text{m}^2$) parallel squares for the current flow. Using different configurations of graphene dimensions, we are able to extract the graphene sheet resistances for different capacitance values, thus establishing our measurement process. Specifically, the total resistance for the three different groups of devices differs, since the capacitance depends on the CPW discontinuity's dimensions. However, the monolayer graphene's sheet resistance should be identical regardless of the capacitance.

The calculated graphene sheet resistances for both the four and eight square devices are given in Fig. 6. The graphene sheet resistance is almost uniform across the entire bandwidth. In Table I, the average measured sheet resistance value is presented along with those found in the literature, validating our high-yield fabrication and measurements procedure. To the best of our knowledge, previous works that have measured the graphene characteristics using in-plane propagation devices (i.e., transmission lines, etc.) are limited to lower frequencies and do not apply proper calibration (only numerical de-embedding) and/or use graphene multilayers.^{6,7} On our prototype wafer, we measured 39 functional devices out of 42 in total, leading to a 92% yield. Even though we fabricated more than 280 devices, extensive measuring using RF contact probes leads to their degradation, so we decided to measure only 42 devices.

IV. SUMMARY AND CONCLUSIONS

Concluding, we presented a high-yield fabrication procedure for the development of on-wafer mmW/THz graphene devices. Using the proposed procedure, we achieved 92% fabrication yield enabling the implementation of large-format, multiwavelength reconfigurable graphene devices, including metasurfaces and phased arrays. To achieve high functional device yield, we covered the graphene monolayer with a Ti sacrificial layer throughout the nanofabrication procedure preventing delamination. In addition, we characterized the in-plane graphene sheet resistance in the 220–330 GHz band for the first time. The measured data are in good agreement with the existing literature, verifying the robustness of the proposed fabrication method.

Future work includes optimization of the fabrication steps to acquire even higher yields. Specifically, we aim to optimize the lift-off process that is a long and aggressive procedure with the use of a heated chemical (PG Remover), hence minimizing graphene delamination even further. Alternatively, we can change the thickness of the protective Ti sacrificial layer to provide further protection during the lift-off process. A limiting aspect of this work is metal

degradation at the landing pads due to the contact force applied by the RF probes and the poor metal to graphene adhesion. Namely, after a few landings (4–5) the metal completely delaminates, preventing any further access to the RF graphene devices. In future revisions of the process, the metal contact degradation can be mitigated by adding another fabrication step that cleans the landing areas from graphene using dry etching, thus providing rigid metal to substrate adhesion. Finally, although this work has focused on high resistivity silicon substrates, the method can be extended to wafers that are coated with thin insulating layers (e.g., aluminum oxide and silicon nitride).

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