Toward Large-Scale Dynamically Reconfigurable Apertures Using Graphene

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***Abstract*—We present a novel fabrication technique for large-scale, on-wafer graphene devices. With the proposed technique, large-area graphene apertures can be fabricated, enabling the proliferation of graphene-based reconfigurable devices, including metasurfaces. Such topologies require large-area high yield fabrication processes. To avoid graphene delamination during the chemical processes of the fabrication, we use a titanium sacrificial layer to protect the graphene monolayer. To evaluate the fabrication method, we present broadband in-plane graphene measurements in the 220-330 GHz band for the first time and compare the measured resistance sheet with previous works.**

Keywords*—*Graphene, reconfigurable, apertures, measurements

I. INTRODUCTION

Graphene has attracted huge interest in the electromagnetics community due to its tunable nature, that enables the development of low-profile, dynamically reconfigurable devices, including large-aperture metasurfaces [1]-[6]. Such topologies can be exploited for high-spatial-resolution imaging and communication applications. Their key advantage compared to the other topologies (e.g. phased arrays) is the absence of complex/lossy and bulky feeding networks. As such, reconfigurable graphene-metasurfaces exploit integrated graphene modules to manipulate the aperture radiation characteristics. Specifically, using electrodes (or other biasing schemes including ion-gel), an external bias is applied that shifts the graphene Fermi level, thus tuning the graphene sheet impedance. This tunability is exploited to control the effective electromagnetic properties (e.g. surface impedance) of the metasurface's unit cells (Fig. 1), hence, dynamically reconfigure the aperture currents, forming various radiation patterns. For example, generating orthogonal radiation patterns we can implement real-time, lensless imaging systems [4].

Most of the studies concerning such topologies are limited to theoretical modeling since fabrication poses several engineering challenges. Namely, large-scale graphene fabrication has been a roadblock toward developing devices form DC to high-frequency applications [7]. Specifically, the delicate nature of graphene prohibits the use of multiple chemicals that are commonly used in high-yield/large-scale fabrication procedures [7]. Therefore, to device dynamically reconfigurable graphene metasurfaces in the sub-millimeter wave (sub-mmW) region, we developed a high-yield nanofabrication process that protects the delicate graphene from the chemically aggressive processes. In addition, alternative technologies including CMOS/SiGe that can be exploited to achieve reconfigurability through transistors, lead to complex designs that significantly increase the cost of these large-aperture topologies. Hence, the proposed fabrication method constitutes a cost-effective/robust solution for the development of large-scale graphene-based metasurfaces.

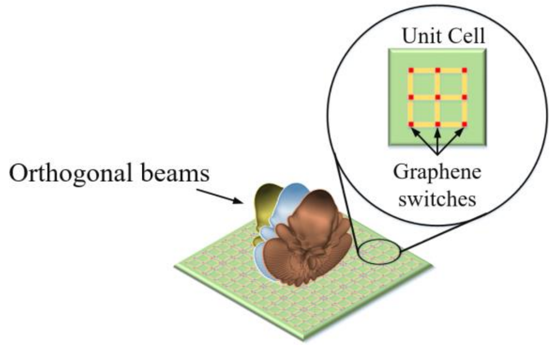

Fig. 1 A dynamically reconfigurable graphene metasurface {Inset: the unit cell consisting of graphene switches (red) and metallic patches (orange)}.

II. LARGE AREA GRAPHENE FABRICATION PROCESS

The nanofabrication method is presented in Fig. 2. In this process, we use a 30 nm titanium (Ti) sacrificial layer that protects graphene throughout etching, development, and lift-off. These steps are the most aggressive due to the use of strong chemicals and are responsible for graphene delamination from the carrier substrate.

Initially, to devise the graphene devices, we transfer a 2 cm× 2 cm graphene monolayer on a high-resistivity silicon substrate (>10,000 Ω·cm) using a wet process. Then, we deposit a thin (30 nm) Titanium layer to cover the graphene sheet. Afterward, we use photolithography, development, sputtering, and lift-off, to pattern the metal topology of our devices. After the metal layer is formed, we use photolithography and dry etching to pattern the graphene devices. Finally, we clean the remaining Ti using a strong solution of hydrofluoric acid (HF).

After the nanofabrication is completed, we deposit the ion-gel gating material on top of the graphene devices. Instead of the common back gating structures with doped semiconductors (e.g. doped silicon), ion-gel is used since it is transparent in the

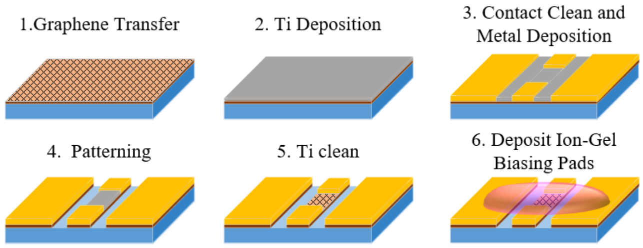

Fig. 2 The proposed nanofabrication procedure used to develop large-area graphene devices: 1. Transfer graphene on the high-resistivity Si substrate, 2. Deposit a 30 nm Ti sacrificial layer using electron-beam evaporation, 3. Form the metal layer of gold/chrome using photolithography, electron-beam evaporation, and lift-off (before the metal deposition we clean the Ti from the open areas to ensure good metal-graphene contact) 4. Pattern graphene devices using dry etching, 5. Clean the Ti sacrificial layer using wet chemistry, 6. Deposit ion-gel on top of the devices for biasing.

sub-mmW region [5], and works as an encapsulating layer that protects the graphene from atmospheric exposure.

The final device, shown in Fig. 2-6, is a coplanar waveguide (CPW) topology with a series graphene piece. We used the depicted design to test the graphene switching performance carrying out on-wafer measurements, as described in the following section. In our prototype, we developed over 280 graphene modules, covering a 2 cm×2 cm area, with more than 90% yield.

III. MEASUREMENT RESULTS

In this work, we are interested in extracting the graphene sheet impedance that can be exploited for the theoretical design and analysis of dynamically reconfigurable apertures. For that purpose, we carry out sub-mmW measurements in the 220-330 GHz band using a Rohde-Schwarz ZVA 24 Vector-Network-Analyzer (VNA) and two Virginia Diodes frequency extenders. Afterward, we use GGB contact probes to couple the RF signal on the CPW structure. Finally, we carry out on-wafer thru-reflect-line (TRL) calibration [8] to eliminate the systematic errors caused by the CPW losses, contact probe coupling, and the VNA. The calibrated measured S_{21} data are given in Fig.3. From the measured scattering parameters, we extract the graphene sheet impedance given in Table I and compare with previous works.

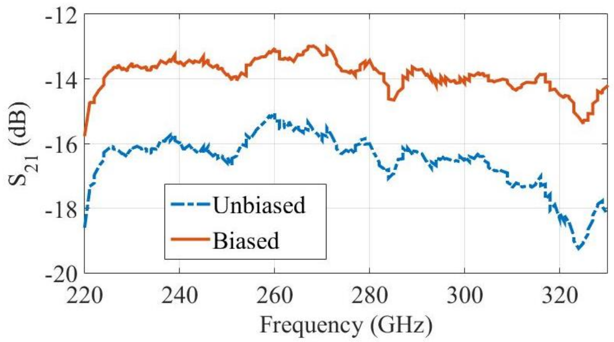

Fig. 3 The S_{21} parameter of the graphene device for the biased and unbiased case.

TABLE I
REPORTED GRAPHENE SHEET RESISTANCES

Unbiased Sheet Resistance (Ohm/□)	Frequency Range (GHz)	Maximum Achieved Ratio	Reference
1335	220-330	5	This Work
1600	200-1000	3.8	[5]
1490	250-2000	4	[6]

IV. CONCLUSIONS

In this work, we present a high-yield fabrication procedure for the development of dynamically reconfigurable graphene metasurfaces. Additionally, we extracted the graphene sheet impedance through on-wafer measurements. The fabrication process successfully protects the graphene from delamination, thus providing good RF performance. As such, graphene sheet impedance is measured at 1335 Ω/□ and the maximum achieved switching ratio is 5. Instead of using theoretical equations that provide inaccurate performance estimations, we will use the presented measurement results to design high-performance metasurfaces. In addition, by exploring the high-yield fabrication procedure (>90% yield), we enable the proliferation of such graphene topologies.

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