On-Wafer Graphene Devices for THz Applications Using a High-Yield Fabrication Process

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***Abstract*—We characterize a novel fabrication procedure for the implementation of large arrays of subwavelength graphene devices. With the proposed process, we can now integrate graphene layers on large substrate areas (> 4 cm^2) and implement thousands of devices with high-yield (> 90 %). Examples of such systems include broadband THz phased arrays and metasurfaces that can be used in THz imaging and sensing. Current nano-fabrication processes hinder the proliferation of large arrays due to the fragile nature of graphene. Conversely, we use titanium sacrificial layers to protect the delicate graphene throughout the fabrication process. Thus, we minimize graphene delamination and enable multiple devices on large-area substrates with high-yield. In addition, we present a series of on-wafer measurement results in the 220-330 GHz band, verifying the robustness of our fabrication process.**

***Index Terms*— Graphene, on-wafer, fabrication, characterization, terahertz**

I. Introduction

A significant research effort has been devoted in dynamically reconfigurable millimeter-wave/Terahertz (mmW/THz) devices (30 GHz-1 THz) that has led to the development of various novel configurations both for imaging and communication applications [1]-[13]. At these frequencies, reconfigurability has been achieved using tunable capacitors [1], diodes [2], and tunable materials [3][4], (e.g. indium tin oxide). Nevertheless, in the past years, several research efforts have focused on switches and other devices that exploit the tunable electromagnetic properties (e.g. conductivity) of 2D materials such as graphene [5]. Graphene exhibits tunable sheet resistance that is regulated with the use of external biasing mechanisms, such as field-effect-transistors [5]. In addition, graphene typically exhibits tunability in ultra-wide bandwidths that makes it attractive for broadband applications [5]-[9].

Nonetheless, most of the works concerning the development and fabrication of large-scale RF graphene devices are either limited to low-frequencies (< 110 GHz) [5]-[7] or used for THz out-of-plane propagation applications [8][9]. In-plane graphene characterization has been carried out for either for dual layered graphene [5] or graphene flakes [6] that are insufficient to extract the monolayer properties. Moreover, a DC-110 GHz in-plane graphene monolayer characterization was carried out using on-wafer devices in [7]; however, this study uses numerical calibration to de-embed the transmission line leading to high-frequency inaccuracies. On the other hand, out-of-plane spectroscopy has been deployed for the characterization of graphene sheet resistance in the 0.2-2 THz range. Even though spectroscopy is a well-established technique, the resonance effects caused by the substrate, limit the ability to measure graphene sheet resistance accurately in a broad spectrum [8][9].

Furthermore, due to difficulties encountered during fabrication procedures, mmW/THz graphene devices are predominantly studied using theoretical models and full-wave simulations [10]-[13]. Typically, graphene devices are fabricated using well-established photolithography techniques, however, the yield is low (< 70 %); since wet exfoliation is common due to poor adhesion between common substrates and graphene [14]. This effect deteriorates in the case of low-loss on-wafer RF devices that demand thick metal layers. For example, at 300 GHz the skin depth of gold (Au) is 140 nm, hence the Au thickness for a 300 GHz transmission line should be at least 280 nm to avoid excess ohmic losses. However, developing thick metal layers (>0.2 μm) with integrated graphene patches is non-trivial, due to the compatibility of graphene with the chemicals used during the fabrication steps. In more detail, to fabricate thick metal layers it is preferable to use double layer lift-off photoresists to achieve fine resolution with higher yield and easier processes [15]; though, the chemicals used during this process dramatically increase graphene exfoliation.

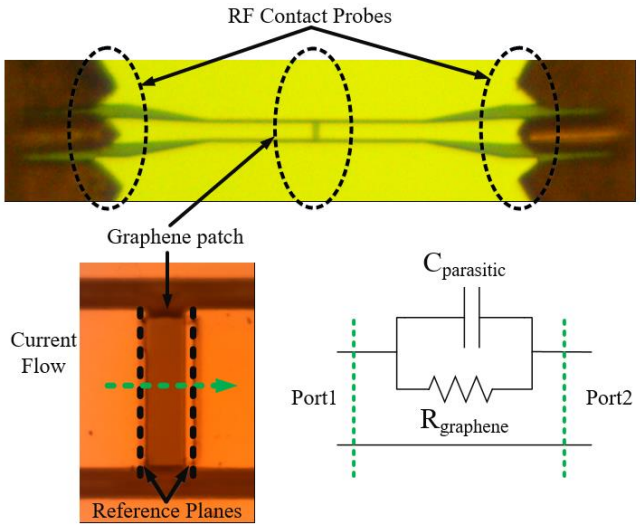

Fig.1 The fabricated CPW lines with the embedded graphene patches and the equivalent circuit model. Graphene patch length is 5 μm and the width is 20 μm (4 parallel squares for the current flow). CPW width is 20 μm and the gap is 4 μm, resulting in 36 Ω characteristic impedance. The landing pads of the contact probes are 50 Ω.

In this work, we present a high-yield nano-fabrication process that enables the development of large-scale mmW/THz graphene devices using Titanium (Ti) sacrificial layers to prevent graphene exfoliation. Furthermore, to validate the outcome of our procedure we carry out on-wafer, in-plane measurements of the graphene sheet impedance in the 220-330 GHz band for the first time. In this manner, we characterize monolayer graphene properties in sub-mmW frequencies, enabling the development of multiple novel reconfigurable devices, including phase shifters and metasurfaces. The measured data are compared with related previous works that either measure the graphene characteristics using in-plane devices (e.g. transmission lines) in lower-frequencies (below 100 GHz) or characterize the properties using out-of-plane quasi-optical setups [6]-[9].

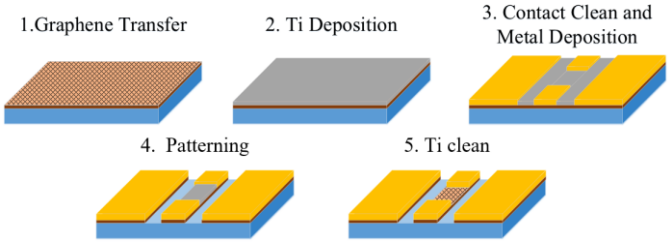

Fig.2 The proposed nano-fabrication procedure used to develop large-area graphene devices: 1. Transfer graphene on the high-resistivity Si substrate, 2. Deposit a 30 nm Ti sacrificial layer using electron-beam evaporation, 3. Form the metal layer of gold/chrome using photolithography, electron-beam evaporation, and lift-off (before the metal deposition we clean the Ti from the open areas to ensure good metal-graphene contact) 4. Pattern graphene devices using dry etching, 5. Clean the Ti sacrificial layer using wet chemistry.

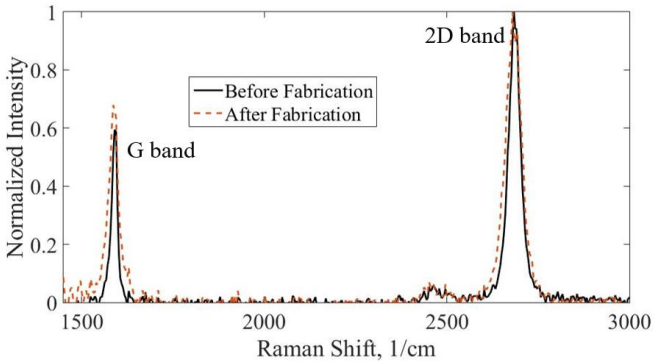

Fig.3 The Raman spectrum of the graphene monolayer acquired before and after the fabrication procedure (60 sec total integration time).

II. Fabrication Process Using Titanium Sacrificial Layers

In this work, we propose a high-yield nano-fabrication process that uses Titanium sacrificial layers to protect graphene throughout the steps and retrieve its intrinsic properties [16]. To enable accurate on-wafer THz characterization, we integrate graphene patches along the signal line of a coplanar-waveguide (CPW), as depicted in Fig.1. The CPW line is implemented with 50 Ω contact pads on both ends to facilitate contact with RF probes. Figure 2 details the fabrication process we follow to develop the graphene devices. Initially, we transfer a graphene monolayer on the high-resistivity (>10,000 Ohm·cm) silicon substrate using wet transfer [17]. The Raman spectrum of the graphene monolayer on high resistivity silicon is plotted in Fig. 3.

Graphene is transferred at the beginning of the process, to increase the overlapping metal-graphene area, achieving good ohmic contact and providing mechanical rigidity by anchoring the graphene on the substrate. In Fig. 1, we depict a fabricated on-wafer CPW transmission line that has a small graphene patch intersecting the center conductor. These devices are used to characterize the graphene properties (sheet resistance versus frequency) in the 220-330 GHz band and provide an estimate on the yield of the proposed fabrication process. In Fig. 3, we also present the acquired Raman spectrum of the graphene patches on the final devices. As clearly shown, the graphene monolayer remained intact throughout the fabrication procedure. In our prototype, 265 out of the 288 graphene devices were functional, resulting in a 92 % yield.

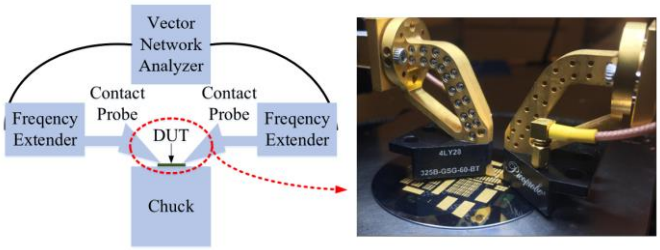

Fig.4 The setup used to carry out the on-wafer measurements in the 220-330 GHz band.

III. On-Wafer Characterization of Graphene Sheet Resistance

We conducted on-wafer measurements to characterize graphene's intrinsic properties in sub-THz for in-plane wave propagation. To the best of our knowledge, previous works that have measured the graphene sheet impedance using in-plane propagation devices (transmission lines etc.) are limited to lower frequencies and measure either graphene multilayers [5], have graphene flakes [6], or do not perform on-wafer calibration (numerical de-embedding form contact tip to device) [7].

Therefore, we implemented the topology shown in Fig. 1, consisting of a CPW line integrated with a graphene patch on high-resistivity silicon, embedded as the device-under-test (DUT). Initially, to measure the graphene properties we acquired the scattering parameters of the graphene patches, using the setup depicted in Fig. 4, in which we use a Rohde & Schwarz ZVA network vector analyzer, connected to Virginia Diode Inc. (VDI) WR-3.4 frequency multipliers that up-convert the microwave signal to the 220-330 GHz band. Then, we couple the RF-signal to the CPW lines using GGB contact probes (Fig. 1).

The accurate graphene sheet impedance characterization requires measurement of the parallel parasitic capacitance and a necessary on-wafer calibration that will provide intrinsic values of the devices. As such, we carried out a two-tier calibration to eliminate the errors associated with the waveguide mismatches, contact probe landing, substrate losses etc. Specifically, we first calibrate the waveguide ports of the extenders using a waveguide-based Short-Open-Load-Thru (SOLT) calibration [18]. The acquired S_{21} raw-data from a graphene device and a device without the presence of the graphene (open) are given in Fig. 5. Then, we perform an on-wafer Thru-Reflect-Line (TRL) calibration [19], shifting the reference plane on the graphene DUT (Fig.1). The calibrated S_{21} data are also given in Fig. 5. In addition, in Fig. 5 we depict the theoretical S_{21} calculated for the CPW open discontinuity, calculated using full-wave simulations. Afterward, we use the calibrated scattering parameters to calculate the device ABCD parameters [20]; hence, the total series device impedance is

$$Z_{total} = B \qquad (1)$$

where B is the parameter of the ABCD matrix. However, this impedance incorporates both the parasitic capacitance and graphene resistance (Fig. 1). Therefore, graphene sheet resistance is obtained from

$$Z_{graphene} = \frac{Z_{capacitance} Z_{total}}{Z_{capacitance} - Z_{total}} \times N \qquad (2)$$

where N is the number of parallel graphene squares the current flows through the patch ($N=4$ for the case of Fig. 1). To characterize graphene sheet resistance accurately we devise several DUTs with various N values. Specifically, we used two sets of devices with $N=4$ and $N=8$, with respective dimensions of 5×20 μm and 5×40 μm. The averaged extracted sheet resistances are given in Fig. 6. In addition, in Table 1, we present the average value of our graphene impedances along with other studies that use lower-frequency in-plane characterization, or out-of-plane characterization using quasi-optical setups. Our measured data are in good agreement with the literature, validating the reliability of our fabrication process and the expected broadband characteristics of graphene in the mmW/THz range. Moreover, even though the tabulated literature measurements are obtained over broadband frequency ranges, the reported sheet resistance values in these publications correspond to either single frequency points or averaged values.

IV. Discussion

We present a novel high-yield fabrication procedure for the development of large-scale arrays of tunable graphene-based devices, whose development is currently hindered by the limitations of existing nano-fabrication processes. For example, using this process we can develop large-scale/low-profile multiple-input-multiple-output (MIMO) printed antenna arrays, with embedded graphene switches to carry out simultaneous transmission exploiting orthogonal codes. Therefore, we can achieve fast image acquisition and low noise compared to existing systems that use sequential scanning to acquire the data, leading to real-time mmW/THz imaging configurations for automotive and security applications. In another application example, the proposed process can be exploited to develop, large-area dynamically reconfigurable metasurfaces that can be used either for imaging or communication purposes [10].

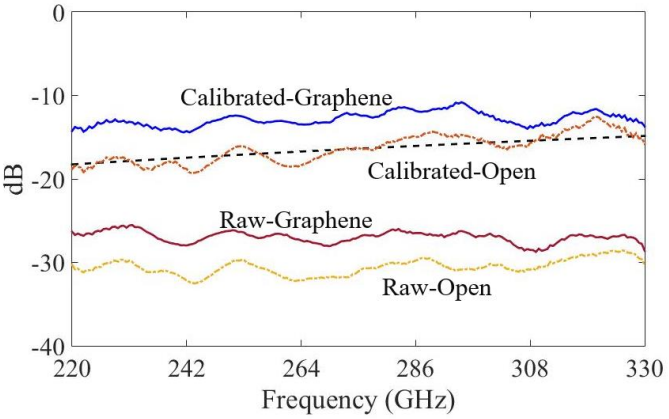

Fig.5 The raw and calibrated $|S_{21}|$ of the devices with and without graphene. As expected graphene increases the amount of the signal coupled to the second port. In addition, the black dotted line represents the theoretical $|S_{21}|$ value expected for the CPW open discontinuity (4 squares).

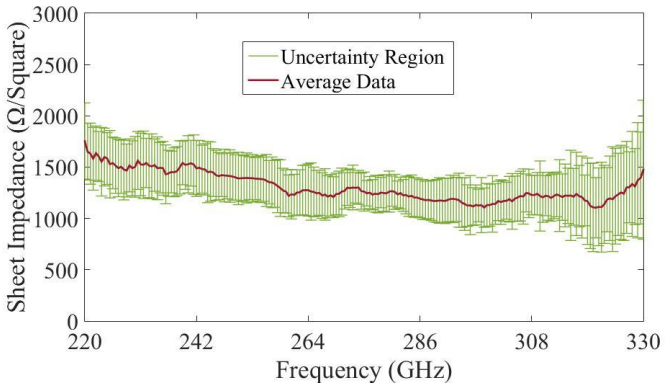

Fig.6 The measured graphene sheet resistance in the 220-330 GHz band. The uncertainty region includes both measurement errors and device variability.

Table 1. Reported Graphene Sheet Resistances

Sheet Resistance (Ohm/□)	Frequency Range (GHz)	Measurement Configuration	Reference
1100	1-20	In-plane	[6]
1250	DC-110	In-plane	[7]
1335	220-330	In-plane	This Work
1600	200-1000	Out-of-plane	[8]
1490	250-2000	Out-of-plane	[9]

V. Conclusions

In this work, we presented a high-yield fabrication procedure for the development of on-wafer mmW/THz graphene devices. Using the proposed procedure, we achieved more than 90 % fabrication yield enabling the design and fabrication of novel large-area graphene devices like metasurfaces and phased arrays. To achieve high-yield, we cover the graphene monolayer with a Ti sacrificial layer throughout the nano-fabrication procedure preventing chemical delamination. In addition, we carried out characterization of the in-plane graphene sheet resistance in the 220-330 GHz band for the first time, using a state-of-the-art setup. The measured data are in good agreement with the existing literature verifying the robustness of the fabrication and measurement procedures. As part of the future work, we plan to deposit ion-gel on top of the graphene patches and measure their switching performance. Exploiting the external biasing scheme, we will be able to reduce the graphene sheet impedance, hence create on-wafer integrated switches. In addition, to further decrease the graphene sheet impedance, multilayer graphene structures could be developed.

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