Smart Self-driving Multi-level Gate Driver for Fast Switching and Crosstalk Suppression of SiC MOSFETs

Chunhui Liu, Zhengda Zhang, Yifu Liu, Yunpeng Si, Qin Lei

School of Electrical, Computer and Energy Engineering

Arizona State University

Tempe, USA

Email: cliu212@asu.edu

Tel.: 623-213-0920

***Abstract*- Wide band gap devices, like silicon-carbide and gallium-nitride, have high switching speed potential. However, the actual speed in practical application is limited by the circuit parasitic components and the interaction between high-side switch and low-side switch in a phase-leg configuration, known as crosstalk effect. This paper proposes an isolated voltage source gate driver with crosstalk suppression capability to take full advantage of the inherent high switching speed ability of Silicon-carbide device. By applying variable gate voltage through the auxiliary circuit, the crosstalk problem can be mitigated. Using the original gate-source voltage as auxiliary circuit driving signal, the gate driver dose not introduce any extra control signals, which avoids the additional signal/power isolations and makes the auxiliary circuit very convenient to be implemented on the existing commercial gate driver. The auxiliary circuit makes the gate voltage rise from 0V other than -5V when the switch turns on, leading to faster switching speed and lower switching loss compared with traditional gate driver. LTSPICE simulation and double pulse test experiment results based**

on 1.2kV/60A Silicon-carbide MOSFET are conducted to evaluate the crosstalk suppression capability of proposed gate driver.

Keywords: **SiC MOSFET, Crosstalk suppression, Smart Gate Driver, self-driving**

I. INTRODUCTION

Now the Silicon Carbide device is expected to replace the Si device due to its high switching speed capability, allowing the shorter deadtime in a phase-leg and higher switching frequency. These benefits of SiC lead to higher power density and efficiency of power electronics converter. [1~6] However, in practical application, the SiC MOSFET switching speed is limited and usually much lower than the expected potential speed, especially in phase-leg configuration.

The biggest problem is the parasitic inductance in both gate loop and main power loop, which may introduce significant oscillation in device drain-source voltage (Vds) and gate-source voltage (Vgs), and thus limit the switching speed. Besides, the equivalent coupling capacitor (gate-drain capacitor, Cgd, miller capacitor) between power loop and gate loop will induce current to the gate during the Vds dv/dt happens. This current charges the Cgs while dv/dt is positive, which is at the device turn-off transient, and discharges the Cgs while dv/dt is negative, which is at the device turn-on transient. If the positive dv/dt happens during or after the gate source voltage falling edge, the additional miller charging may delay the turn-off, or mis-trigger the device after it is turned off, which can lead to the phase leg shoot-through fault. If the negative dv/dt happens before the gate source voltage rising edge, the additional miller discharging will introduce a negative overshooting on the negative gate voltage, which may over-voltage breakdown the gate of the device[1]. These problems are so-called crosstalk effect [3-4]. The mis-trigger problem is severe in hard-switching case and the negative overshooting problem is severe in soft-switching case. To avoid miller effect caused failure, the device switching speed needs to be forced lower [1-4], thus the fast switching characteristics of the SiC MOSFET is not fully utilized and the device efficiency will hit a certain boundary.

Previous work has been reported to deal with the crosstalk problems in two aspects[2~6]: power loop and gate driver loop. In terms of the power loop, many papers make improvements on enhancing dv/dt immunity of isolation, minimizing common source inductance or linearizing the Vds dv/dt. In terms of the gate loop, the basic idea is to modify the gate voltage during the dv/dt transient to avoid negative overvoltage breakdown or mis-triggering.

During the turn-off transient of positive Vds dv/dt, if the Vgs jumps to the threshold voltage, usually a relatively low voltage for the SiC MOSFET[4], the switch will mis-turn on. This issue can be overcome by lowering the off-state gate voltage to a safer negative level (e.g. -5V), to make Vgs harder to reach the threshold voltage. However, the thing followed is the higher risk of negative gate voltage breakdown before the turn-on transient, since the starting point of the negative overshooting is already a negative voltage. To address this problem, the state-of-the-art work proposed the methods of clamping the gate voltage to 0V or less negative level, e.g. -2V, by adopting different circuit topologies. In the intelligent gate driver proposed in [3], the gate driver circuit can be actively controlled to generate multi-level Vgs to mitigate the issue, with additional two transistors and two diodes. However, the auxiliary switches themselves introduce additional control signals and gate driving circuit. Thus, except for the isolation barrier required between the power switch side and controller side, the auxiliary switch also needs its own driving signals and galvanic isolations, which adds large number of auxiliary components and makes the circuit relatively complex. Moreover, these additional isolation barriers introduce additional common mode conduction path for the leakage current caused by the high dv/dt of the device, which will distort the control signal of the other channel at the controller side and may cause severe EMI issue (e.g. mis-trigger)[7]. Another drawback of this method is the high Rdson caused by the low on-stage gate voltage. In this paper, a smart self-driving multi-level gate driver (SMGD) for SiC MOSFETs, with mis-triggering and negative overvoltage suppression function, is proposed. Using original Vgs with simple RC delay as control signal of the auxiliary circuit, the proposed SMGD has these advantages over the other crosstalk suppression techniques: 1. No additional control

signals; 2. No additional dc/dc power supply and signal isolation stages for the auxiliary switch; 3. Easy to be implemented on the commercial gate driver IC. This paper analyzes the switching transient typical waveforms of a phase leg configuration and explain the root cause of crosstalk effect in section II. Then, in section III and IV, the operation principle of the proposed SMGD and its design guideline are discussed in detail. In section V, SMGD additional driving loss is evaluated and its impact on switching loss is also analyzed. Finally, a SMGD based on the commercial gate driver ADuM4135 is developed, the SPICE simulation and double pulse test results are discussed in section VI and section VII, respectively.

II. SWITCHING TRANSIENT ANALYSIS IN A PHASE-LEG AND CROSSTALK SUPPRESSION METHOD

A. Root cause of crosstalk

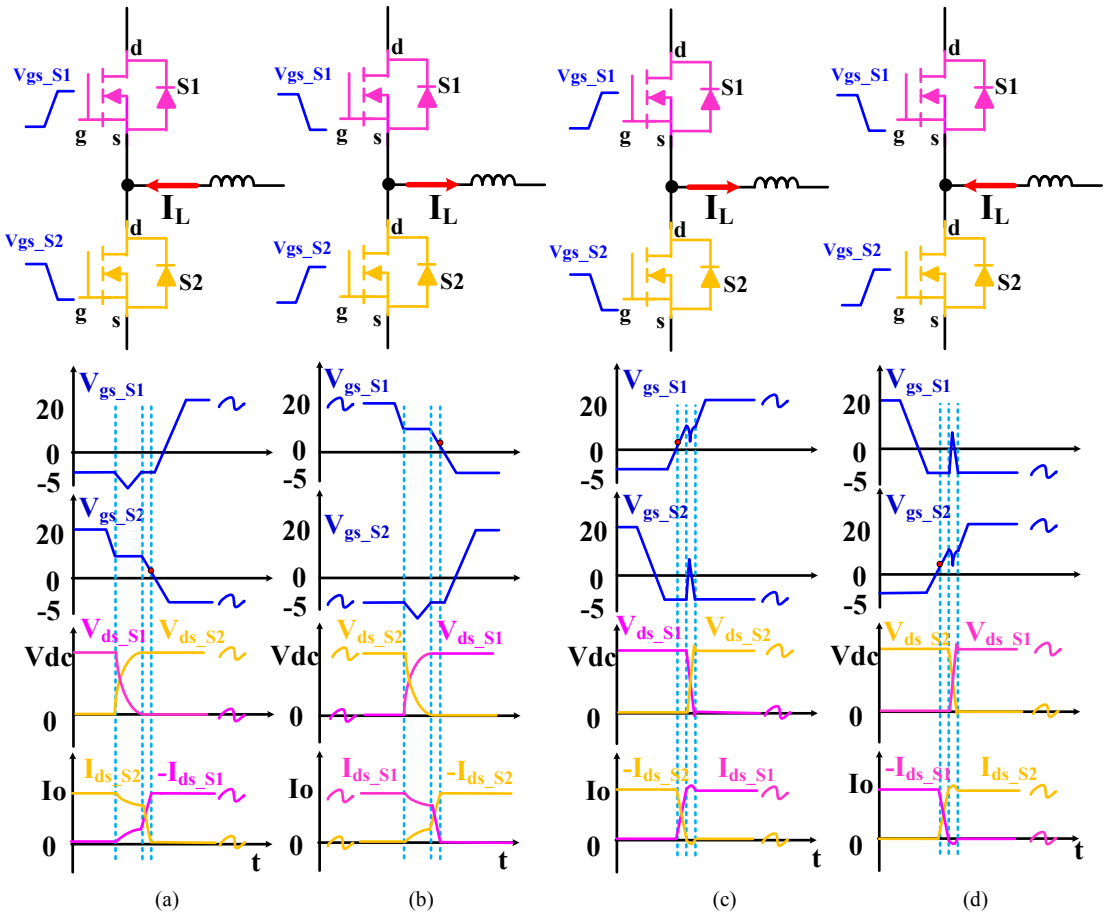


Figure 1 Vgs, Vds and Ids waveforms when (a) (b) the load current helps to charge the Cds of turn-off device and discharge the Cds of the complimentary device in the deatime (ZVS soft-switching); (c)(d) the load current does not help building up the device Vds voltage in deadtime (hard switching).

The crosstalk happens at the device Vds dv/dt transient and causes the distortion on the device Vgs. The Vds dv/dt can generate current flow (miller current) between MOSFET drain and gate through the gate-power loop coupling capacitor Cgd. At turn-off, the miller current caused by the positive dv/dt tries to charge the Cgs; at turn-on, the miller current cause by the negative dv/dt tries to discharge the Cgs. Look at one on/off transient of a phase leg. If the load current helps to charge the Cds of the turn-off device and discharge the complimentary device during deadtime, the Vds dv/dt of both devices will start at the turn-off signal falling edge and will complete during deadtime, This dv/dt caused miller current elevates the Vgs of the turn-off device and causes the turn-off miller plateau. Meanwhile, it pulls down the Vgs of the complimentary switch when this switch

Vgs is still at the off-state negative level to possibly overvoltage breakdown the device. This is typically the resonant ZVS switching case, as shown in Figure 1 (a)(b). In contrast, if the load current direction is opposite to the current direction of building up device Vds, a much larger Vds dv/dt is forced to happen during the turn-on signal rising edge in the deadtime zone, which elevates the Vgs of the off device at a large amplitude to possibly mis-trigger the device, and pulls down the Vgs of the complimentary device during its rising-up to delay the turn-on process (turn-on miller plateau). This case is shown in Figure 1 (c)(d), which are the turn-on and turn-off typical waveforms of hard-switching. For the SPWM and double pulse test, the waveforms of a phase-leg can be (a)(d) or (b)(c) depending the load current direction.

B. Proposed suppression method for the crosstalk effect

Figure 2 proposed gate voltage waveform for cross talk suppression

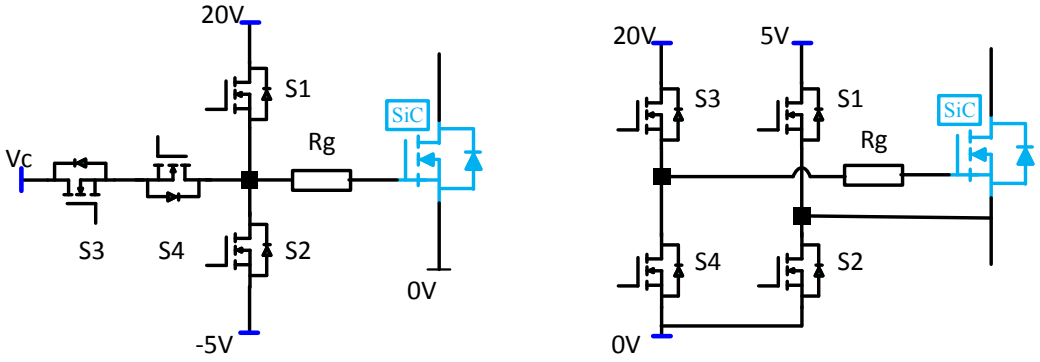
To mitigate the risk of gate mis-triggering caused by Vds positive dv/dt, one effective method is to bring the off-state gate voltage to a more negative level. However, this will take the Vgs negative overshoot to a more negative level thus exposes the gate to higher risk of negative over-voltage breakdown.

Many gate driver companies and papers [2][8][15][16]suggest using clamping strategies: 1. Zener diode directly clamps Vgs between +20V and -5V; 2. two Schottky diodes connecting the MOSFET gate to power supply voltage +20V/-5V directly to limit the Vgs in the range of -5V~20V. Because the dynamic response of Schottky diode is faster than that of Zener diode, the Schottky diode clamping is more effective than Zener diode clamping, but still, the Schottky diode clamping performance is limited by its dynamic response and diode current rating[2][8]. Moreover, the

parasitics on the Schottky diode clamping path will affect the clamping result. As a result, usually the voltage overshooting can be alleviated to a certain extent by using Schottky diode clamping strategy, but it cannot guarantee the device is safe from overvoltage breakdown. Therefore, a more effective strategy is to keep the gate voltage at an adequate negative level when the gate positive spike (possibly mis-trigger) happens and pull up the gate voltage to a less negative level before the gate negative overshooting event. This requires a multi-level gate voltage at off state. The proposed gate driver circuit achieves this goal with minimum number of auxiliary devices and a very simple passive circuit. As shown in Figure 2, the proposed crosstalk suppression method (red dotted line) brings up the gate voltage to 0V and clamp it at 0V after the mis-triggering period (T2~T3) and before the turn-on signal comes (T4), makes negative overshooting ride on 0V level (T3~T4) and the risk of negative breakdown is significantly mitigated.

III. Operation Principle of SMGD

The commonly used voltage source gate driving circuit for SiC MOSFET consists of three components (no bootstrap type): one isolated gate driver IC for signal amplification and signal isolation, one isolated DC/DC power converter for supplying gate driving power and on/off gate resistors to limit the maximum gate driving current and adjust the switching speed.



(a) T-type gate driver (b) H-bridge gate driver

Figure 3 State of the art three-level gate driver topologies

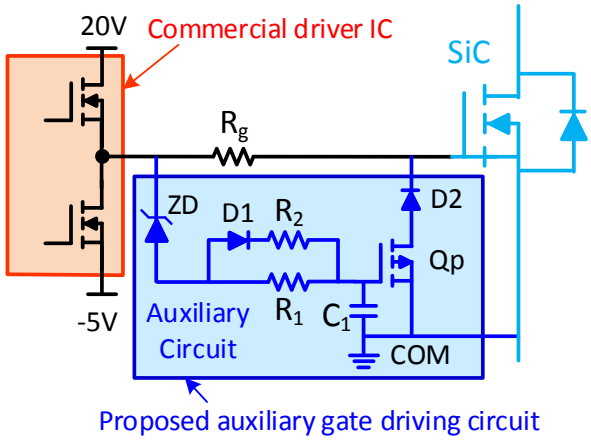


Figure 4 proposed three-level gate driver schematic for crosstalk suppression

To implement the three-level gate driver, one easy way is to use the three-level circuit topology, such as H-bridge and single-phase T-type, as shown in Figure 3, to connect three levels of power supply voltage to the gate. However, the devices themselves in these circuit need gate driver circuits. Moreover, all these gate driver circuits require three parts: isolated gate signal, isolated gate power supply and gate resistors. It not only adds many extra components to the circuit, but also introduces additional high voltage isolation barriers which can lead to complex common mode current path and distort the gate signal in an unpredictable way.

In order to overcome these drawbacks, the key is to utilize the existing gate signal and gate power supply to drive the auxiliary switch. The proposed gate driver is a highly cost-effective and compact self-driving three level gate driver, as shown in the blue part of Figure 4. To create a zero-level gate voltage during the off-state, an active switch Qp is used to connect the gate and source; whenever the zero voltage level is needed, it can be turned on to clamp the gate voltage to 0V. Originally it needs an additional gate driver circuit, but this can be avoided if the original gate driver output off-state voltage can be utilized to drive this switch. The gate driver IC output voltage at off-state cannot be directly used since the zero clamping does not happen at the same moment of the off signal, however, the off-state gate voltage can be delayed with a RC circuit to drive the active switch Qp as long as Qp is a P-channel MOSFET. The RC time constant can be designed to guarantee the Qp is triggered after the gate positive overshooting period. The operation of Qp is

supposed to be active only during the off-state, which cannot be simply achieved by this RC circuit. Whenever the Vgs is positive, Qp should be turned off, therefore, a series-connected diode is needed to block the positive gate voltage as well as the reverse conduction of the Qp body diode. Under this condition, in order to turn off the Qp, an adequate positive voltage should be applied on the gate of Qp. Since the gate of Qp is connected to the gate driver IC output, which at this moment outputs a positive high voltage (e.g. 20V , 18V etc.), a component is necessary on the Qp gate path to reduce this high voltage to a proper value to protect the Qp from gate overvoltage breakdown. Besides, this component should not affect the off-state negative gate voltage. A Zener diode is suitable to achieve this goal. Therefore, the complete auxiliary circuit is constructed, as shown in the dark blue block of Figure 4. The auxiliary circuit consists of two parts: the first part is the SiC MOSFET gate-source clamping circuit - the Schottky diode D2 and auxiliary switch Qp in series connection. The second part is the RC delay circuit connected to gate driver IC output port to generate the control signal for the auxiliary switch Qp. The labels' corresponding components are listed in Table I.

Table I components list for auxiliary circuit

Label	Component
ZD	18V Zener diode
D1, D2	Schottky diode
Qp	P-channel MOSFET
C1	Gate capacitor of Qp
R1,R2	Gate on/off resistor of Qp

The gate of the auxiliary switch Qp is connected to the output of traditional gate driver IC through RC circuit. When the turn-off signal comes, the gate driver negative output voltage (-5V) will charge the gate of SiC MOSFET through Rg and meanwhile the IC output voltage will charge the

auxiliary RC circuit to make the voltage across C1 reach the threshold voltage of Qp after a designed delay time. This delay makes the Qp turn on after the SiC MOSFET gate passes the positive overshooting period (T2~T3 in Figure 2). Once Qp turns on, the Qp and D2 provide the short circuit path between the SiC MOSFET gate and source. Therefore, the 0V gate voltage is achieved by D2-Qp clamping.

The operation procedure can be divided into four stages in Figure 5:

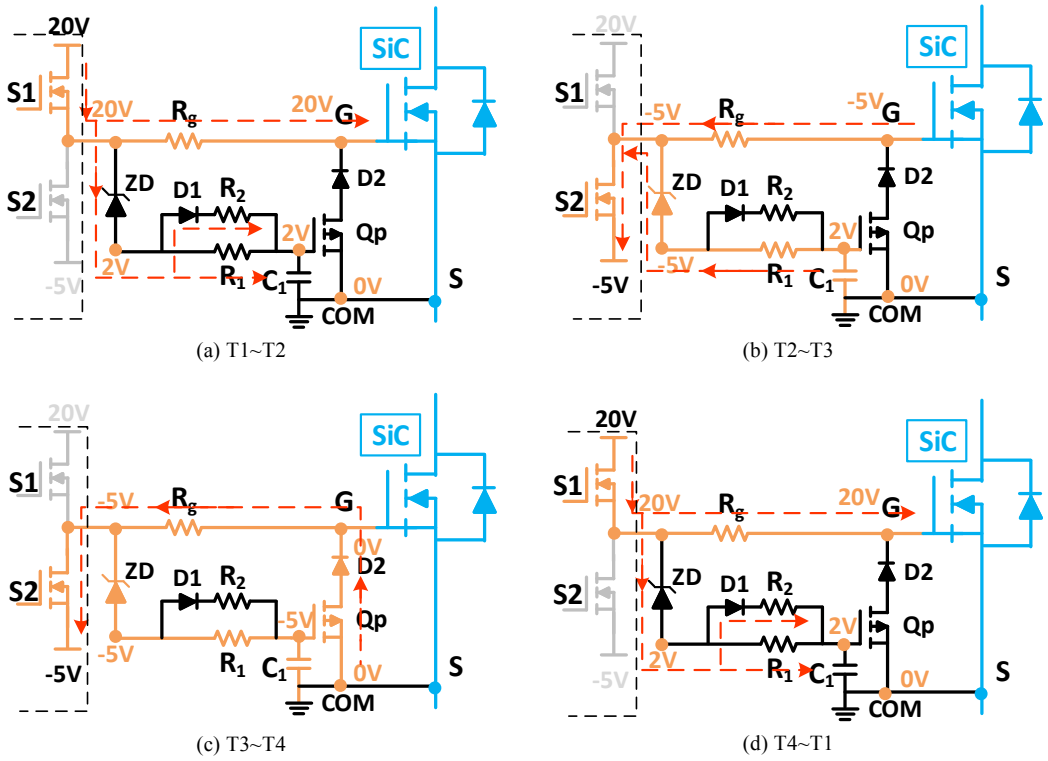


Figure 5 Operation principle for each stage, the time points T1~T4 shown in Figure 2

(a) T1~T2: the Vgs is in steady on-state with 20V voltage. The auxiliary circuit is blocked by D2 and Qp, the ZD is working at Zener diode breakdown voltage to limit the voltage across C1, protecting the gate of Qp from overvoltage.

(b) T2~T3: when turn-off gate signal comes, the -5V voltage connects through S2, the -5V voltage supply will discharge the SiC MOSFET gate-source capacitor (Cgs) and the auxiliary R1C1 circuit at the same time. Due to the R1C1 delay, before the voltage across C1 reaches Qp threshold

voltage, the SiC MOSFET gate voltage (Vgs) is already discharged to -5V, making the SiC MOSFET turn-off faster and mis-trigger harder.

(c) T3~T4: After T3 time point, the gate voltage of Qp reaches its threshold and Qp is turned on, clamping the SiC MOSFET Vgs to 0V by D2-Qp branch. Thus, before the next turn-on, a clamping circuit is connected directly from gate to source, the gate voltage is already 0V and is harder to exceed gate negative voltage limit. When turn-on gate signal comes, the Cgs voltage will be charged from 0V to 20V, which takes less time to turn-on than traditional gate driver (from -5V to 20V).

(d) T4~T1: Once the gate voltage becomes positive, the auxiliary D2-Qp branch will be blocked by the Schottky diode D2 immediately. The 20V power supply, at the same time, will charge the R2C1 circuit, the Zener diode ZD is in series with the RC circuit to limit the voltage on C1 lower than positive driving voltage (20V), protecting the P channel MOSFET from gate overvoltage breakdown. The steady state voltage on C1 is $V_{C1} = V_{cc}(20V) - V_{ZD}$ .Although D2 blocks the connection between gate and source, the auxiliary switch Qp still needs to be turned off as soon as possible, in order to prepare for the next Qp turn-on procedure. The Qp has the possibility to not be completely turned off due to the RC delay circuit, especially when the SiC has a short on period. If this happens, when the gate off signal comes, the Qp is still at on-state instead of being turned on after an expected RC time delay, which brings the gate voltage to zero level before the Vgs positive overshooting happens. The bad impact of this is that the positive spike will ride on a 0V Vgs rather an adequate negative level, which exposes the device in a much higher risk of mis-triggering. Therefore, a small RC time constant is still necessary for the Qp turn-off even though the D2 can block the positive voltage immediately. That is why a parallel gate path with R2 and D1 are used here. It will not affect the Qp turn-on time constant and turn-on/off time constants can be designed separately.

IV. DESIGN GUIDELINE FOR PROPOSED AUXILIARY CIRCUIT

4.1. RC circuit design

There are two different RC circuits in the auxiliary gate circuit: ON time RC circuit R1C1 and OFF time RC circuit (R1//R2)C1. These two time constant should be considered separately.

4.1.1. The ON time R1C1 circuit

The rise time of the R1C1 circuit Tr is equal to 3 times of the time constant T_{c1} for 95% voltage rise: $T_r = 3T_{c1} = 3R1 \times C1$. The rise time should fulfill the constraint EQ.1:

$$T_{set} < T_r < T_{off} \quad \text{(EQ.1)}$$

Where T_{set} represents the time period from the off gate signal falls under threshold to the end of the Vds dv/dt in the hard switching case (Figure 1(c)(d)), and the time period of the deadtime in the soft-switching case (Figure 1 (a)(b)). T_{off} refers to the minimum off-state period, which is usually depends on the modulation index or maximum duty cycle of the converter operation.

For example, in the SPWM application, there usually is minimum pulse and maximum pulse limitation. If the switching frequency is 1MHz, and the duty cycle is limited between 0.1~0.9. The minimum off time T_{off} is calculated as 100ns. Thus, the minimum T_{c1} is 33ns, and [R1, C1] can be [10ohm, 3.3nF].

Besides, the gate circuit time constant R1C1 affects the switching speed of the Qp, which is also the transition speed of the SiC MOSFET Vgs rising from -5V to 0V. The switching speed of the Qp heavily depends on its Vgs slew rate around the threshold point. A smaller time constant R1C1 leads to a higher Vgs slew rate thus creates a higher Vds dv/dt for the Qp. The total time cost for the gate of SiC MOSFET changing from -5V to 0V is composed of the R1C1 time delay (*Tr*) and the transition time of Qp. As discussed, the transition time of Qp is positively related to the *Tr*. Therefore, if the application needs a ultra-high switching frequency, the *Tr* should be designed as small as possible, for example, bounding the lower limit T_{set}.

4.1.2. The OFF time (R1//R2)C1 circuit

The off time constant should fulfill the constraint EQ.2:

$$3T_{c2} < T_{on} \tag{EQ.2}$$

Where T_{c2} is (R1//R2)C1 time constant and T_{on} is minimum on-state time per application.

When the turn-on transient comes, it is not necessary to turn off the auxiliary PMOS Qp immediately since the Schottky diode D2 will block the gate ON state voltage even though the Qp is still on. The (R1//R2)C1 time constant should guarantee that during the minimum SiC MOSFET Vgs on-state time (determined by the application minimum duty cycle), the PMOS Qp can be completely turned off before the next SiC turn-off transient, which means C1 finishes charging process to positive steady state voltage before the next turn-off transient. What is more, C1 value should be the sum of the Qp gate-source capacitor Cgs and the external capacitor.

4.1.3. R1, R2 design

After the ON/OFF time constant is determined, the resistor R1 and R2 values are mainly limited by the commercial gate driver pulse current limit. Different from conventional gate driver, the output current of the gate driver IC in the proposed flows into two parallel paths – one is the gate of the main SiC MOSFET, and another is the gate of the auxiliary switch Qp. The commercial gate driver current limit should be bigger than the sum of the SiC gate pulse current and auxiliary switching pulse current. The equations are:

$$\begin{cases} \dfrac{V_{cc}(20V)-V_{ZD}-V_{ss}(-5V)}{R1//R2}+\dfrac{V_{cc}(20V)}{R_g} \le I_{GD\_SOURCELimit} \\ \dfrac{V_{cc}(20V)-V_{ZD}-V_{ss}(-5V)}{R1}+\dfrac{V_{cc}(20V)-V_{ss}(-5V)}{R_g} \le I_{GD\_SINKLimit} \end{cases} \tag{EQ.3}$$

Where the $V_{cc}(20V)$ and $V_{ss}(-5V)$ are 20V/-5V gate driving voltage; V_{ZD} is Zener diode ZD breakdown voltage; $I_{GD\_SOURCELimit}$ is the gate driver IC output positive current pulse limit; $I_{GD\_SINKLimit}$ is the gate driver IC output negative current pulse limit. If the gate resistor of the main SiC MOSFET Rg is determined per application desired dv/dt, the R1 and R2 lower limit can be

calculated by EQ.3.Once the R1 and R2 is calculated, the capacitor C1 is determined per time constant T_{c1} and T_{c2} limitation.

4.2. Diode D2 and ZD selection

D2 is to block the SiC positive gate voltage, so D2 voltage rating should be larger than the gate absolute voltage (Vg++|Vg-|). And the Schottky diode is preferred since the reverse recovery loss is neglectable. When selecting the Schottky diode, the reverse static loss [10] is important parameter since it is directly related to the auxiliary circuit additional power loss.

ZD is to protect Qp gate from overvoltage breakdown. So, the Zener diode breakdown voltage V_{ZD} should fulfill the equation:

$$V_{cc} > V_{ZD} > V_{cc} - V_{Qp\_gs\max} \quad \text{(EQ.4)}$$

where $V_{Qp\_gs\max}$ is Qp maximum gate voltage; V_{cc} is gate absolute voltage difference ($\left|V_{g+}\right| + \left|V_{g-}\right|$). By this constraint equation EQ.4, the Qp gate voltage is guaranteed to be smaller than maximum gate voltage.

V. SMGD LOSS EVALUATION

By utilizing the auxiliary circuit, the driving loss will increase. The major driving loss of the auxiliary circuit is due to the loss of Rg during the 0V Vgs period, since the Rg is connected to the gate IC output directly through Qp. However, the effect of this additional power loss to the whole circuit depends on how much percentage this additional driving loss takes up in the circuit total power loss. According to calculation, this additional driving loss is only 16% of the original driving loss and moreover, the driving loss is less than 1% of the total power loss (including switching loss, conduction loss of the main devices). Therefore, the auxiliary circuit adds negligible loss to the circuit. The details of the calculation will be shown in the following paragraphs of this section.

Instead of lowering the efficiency, it is found that the proposed driving strategy actually helps significantly reduce the turn-on loss of the main SiC switch. By adding the additional zero level

for the gate voltage, the gate rises from 0V to 20V at the second stage instead of from -5V to 20V like the traditional case, which makes the gate current higher when the gate voltage reaches the threshold. The higher gate current means higher gate voltage slew rate [11~14], and it can push a higher dv/dt on the device, which in another word means lower switching loss. In section VII, the switching loss reduction will be evaluated.

The details of the calculation are as follows.

The traditional voltage source gate driver loss is calculated by EQ.5 [9]

$$P = Q_g \times (V_{g+} - V_{g-}) \times f_{sw} \quad \text{(EQ.5)}$$

Where Qg is gate total charge, V_{g+} / V_{g-} are on/off state gate voltage, and f_{sw} is switching frequency.

For the 1.2kV/60A SiC MOSFET C2M0040120D from Wolfspeed switching at 1MHz frequency, the driver loss is 2.875W per EQ.5. If higher current rating MOSFET is used, the gate total charge Qg will be bigger and the driver loss will be bigger (e.g. 4.025W driver loss for 1.2kV/90A MOSFET C2M0025120D).

The additional loss induced by the auxiliary circuit composed by three parts: 1. P-MOS Qp gate driving loss; 2. D2 reverse power loss; 3. Qp, D2, Rg conduction loss during clamping period.

1. For the ZD, D1, R1, R2 driving circuit, if Qp is FDN358P from ON Semiconductor, the loss per EQ.5 is $P_1 = 0.028W$.
2. If D2 is RB550VYM-30FHTR from ROHM semiconductor, the D2 reverse recovery loss can be neglected, and the static reverse power loss P_2 is 0.04W from datasheet [10].
3. The conduction loss during clamping is big, because the negative voltage is largely applied to gate resistor Rg. In proposed driver, the gate resistor is 10ohm and the negative voltage is -5V; the forward voltage-drop of Qp and D2 are 0.5V and 0.6V, respectively. So, the current Ig_clp can be calculated by:

$$I_{g\_clp} = \frac{5 - 0.5 - 0.6}{R_g} = 0.39A$$

Suppose the clamping time is one fourth of the total switching period, which means the clamping happens in the middle of the off-state, so the power loss is

$$P_3 = \frac{1}{4} I_{g\_clp} \times V_{g-} = 0.487W$$

So, the additional power loss induced by auxiliary circuit is

$$P_{loss} = P_1 + P_2 + P_3 = 0.555W$$

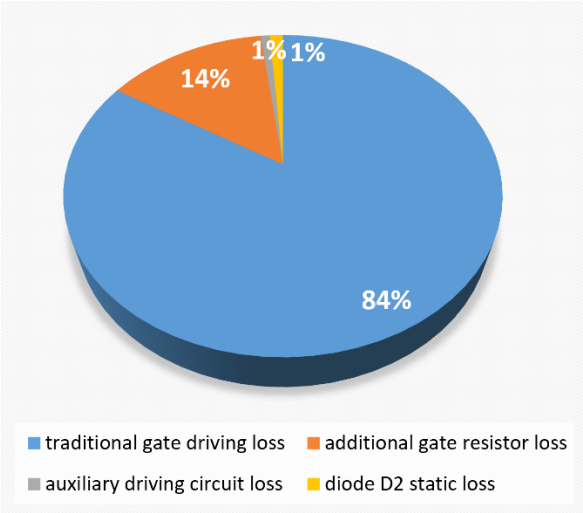
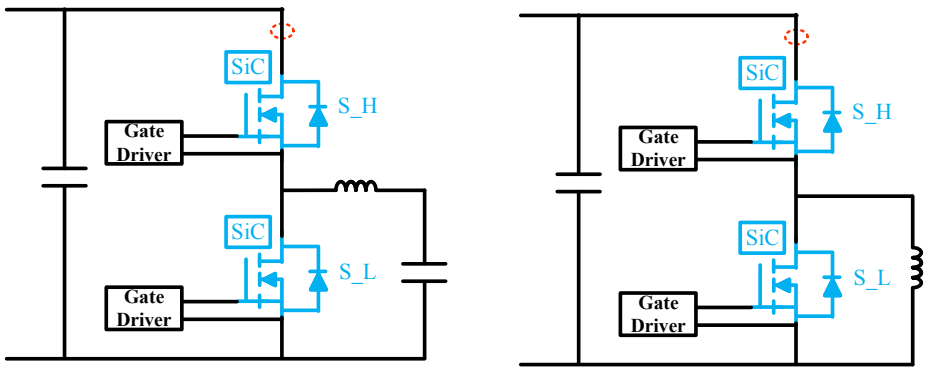


Figure 6 SMGD gate driving loss breakdown

The loss breakdown is shown in Figure 6. The additional gate driving loss accounts for 16% of the total driving loss after adding the auxiliary circuit for 1MHz switching frequency.

VI. LTSPICE SIMULATION RESULTS

In this section, two representative cases for phase-leg configuration, ZVS soft-switching and double pulse test are conducted, the schematics are shown in Figure 7.



(a) ZVS soft-switching (b) high-side switch double pulse test

Figure 7 schematics of SPICE simulations: (a) ZVS soft-switching; (b) high-side switch double pulse test

A. ZVS simulation results

The SPICE simulation using half bridge ZVS soft-switching is developed, corresponding to the case of Figure 1 (a)(b). Figure 8 shows the gate voltage waveforms with and without the proposed auxiliary circuit. Without auxiliary circuit, the Vgs waveforms of both upper and lower devices in the phase leg have negative overshooting voltage before the gate signal rise-up. There is a large negative overshooting during phase-leg deadtime period which could result in gate overvoltage breakdown. While using the auxiliary circuit, the negative overshooting voltage is almost clamped to 0V.

B. Double pulse test simulation results

Figure 9 shows the double pulse test simulation results, corresponding to the case of Figure1 (c)(d). The Vgs of device under test (red) has the miller plateau for both Vgs rising and falling edge because it is hard-switching, and the change of Vds depends on this device signal. And the complementary switch Vgs (blue) has possible mis-trigger issue after Vgs falling edge. Without auxiliary circuit, as shown in Figure 9(a), the Vgs negative overshooting reaches -9V. With auxiliary circuit, as shown in Figure 9(b), the negative overshooting nearly disappears. From the simulation, the transition time is around 100ns.

The crosstalk suppression capability of this auxiliary circuit is verified for both case 1 in Figure 1(a)(b) and case 2 in Figure 1(a)(d)/(b)(c) applications in section III. The simulation and hardware components part number are listed in Table II.

Table II components list for auxiliary circuit

LABEL	COMPONENT	PART #
ZD	18V Zener diode	TDZV18B
D1, D2	Schottky diode	RB550VYM-30FHTR
Qp	P-channel MOSFET	FDN358P
Rg	Gate resistor	10ohm
R1,R2	Auxiliary circuit resistor	20ohm
C1	Auxiliary circuit capacitor	4.7nF

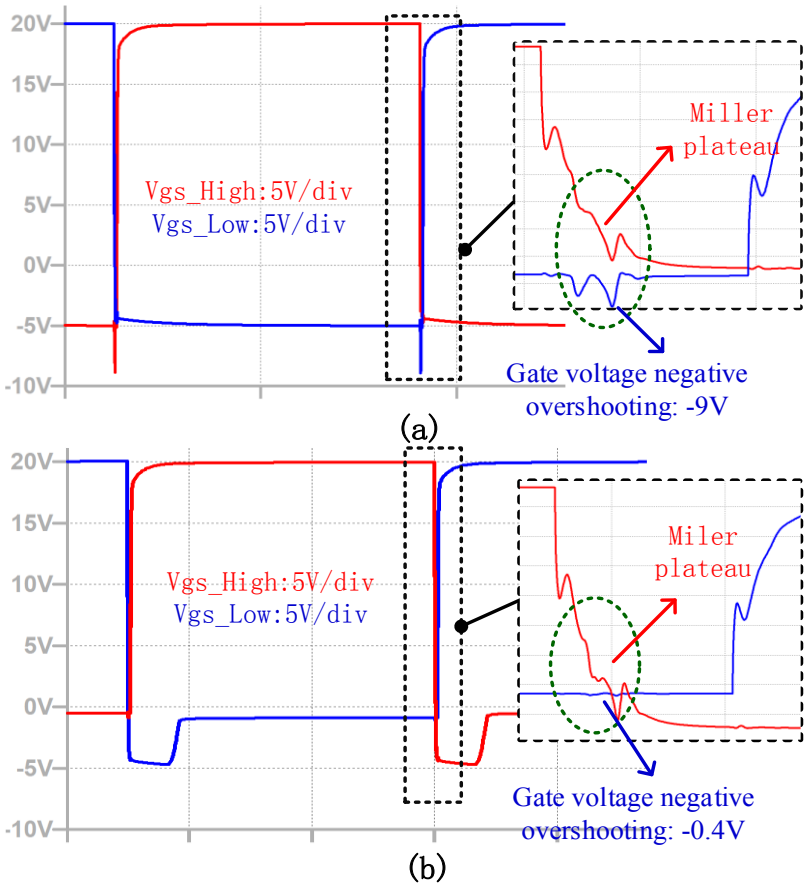
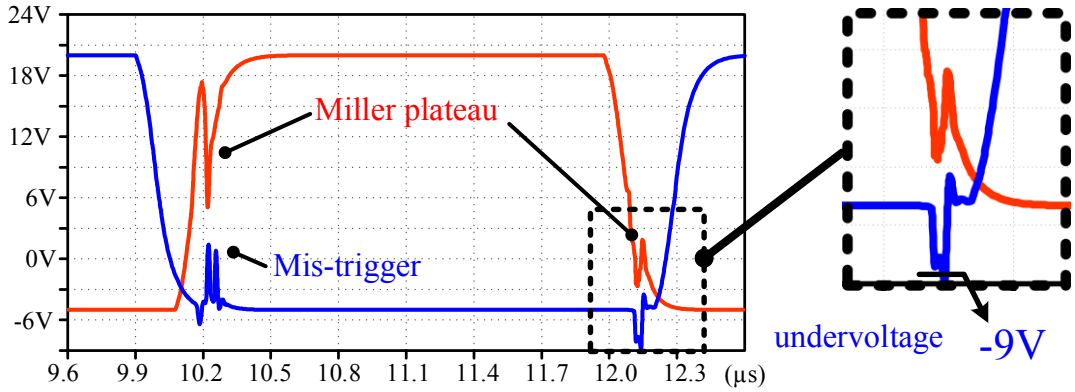
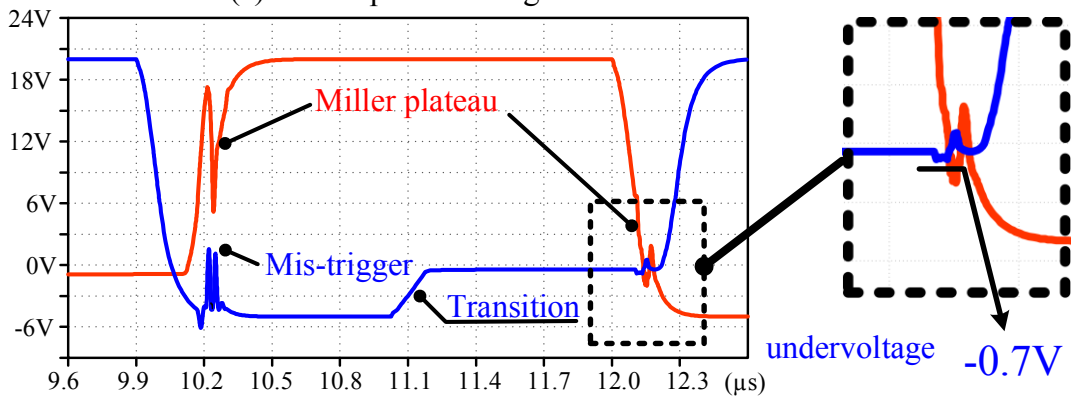


Figure 8 ZVS simulation results: (a) without proposed auxiliary circuit, the high-side and low-side MOSFET Vgs waveforms; (b) with proposed auxiliary circuit, the high-side and low-side MOSFETs Vgs waveforms



(a) double pulse test Vgs waveforms without SSGD



(b) double pulse test Vgs waveforms with SSGD

Figure 9 double pulse test simulation results: (a) without proposed auxiliary circuit, the high-side and low-side MOSFET Vgs waveforms; (b) with proposed auxiliary circuit, the high-side and low-side MOSFETs Vgs waveforms

VII. Experiment Results Analysis

A gate driver board with proposed auxiliary circuit is developed, and the picture of gate driver auxiliary circuit is shown in Figure 10. The gate signal of SiC MOSFET and auxiliary circuit P-MOS Vgs waveforms before the main power is on are shown in Figure 11. A zero level gate voltage is created for the SiC MOSFET in the middle of the off period, right after the gate voltage of the auxiliary PMOS Qp (negative gate voltage driving) reaches its threshold. The RC time constant controls the start time of the zero gate voltage. The rise time from -5V to 0V for SiC gate voltage is around 100ns.

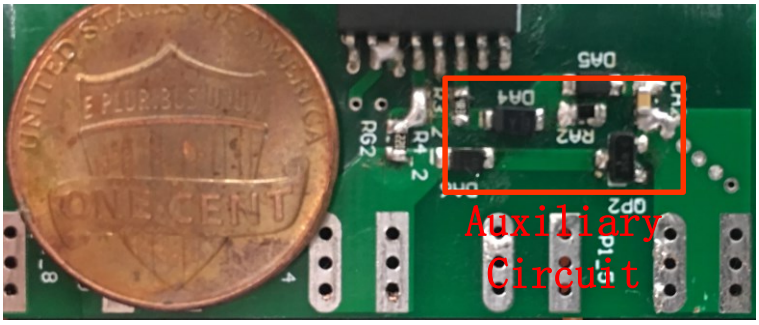


Figure 10 gate driver hardware picture

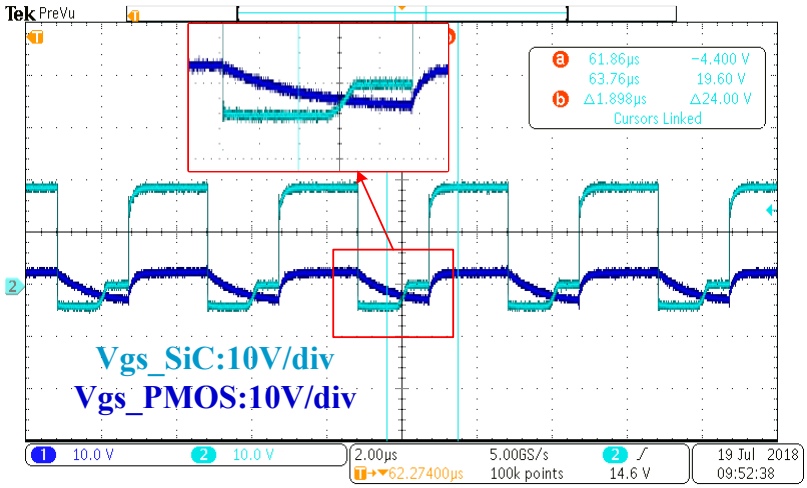


Figure 11 SiC MOSFET Vgs waveform (light blue) and PMOS Vgs waveform (dark blue)

A double pulse test is conducted using half bridge circuit, as shown in Figure 7(b). The test setup is shown in Figure 12. In this double pulse test, the commercial gate driver is ADuM4135 from Analog Device, and the power device is C2M0040120D from Wolfspeed. The device under test (DUT) is the high side SiC MOSFET, and the low side SiC MOSFET is in parallel with the inductor. Three gate driver configurations - traditional gate driver without Schottky diode clamping, gate driver with Schottky diode clamping and SMGD, are implemented to verify the effectiveness of the proposed SMGD.

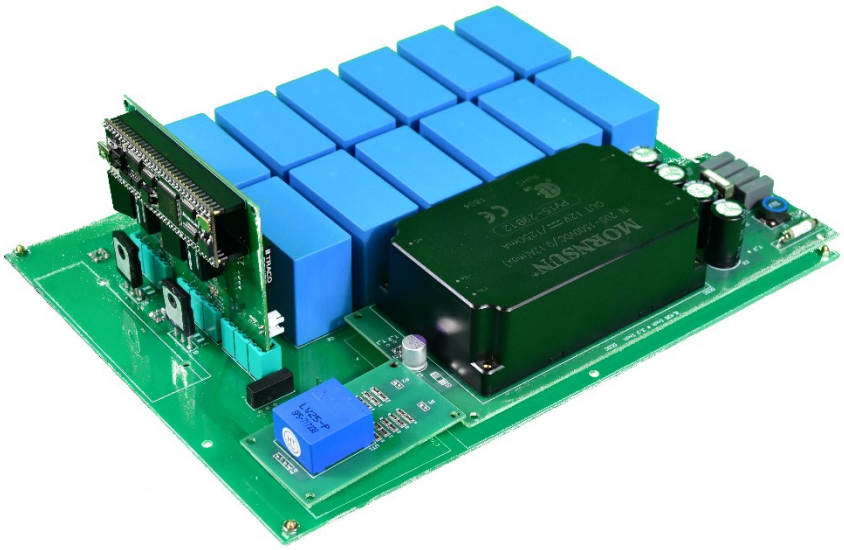


Figure 12 double pulse tester setup

In the double pulse test, the gate resistor value and the other power loop parameters are the same for three configurations The double pulse test condition is 850V dclink voltage and 60A device current for 1200V/60A SiC device. Under this full rating (or even excessive rating) voltage and current, the device will exhibit the maximum dv/dt which will expose the gate to the highest risk of mis-triggering or negative over-voltage breakdown. If under this extreme case, the proposed strategy can help mitigate the risk significantly, it is persuasive to claim the proposed method is effective under the full operation region. Figure 13 shows the double pulse test results of the original gate driver configuration. For the high-side device turn-off transient, the Vds dv/dt is 35.26V/ns and the Ids di/dt is 1.1A/ns. The high dv/dt results in huge crosstalk effect, which makes the low-side Vgs undershooting reach -9.9V, close to the datasheet stated minimum allowable gate voltage “-10V”. This undershooting voltage makes the device vulnerable to the gate breakdown. When the Schottky diode clamping technique is used, as shown in Figure 14, the undershooting voltage is reduced to -7.8V. The amplitude of the undershooting voltage is reduced, but with limited extent, so the risk of gate breakdown still exists, especially under long time operation. Figure 15 shows the results of the proposed SMGD. The gate voltage undershooting is significantly alleviated. The negative voltage

is only -1.8V at Vds dv/dt 35.57V/ns. The transition time of the gate voltage from -5V to 0V is around 100ns. Different from the aforementioned two methods, the proposed SMGD completely saves the device from negative over-voltage breakdown on the gate, showing a transformative solution rather than an additive improvement. With this solution, the device dv/dt can be raised up significantly since the risk of gate mis-triggering or negative breakdown is significantly mitigated. In another word, an important obstacle to stretch the SiC MOSFET to its speed limit has been extenuated in a large extent by the proposed method. Besides, by implementing the SMGD, the DUT (high-side device) turn-on Vds dv/dt is increased which means for the same operation condition, the switching performance of the SMGD is improved and the switching loss is reduced. From the switching loss point of view, the DUT turn-off loss should be similar because the turn-off Vgs waveforms are the same for three gate driver configurations. But turn-on loss of the SMGD will be smaller than the other two. The key parameters and the Eon/Eoff are shown in Table III to verify this. The Eon reduces 60uJ for each switching cycle of SMGD. And the additional gate driving loss introduced by SMGD is neglectable compared with the total loss of the circuit. Therefore, the proposed SMGD can reduce the total loss.

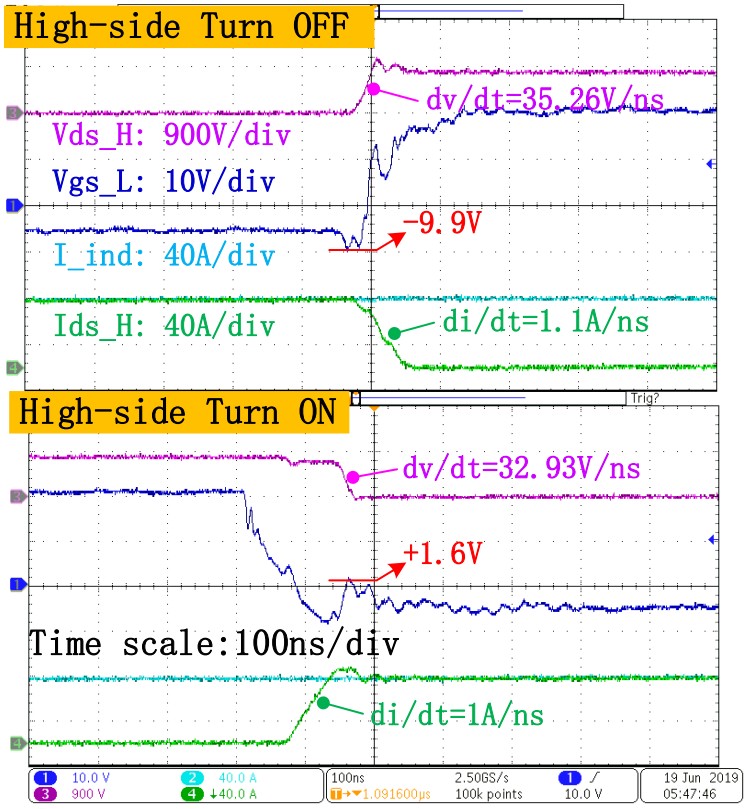


Figure 13 850V/60A double pulse test waveforms: original gate driver configuration without diode clamping. The Vds_H represents high side device drain-source voltage; the Vgs_L is the low side device gate-source voltage; the I_ind is the inductor current; the Ids_H is the high_side drain-source current.

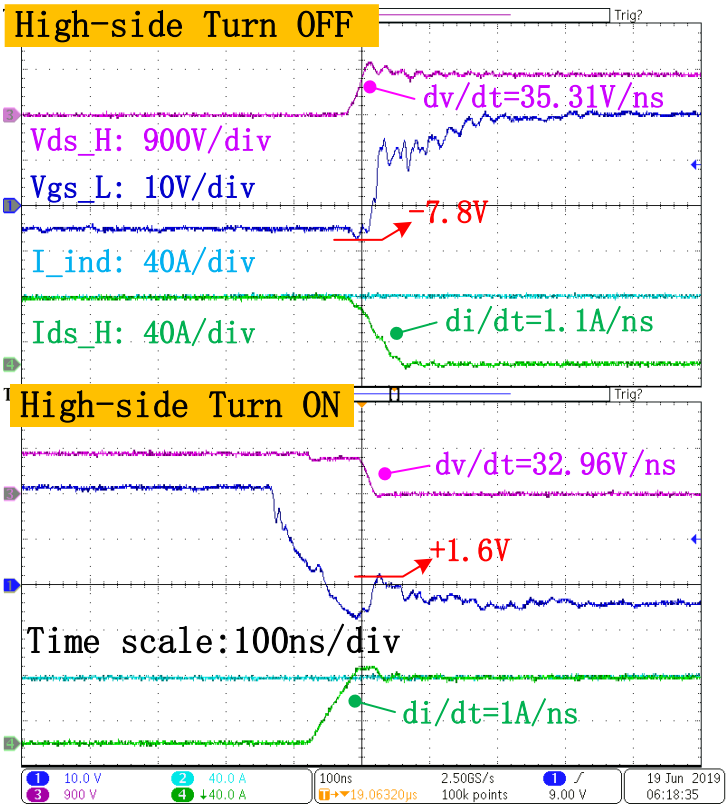


Figure 14 850V/60A double pulse test waveforms: original gate driver configuration with diode clamping. The Vds_H represents high side device drain-source voltage; the Vgs_L is the low side device gate-source voltage; the I_ind is the inductor current; the Ids_H is the high_side drain-source current.

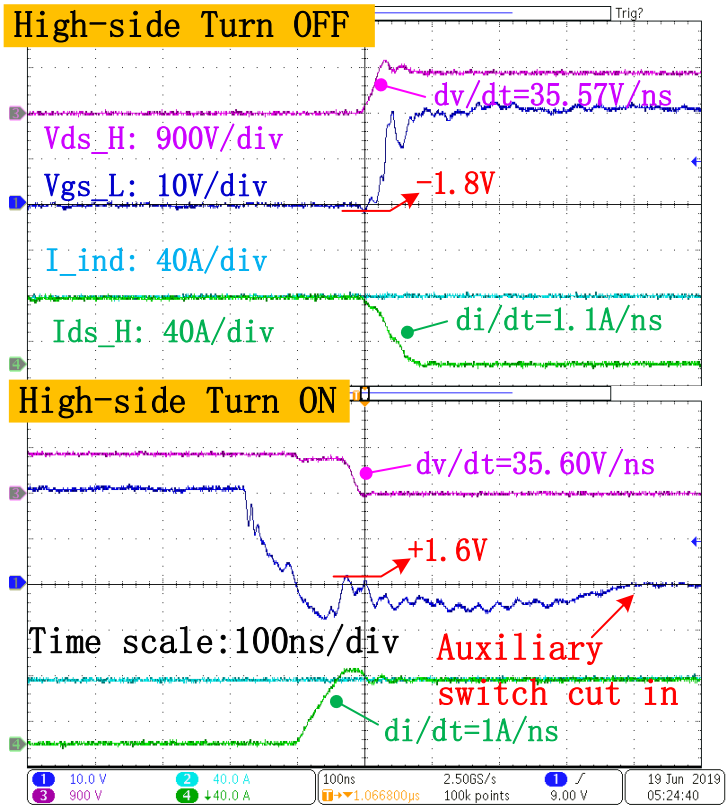


Figure 15 850V/60A double pulse test waveforms: proposed smart self-driving gate driver configuration. The Vds_H represents high side device drain-source voltage; the Vgs_L is the low side device gate-source voltage; the I_ind is the inductor current; the Ids_H is the high_side drain-source current.

Table III 850V/60A double pulse test results of three gate driver configurations

GD configuration	Original GD	Original GD w/ diode clamping	Proposed SSGD
Turn ON dv/dt (V/ns)	32.93	32.96	35.60
Turn OFF dv/dt (V/ns)	35.26	35.31	35.57
Mis-trigger Vgs (V)	+1.5	+1.6	+1.6
Undervoltage Vgs (V)	-9.9	-7.8	-1.8
Turn ON di/dt (A/ns)	1.1	1.1	1.1
Turn OFF di/dt (A/ns)	1	1	1
Eon of DUT (mJ)	2.4174	2.4196	2.3450
Eoff of DUT (mJ)	1.4201	1.4173	1.4194

VIII. CONCLUSIONS

The wide band gap device can switch at much higher speed (dv/dt and di/dt) than Si device. This brings many benefits at system level in terms of efficiency and power density. But the high switching speed can cause problems such as EMI, Vds over-voltage, gate breakdown or gate mis-triggering, and so on. . In this paper, a smart self-driving multi-level gate driver is proposed to solve the issue of high dv/dt caused gate mis-triggering and negative over-voltage breakdown. By inserting a zero level in the gate voltage during the off period, the first portion of the gate voltage can be designed more negative to avoid the mis-triggering, and more important, the negative overshooting in the second portion of the off period can occur based on the zero voltage level instead of a very negative voltage level to avoid the negative breakdown of the gate. When designing the circuit, the circuit complexity is significantly reduced by utilizing the original gate voltage as the trigger of the auxiliary circuit, intead of utilizing independent gate driving circuit and isolation stages. The proposed circuit is easy to be integrated with the commercial gate driver to form the complete three-level gate driver. The proposed gate driver is highly efficient and highly compact, as well as cost-effective.

REFERENCES

[1] J. Biela, M. Schweizer, S. Waffler and J. W. Kolar, "SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC–DC Converter Systems by SiC Power Semiconductors," in IEEE Transactions on Industrial Electronics, vol. 58, no. 7, pp. 2872-2882, July 2011.

[2] C. Liu and Q. Lei, "Design Considerations and Performance Test for SiC MOSFET Based 1000V / 1.5MHz Pulse Power Inverter," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 6641-6645.

[3] Z. Zhang, W. Zhang, F. Wang, L. M. Tolbert and B. J. Blalock, "Analysis of the switching speed limitation of wide band-gap devices in a phase-leg configuration," 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, 2012, pp. 3950-3955.

[4] Z. Zhang, J. Dix, F. F. Wang, B. J. Blalock, D. Costinett and L. M. Tolbert, "Intelligent Gate Drive for Fast Switching and Crosstalk Suppression of SiC Devices," in IEEE Transactions on Power Electronics, vol. 32, no. 12, pp. 9319-9332, Dec. 2017.

[5] C. Liu and Q. Lei, "Smart current source gate driver for fast switching and cross-talk suppression of SiC MOSFET," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 2734-2739.

[6] Alan Elbanhawy, Fairchild Semiconductor, "AN-7019: Limiting Cross-Conduction Current in Synchronous Buck Converter Designs".

[7] Huang, Xiucheng. High frequency GaN characterization and design considerations. Diss. Virginia Tech, 2016.

[8] "Infineon EiceDRIVER 1ED020I12 single IGBT Driver IC". [online] Available: https://www.infineon.com/dgdl/Infineon1ED020I12F2DataSheetv02_01EN.pdf?fileId=db3a304330f68606013122ce5f3649cb
[9] Lakkas, George. "MOSFET power losses and how they affect power-supply efficiency." Analog Appl 10 (2016): 22-26.
[10] ROHM Semiconductor, RB550VYM-30FHTR datasheet, April. 2017._Rev.001. [online] Available: http://rohmfs.rohm.com/en/products/databook/datasheet/discrete/diode/schottky_barrier/rb550vym-30fhtr-e.pdf
[11] Z. Chen, "Characterization and modeling of high-switching-speed behavior of SiC active devices," M.S. thesis, Dept. Electrical Eng., Virginia Tech., Blacksburg, VA, USA, 2009.
[12] J. McBryde, A. Kadavelugu, B. Compton, S. Bhattacharya, M. Das, and A. Agarwal, "Performance comparison of 1200V silicon and SiC devices for UPS application," in Proc. 36th Annu. IEEE IECON, Glendale, AZ, USA, Nov. 2010, pp. 2657–2662.
[13] B. Callanan, "Application considerations for silicon carbide MOSFETs", Cree Inc., Durham, NJ, USA, Appl. [online]. Available: https://www.mouser.com/pdfDocs/Cree-Application-Considerations-for-Silicon-Carbide-MOSFETs.pdf
[14] P. Anthony, N. McNeill and D. Holliday, "High-Speed Resonant Gate Driver With Controlled Peak Gate Voltage for Silicon Carbide MOSFETs," in IEEE Transactions on Industry Applications, vol. 50, no. 1, pp. 573-583, Jan.-Feb. 2014.
[15] Williams, Richard K. "Power MOSFET having voltage-clamped gate." U.S. Patent No. 6,172,383. 9 Jan. 2001.
[16] Toshiba Application Note "MOSFET Gate Drive Circuit." Jul.2018. [online]. Available: https://toshiba.semicon-storage.com/info/docget.jsp?did=59460