Analog to Digital Feature Converter based on Oversampling Modulators for ECG Delineation

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***Abstract*— We present an Analog to Digital Feature Converter system based on oversampling modulators. The system consists of a Delta Sigma Modulator, two Delta Modulator, and one Second-order Delta Modulator in parallel. The goal of the Analog to Digital Feature Converter is to extract the waveform features from the analog signal during analog to digital conversion to save system power. We demonstrated this system in an example application of electrocardiogram (ECG) delineation with a counting based feature extraction algorithm. Compared the conventional ECG delineation methods using wavelet transform, the proposed method has much lower power consumption for data conversion and computation.**

***Index Terms*—Analog to Digital Feature Converter, Oversampling Modulators, Feature extraction, ECG delineation.**

I. Introduction

Future wearable wireless biomedical sensors demand novel technologies to overcome the increasing challenge in implementing intelligent signal sensing and processing and the shortage of battery lifetime [1]. Such devices are expected to provide automatic monitoring and processing of physiological signals, and be capable of identifying abnormal signals and contacting medical systems if necessary [2]. Wearable Electrocardiogram (ECG) sensor [3] is one of the important wearable medical devices for arrhythmia detection. However, most of the current solutions on ECG monitoring lack local signal processing capabilities on the wearable sensor and heavily rely on wireless data communication [4], [5] and the remote processing, which is power hungry and brings the security, privacy and latency issues. The reason is that on-sensor ECG signal analysis is power hungry due to the high computing overhead of the circuits and systems that performs the digital signal processing algorithms. For example, researches [6], [7], achieve high-performance classifiers, but are not suitable to be implemented on the wearable sensors due to the high computing overhead.

Machine learning is a promising solution and has recently been applied to continuous monitoring of physiological signals for on-sensor processing [8]. The wearable sensors need to keep the power consumption at the level of milliwatts (mW) or less in order to keep a reasonable battery lifetime. However, the implementation of deep learning inference using neural network would consume hundreds of mW due to the intensive multiply-and-accumulate (MAC) operations and the data movement between memory and the processing unit [9]. Therefore, a machine learning algorithm that can accommodate real-time processing without too much data storage and movement is preferred in wearable sensor applications. One of the most power-hungry parts in machine learning is feature extraction, which requires extracting key features of the input analog signal. The features should be in digital format since most of machine learning systems are implemented in digital. To address this issue, one idea is to extract the features during data conversion. However, current Nyquist rate analog to digital converter (ADC) are converting data by sampling, which does not have the capability of extracting features. In order to extract features, the samples should be compared with its neighboring samples. Oversampling data conversion meets this requirement.

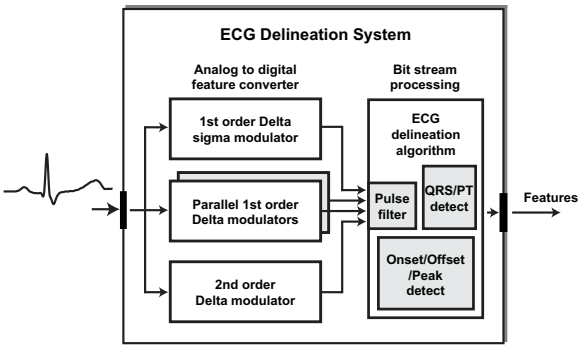

Fig. 1. Diagram of the proposed Oversampling based Analog to Digital Feature Converter with bit-stream processing algorithm.

Compared to the conventional ADC [10], which focuses on preserve the signal quality in the digital domain so that the reconstruction of the analog signal is accurate, our proposed analog to digital feature converter (ADFC) emphasis on extracting the features from the analog signal during analog to digital conversion, without considering signal reconstruction. Our goal is to find an alternative analog to digital architecture to adapt hardware friendly algorithm for power limited sensors so that machine learning algorithms can be applied.

II. Systems and Circuits Design

The proposed ADFC consists of parallel oversampling modulators including the Delta Sigma modulator, the Delta modulator, and the second-order Delta Modulator as shown in Fig. 1. The oversampling modulators generate digital bit-streams from the analog waveform. The bit-streams are pulse-density modulation of the analog features. For example, the pulse density of the Delta-Sigma modulator output is proportional to the amplitude of the analog waveform, while the pulse density of the Delta modulator and the second-order Delta modulator

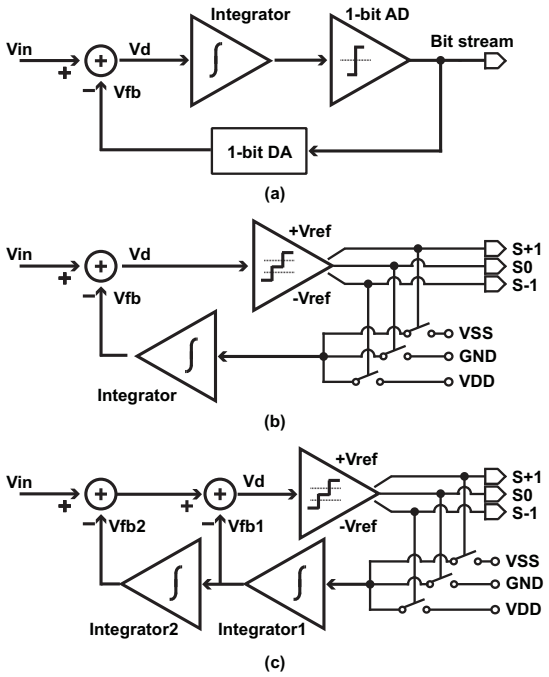

Fig. 2. Schematic of the Oversampling Modulators (a) Delta Sigma modulator; (b) Delta modulator; (c) Second-order Delta modulator.

are proportional to the derivative and the second derivative of the analog waveform, respectively. Therefore, using the combination of the oversampling converters, the amplitude, slope, and turning points of the analog waveform can be identified using a counter that counts the number of pulses in a pre-defined timing window.

The topology of the Delta-Sigma modulator and the first and second Delta modulators are shown in Fig. 2. In order to save system power, the Delta modulators are modified into a ternary architecture as we reported in [11]. In the modulator circuits, The discrete switched capacitor integrator generates the feedback voltage, which is subtracted from the input, then a three state comparator detects the residue voltage and controls the switches to feed the according voltage to the integrator for generating the feedback. The proposed second-order Delta modulator is similar to the first order Delta modulator in [11], while the residue voltage Vd is now generated by Vin subtracting the sum of the outputs from both the integrators. The Delta Sigma modulator [12] is achieved by a simple topology like in [13].

The behavior of the ternary Delta modulator and the second-order Delta modulator is simulated in Fig. 3. The Delta modulator detects the slope of the input waveform. If the input has a rising slope, the output generates a positive bit-stream and vice versa. While the second-order Delta modulator detects the turning point of the input waveform. When there is an upward turning point, the output generates a positive bit-stream where the first positive bit represents the moment of the turning point. Thus, the second-order Delta modulator can be used to detect the onset, peak and end point of the input waveform. Fig. 3 (a) shows the first order Delta modulator's outputs for ramp signals with different slopes. A larger slope

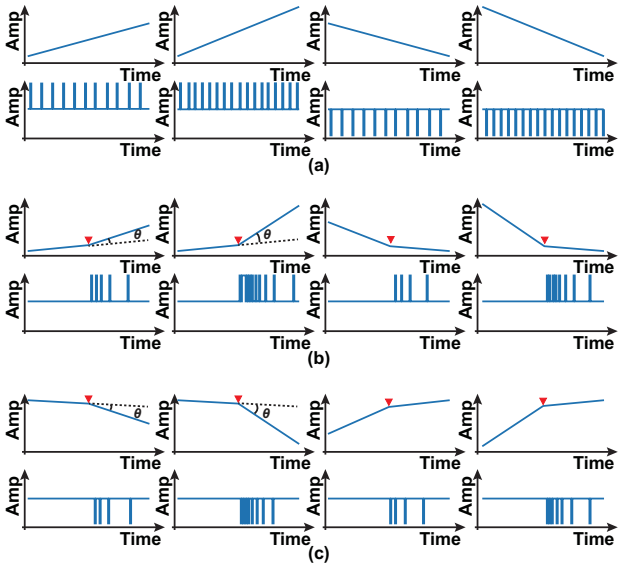

Fig. 3. Example input/output waveform of the first and second-order Delta modulators. (a) First order Delta modulator with input of ramp signals; (b) Second-order Delta modulator with input of upward turning points; (c) Second-order Delta modulator with input of downward turning points.

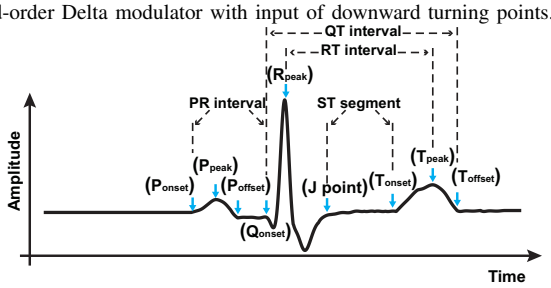

Fig. 4. The definition of onset, peak, and end of each wave, as well as the segment and intervals in ECG signal.

in the input signal generates a higher density in the output pulses and vice versa. Fig. 3 (b) and (c) illustrates the second-order Delta modulator's output signals with different upward and downward turning angles of the input waveform. A larger upward or downward turning angle (θ) produce a higher pulse density at the positive or negative output, respectively.

The design parameters of the oversampling modulators include the sampling rate, the bandwidth, the integration gain, the threshold voltages, and the reference voltage. Due to the space limit, we plan to introduce the systematic design method in another paper. Since the oversampling modulators generate only one bit at a time, the total power consumption is much lower than a conventional multi-bit ADC. Given the fact that biomedical signal acquisition and processing usually require oversampling [8], the parallel architecture of the oversampling modulators can extract digital features directly from the analog waveform during the analog to digital conversion, which costs less power than the combined power of the conventional ADC and its following digital signal processing circuits.

III. ECG Delineation Algorithm

One application example of the proposed ADFC is ECG delineation. ECG delineation detects the timing information of the peak, onset, and end points of different ECG waves,

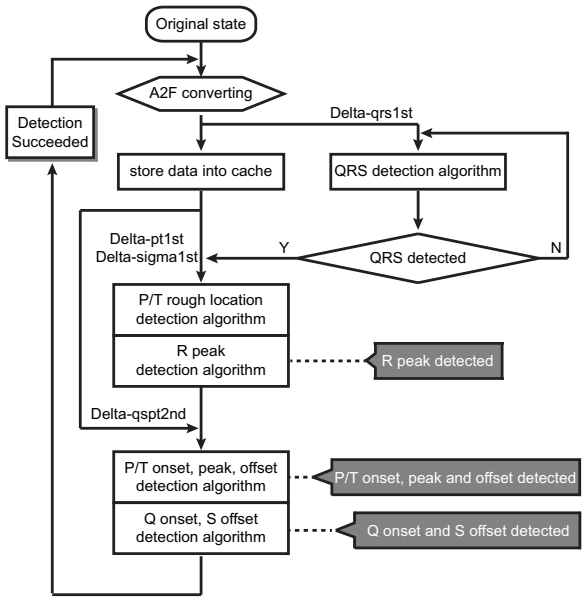

Fig. 5. The operation flow of the proposed bit-stream feature extraction algorithm.

including P, Q, R, S, and T waves, in order to measure the intervals and segments between these waves, which is shown in Fig. 4. During delineation, the detection of the QRS complex is one of the most important tasks because the QRS complex indicates the contraction process of the ventricles. Besides the QRS complex, the P wave and T wave detection also play very important roles in extracting the features, since P wave indicates that if the heartbeat is initiated by the sinus node while the end of T wave shows the repolarization of the ventricles. Moreover, the PR/RT/QT intervals and the ST segment have strong relationships with diagnosing some arrhythmia [14]–[16].

The proposed system contains four parallel oversampling modulators. The Delta Sigma modulator $Delta-sigma1st$, the second-order Delta Modulator $Delta-qspt2nd$, and the two Delta modulator $Delta-qrs1st$ and $Delta-pt1st$ with different integration gain for detecting the QRS and the P/T waves, respectively. The delineation algorithm is presented in Fig. 5. In the first step, the QRS complexes are detected by the Delta modulator $Delta-qrs1st$ with the QRS detection algorithm proposed in [11]. The main idea is to find the waves that meet the defined requirement of the slope. In the second step, the Delta modulator $Delta-pt1st$ starts to search back to find the rough P wave location, and wait for detecting the T wave location. Meanwhile, a moving average value register records the maximum point in the QRS detection area from the bit-stream of the Delta Sigma modulator $Delta-sigma1st$. Then, the onset, peak, and the end point of the P/T wave, as well as the onset of Q wave, and the end point of S wave are detected by the second-order Delta modulator $Delta-qspt2nd$ since the second-order Delta modulator is good at detecting the turning point of the input waveform. A pulse filter using erosion and dilation algorithm is designed for reducing the disturbance of small waves, noise, or baseline drift for the

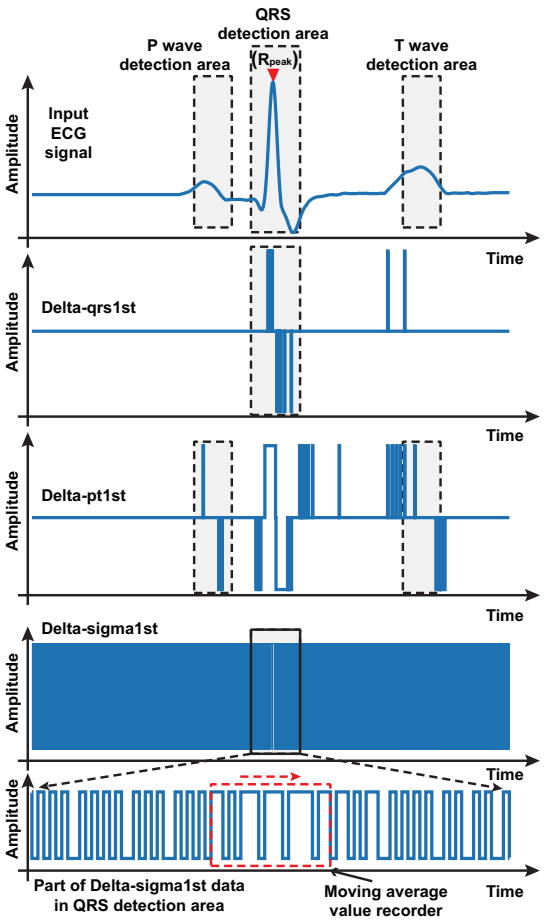

Fig. 6. Simulation results of the Delta Sigma modulator and the parallel first order Delta modulators with an ECG signal input.

oversampling modulators.

The bit-stream processing algorithm is based on counting the number of pulses in a moving window, without performing addition and multiplication such as in the wavelet transform algorithm. The features extracted from the counting results can be used in machine learning algorithms like support vector machines. The digital counting circuits use much less power than the MAC circuits at the same clock frequency. This is another benefit of using the ADFC.

IV. Simulation Result and Power Estimation

We simulate the system with an input of a typical ECG signal. The operating frequency of all the oversampling modulators is set to 1 kHz. From the simulation results as shown in Fig. 6, we can see that the QRS complex is detected by $Delta-qrs1st$ and the proposed algorithm, while $Delta-pt1st$ detects P/T waves and $Delta-sigma1st$ identifies the peak of the R wave. Q wave onset is decided by the first downward turning point in the QRS detection area from the bit-stream of $Delta-qspt2nd$, and the J point (S wave offset) is located at the first downward turning point after consecutive upward turning points of the R-S segment as shown in Fig. 7. Onset, peak and end point of P/T waves can also be clearly identified from bit-stream of $Delta-qspt2nd$ in P/T wave

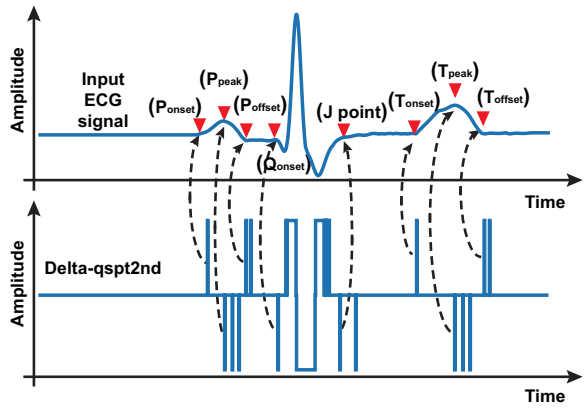

Fig. 7. Simulation results of the second-order Delta modulator in detecting onset, peak and end points of the ECG signal input.

detection area. With the information of onset, peak and end point of each wave, we can obtain PR/RT/QT intervals and the ST segment data.

The power consumption of the proposed Analog to Digital Feature Converter is estimated based on the fabricated Delta modulators using IBM 0.13 μm technology [11]. The two Delta modulators consume 720 nW with a $\pm$0.6V power supply and work at 1k Hz. For the second-order Delta modulator, since the second stage integrator cost approximately 50% power of the first stage integrator, the second-order Delta modulator is expected to consume 540 nW. Because the Delta Sigma modulator has almost the same main circuit block to the Delta modulator, we estimate the total power of the proposed converter as 1.62 μW. Compared to the ECG delineation system that applied Pan and Tompkins (PAT) algorithm and realized in 65 nm technology [17], which consumes 614 μW, or system with digital wavelet transform (DWT) based ECG delineation algorithm that is achieved in a microcontroller [18], which consumes minimum 6.6 mW, our proposed system can achieve much lower power and has great potential for future low-power wearable ECG sensors.

V. Conclusion

An analog to digital feature converter which is aimed at providing a low-power feature extraction method for machine learning on wearable ECG sensors has been presented. The proposed system includes parallel Delta-sigma modulator, two ternary Delta modulators, and a ternary second-order Delta modulator, which can extract features such as the peak, onset, end point, slope, and turning angle of the analog waveform. An example application of ECG delineation demonstrated the feasibility of the ADFC with the delineation algorithm. The simulation results show that the key measurement of ECG waveform is able to be performed with much lower power compared to the existing solutions. The system has a great potential for future wearable ECG monitoring sensors.

VI. Acknowledgment

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References

[1] Y. Liu, P. M. Furth, and W. Tang, "Hardware-efficient delta sigma-based digital signal processing circuits for the internet-of-things," *Journal of Low Power Electronics and Applications*, vol. 5, no. 4, pp. 234–256, 2015. [Online]. Available: http://www.mdpi.com/2079-9268/5/4/234

[2] V. Sai and M. Mickle, "Exploring Energy Efficient Architectures in Passive Wireless Nodes for IoT Applications," *IEEE Circuits and Systems Magazine*, vol. 14, no. 2, pp. 48–54, Secondquarter 2014.

[3] X. Zhang, Z. Zhang, Y. Li, C. Liu, Y. X. Guo, and Y. Lian, "A 2.89 μW Dry-Electrode Enabled Clockless Wireless ECG SoC for Wearable Applications," *IEEE journal of solid-state circuits*, vol. 51, no. 10, pp. 2287–2298, 2016.

[4] Q. Hu, Y. Chen, J. Kliewer, and W. Tang, "Asynchronous communication for wireless sensors using ultra wideband impulse radio," in *2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug 2015, pp. 1–4.

[5] Q. Hu, X. Tang, and W. Tang, "Integrated asynchronous ultrawideband impulse radio with intrinsic clock and data recovery," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 4, pp. 416–418, April 2017.

[6] P. Li, Y. Wang, J. He, L. Wang, Y. Tian, T.-s. Zhou, T. Li, and J.-s. Li, "High-performance personalized heartbeat classification model for long-term ECG signal," *IEEE Transactions on Biomedical Engineering*, vol. 64, no. 1, pp. 78–86, 2017.

[7] S. S. Xu, M.-W. Mak, and C.-C. Cheung, "Towards end-to-end ECG classification with raw signal extraction and deep neural networks," *IEEE journal of biomedical and health informatics*, 2018.

[8] J. Yoo, L. Yan, D. El-Damak, M. A. B. Altaf, A. H. Shoeb, and A. P. Chandrakasan, "An 8-Channel Scalable EEG Acquisition SoC With Patient-Specific Seizure Classification and Recording Processor," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 1, pp. 214–228, Jan 2013.

[9] V. Sze, Y.-H. Chen, J. Emer, A. Suleiman, and Z. Zhang, "Hardware for machine learning: Challenges and opportunities," in *Custom Integrated Circuits Conference (CICC), 2018 IEEE*. IEEE, 2018, pp. 1–8.

[10] H. Yu, W. Tang, M. Guo, and S. Chen, "A two-step prediction adc architecture for integrated low power image sensors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 1, pp. 50–60, Jan 2017.

[11] X. Tang, Q. Hu, and W. Tang, "A Real-Time QRS Detection System With PR/RT Interval and ST Segment Measurements for Wearable ECG Sensors Using Parallel Delta Modulators," *IEEE transactions on biomedical circuits and systems*, vol. 12, no. 4, pp. 751–761, 2018.

[12] X. Tang, Q. Hu, and W. Tang, "Deltasigma encoder for low-power wireless bio-sensors using ultrawideband impulse radio," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 7, pp. 747–751, July 2017.

[13] C. Qian, J. Shi, J. Parramon, and E. Sánchez-Sinencio, "A low-power configurable neural recording system for epileptic seizure detection," *IEEE transactions on biomedical circuits and systems*, vol. 7, no. 4, pp. 499–512, 2013.

[14] A. D. Krahn, G. J. Klein, and R. Yee, "Hysteresis of the RT interval with exercise: a new marker for the long-QT syndrome?" *Circulation*, vol. 96, no. 5, pp. 1551–1556, 1997.

[15] T. Kobayashi, M. Watanabe, Y. Kokubo, S. Kamakura, K. Kusano, and Y. Miyamoto, "Prolonged PR interval is significantly associated with increased risk of cardiovascular diseases and strokes in a population-based cohort study," *Circulation*, vol. 130, no. suppl_2, pp. A13 451–A13 451, 2014.

[16] W. Shimizu, C. Antzelevitch, K. Suyama, T. Kurita, A. Taguchi, N. Aihara, H. Takaki, K. Sunagawa, and S. Kamakura, "Effect of sodium channel blockers on ST segment, QRS duration, and corrected QT interval in patients with Brugada syndrome," *Journal of cardiovascular electrophysiology*, vol. 11, no. 12, pp. 1320–1329, 2000.

[17] Bayasi, Nourhan and Tekeste, Temesghen and Saleh, Hani and Mohammad, Baker and Ismail, Mohammed, "A 65-nm low power ecg feature extraction system," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2015, pp. 746–749.

[18] F. Rincón, J. Recas, N. Khaled, and D. Atienza, "Development and evaluation of multilead wavelet-based ECG delineation algorithms for embedded wireless sensor nodes," *IEEE Transactions on Information Technology in Biomedicine*, vol. 15, no. 6, pp. 854–863, 2011.