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Research paper

Impact of Al_2O_3 deposition temperature on the performance and initial stability of nanocrystalline ZnO thin-film transistors

R.A. Rodriguez-Davila, R.A. Chapman, P. Bolshakov, C.D. Young*, M. Quevedo-Lopez

The University of Texas at Dallas, 800 W Campbell Rd, Richardson, TX 75080, USA

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ABSTRACT

The initial performance and "time-zero" instability of ZnO TFTs are evaluated using different Al_2O_3 deposition temperature. Fully-patterned bottom-gate and top-contact devices were fabricated and used as the test structures. The initial TFT performance shows a decrease of saturation mobility from 9.2 to 5.6 $cm^2/V{\cdot}s$; increase in threshold voltage from 2.2 to 2.5 V; and subthreshold swing increase from 115 to 225 mV/DEC, with increasing deposition temperature. The time-zero instability ($t = 0$ s) shows an increase in threshold voltage shifting of 4.0, 12.8, and 13.6%; a decrease in the subthreshold swing of 5.3%, 17.7%, and 16.3%; and an increase in saturation mobility of 0.8%, 2.8%, and 4.3% with increasing deposition temperature. Results indicate that the primary mechanism of the threshold voltage shifting is the increase in roughness induced interface states due to possible dangling bonds increasing along with the roughness.

1. Introduction

Large-area and flexible electronics may need to rely on oxide-based semiconductors due to their compatibility with a low-temperature fabrication process. Oxide semiconductors, such as Zinc oxide (ZnO) based thin-film transistors (TFTs), have received increasing attention due to their compatibility with low-cost processing and exceptional electrical performance [1–3], and their potential uses in flexible circuits [3]. Furthermore, another essential aspect is that deposition of the dielectric layer is at these low temperatures, which might result in higher leakage current and higher oxide trap density, which is detrimental to the overall TFT performance and stability. Therefore, the subsequent impact on TFT performance and reliability must be evaluated for practical and commercial applications, since TFTs with high performance and suitable threshold voltage stability are essential.

Several studies that address different dielectric materials, deposition temperature, annealing temperatures, and conditions to improve the performance of oxide-base thin film transistors have been reported [4–10]. In addition, much activity has been dedicated to incorporate high-k dielectrics in TFTs using various deposition methods [11], including: chemical vapor deposition (CVD), physical vapor deposition (PVD), molecular beam epitaxy (MBE), pulsed laser deposition (PLD), wet chemical methods, radio frequency (RF) magnetron sputtering and atomic layer deposition (ALD) as the preferred method for growing high quality, dense, pinhole-free, high-performance gate dielectric films [12]. Since the previous results yield to relatively high initial TFT performance, the threshold voltage instability remains a challenge. The degradation behaviors of ZnO-based TFTs was investigated by several groups previously [13–18]. They indicated that the ΔV_{TH} under bias stress or light illumination could be attributed to charge trapping in the gate dielectric or the active layer/dielectric interface [13,14,18]. In a-Si:H TFTs, the charge trapping sites can be eliminated through a post-fabrication or post-deposition anneal. However, high-temperature annealing is not suitable for large-area/flexible substrates owing to their low softening/melting temperatures [19]. As a way to enhance stability, studies of gate dielectric engineering using bilayers [9,20,21] or nanolaminates [22] structures exist. However, these methods are complicated to replicate because conditions and parameters (like thicknesses) need to be appropriately adjusted and tuned, which becomes problematic for implementation. The ideal alternative is to enhance the dielectric quality during its deposition using permissible temperatures and conditions for large-area/flexible substrates. Is expected that a higher deposition temperature results in better film quality but reduces its applicability in large-area and flexible substrates. Therefore, the effect of the deposition temperature of aluminum oxide grown by ALD in ZnO TFTs as dielectric material is in this chapter. The initial performance and the time-zero instability of the TFTs serve as a reference for the impact. The selection of Al_2O_3 is due to its previously reported performance on ZnO TFTs [23–26], good barrier properties against oxygen and hydrogen [12] and low leakage current due to its

* Corresponding author.
E-mail address: chadwin.young@utdallas.edu (C.D. Young).

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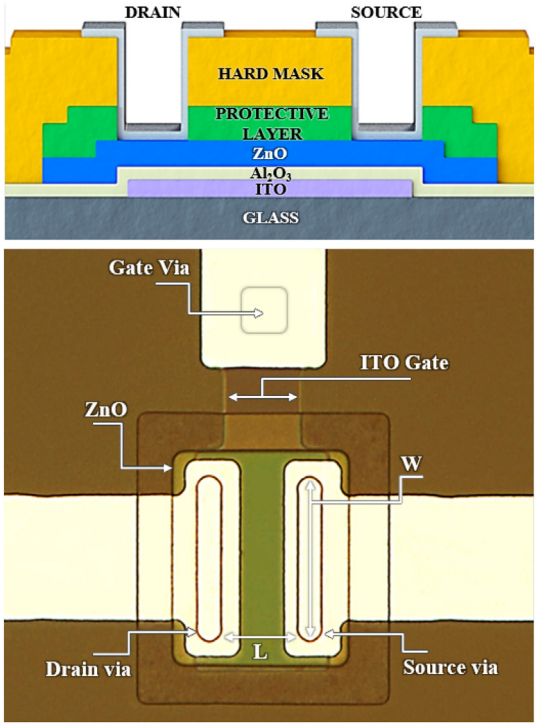

Fig. 1. (a) Cross section and (b) Plan view image of the fabricated TFT with W/L = 40/20 μm.

wide band gap.

2. Materials and methods

TFTs with a staggered bottom-gate/top-contact structure is fabricated using a seven-mask level conventional photolithography process, including the passivation level as well as an additional level for transparent materials alignment. Fig. 1a shows a cross-sectional view of the fabricated TFTs. The TFT-substrate consists of glass with 135 nm of indium tin oxide (ITO) from Luminescence Technology Corp. ITO is patterned using a conventional wet etching lithography process to form the gate electrode. Transparent materials are challenging to align with the photolithography process; for that reason, a reflective layer is formed on top of the alignment marks using 30 nm of chromium. An Ultratech/Cambridge NanoTech Savannah atomic layer deposition (ALD) tool is used to deposit 15 nm of Al_2O_3 at three different deposition temperatures (three fabricated samples), serving as the gate dielectric. Water vapor is the oxygen source, and trimethylaluminum (TMA) (Sigma-Aldrich, 97% purity) is the metal−organic precursor. The ALD chamber pressure was 0.5 Torr during the process with a constant N_2 flow of 20 sccm throughout to carry and purge the precursor vapors. The pulse times are 15 ms for both precursors. The precursor's purge times are adjusted depending on the deposition temperature: 20 s for 100 and 175 °C and 10 s for 250 °C. Al_2O_3 deposition rate changes with deposition temperature (DT). Therefore, the cycles required for 15 nm Al_2O_3 were adjusted before the fabrication and monitored after the deposition. Next, a 45 nm thick ZnO is deposited by pulsed laser deposition (PLD) at 100 °C and an oxygen (O_2) pressure of 20 mTorr. A ZnO target with a purity of 99.99% serves as the material source. The energy density used to ablate the target was 1 J/cm^2. No post-deposition anneal performed on the samples in order to not convolute the different deposition temperatures. A layer of 250 nm of polyp-xylylene-C (Parylene-C) was deposited by chemical vapor deposition at room temperature to protect and passivate the top surface of the oxide semiconductor from the subsequent photolithography steps (PL in Fig. 1a). After patterning the first Parylene layer and semiconductor, another layer of 250 nm of Parylene-C was deposited to encapsulate and protect the active area (HM in Fig. 1a). This second Parylene layer was patterned to extend 20 μm from the edges of the semiconductor. S-D vias were defined using oxygen-based reactive ion etching. Finally, 200 nm of Al was deposited and patterned to define S-D contacts. Fig. 1b shows a plan view, optical image. The designed channel lengths (L) were 10, 20, 40, 60, 80 μm, and the channel widths (W) were 40, 80, 160 μm. *The gate dielectric deposition temperature (DT) is the only variable in the fabrication process.*

The electrical characterization of the TFTs was at room temperature (RT) in the dark using a Cascade probe station and a Keithley 4200-SCS semiconductor parameter analyzer. The following sequence of measurements defines the time-zero instability of the TFTs: (1) transfer curve in saturation (first cycle); (2) I_{DS}-V_{DS} output curve (second cycle); (3) transfer curve in saturation regimen (third cycle); and (4) transfer curve in saturation regimen (fourth cycle). Thickness measurements were performed using a Sentech 800 spectroscopic ellipsometer with a wavelength range of 350 to 850 nm. The Ψ and Δ data obtained at an incident angle of 70° were fitted to obtain the refractive index dispersion. Al_2O_3 surface morphology is investigated using a 3100 Dimension V Atomic Probe microscope (SPM). The acquired images are in tapping mode, and the scan area is 1 μm × 1 μm with a resolution of 512 pixel/line. The scan rate is set to 0.5 Hz using a deflection potential of 350 mV.

3. Results and discussion

The measured thicknesses for ZnO, 1st Parylene protective layer and second layer Parylene hard mask, as evaluated by ellipsometry, were: 45 ± 0.8 nm, 289 ± 0.4 nm and 294 ± 0.4 nm, respectively. The thicknesses, as measured by profilometry, for ITO and aluminum were: 135 ± 1.5 nm and 154 ± 0.6 nm, respectively. According to JCPDS # 36–1451, ZnO film shows (0002) preferential orientation of a wurtzite structure (Fig. S2). The mean crystallite size of ZnO film is 45 ± 1.2 nm, calculated employing Scherrer [27] equation and corroborated using transmission electron microscopy. The measured optical Al_2O_3 thicknesses for the different deposition temperatures are 15.8 ± 0.1 nm, 16.2 ± 0.1 nm, 16.0 ± 0.2, for 100, 175, and 250 °C, respectively. Thickness deposition is uniform across the sample with minimal variation as a function of the deposition temperature. The deposited Al_2O_3 films are amorphous, regardless of the deposition temperature, as shown in Fig. S2.

3.1. Initial TFT performance

Fig. 2a illustrates the initial transfer characteristic comparison (I_{DS}-V_{GS}) for Al_2O_3 deposited at 100, 175, and 250 °C. The off-current (I_{OFF}) is found to be in the range of 10^{-13} A for the three samples. The on-current (I_{ON}), at V_{GS} = 5 V, decreases with Al_2O_3 DT, indicating degradation of the accumulated active channel region. The on and off sheet resistance ($R_{SH\text{-}ON}$ and $R_{SH\text{-}OFF}$, respectively) is investigated using the method of Terada and Muta [29]. The obtained results are in Table S1. As mentioned, $R_{SH\text{-}OFF}$ is independent on the deposition temperature, because it is dependent on the ZnO bulk resistivity (Fix parameter for all samples). However, the dependence of $R_{SH\text{-}ON}$ with DT suggests degradation of the accumulation layer, which depends on the interface Al_2O_3/ZnO.

Following the simplest analytic model for field effect transistors [28], the drain current in saturation can be expressed using Eq. (1); where C_{ox} is the gate dielectric capacitance per unit area, and μ_{SAT} is the saturation mobility. By extrapolating $I_{DS}^{0.5}$ as a function of V_{GS} under the condition of $V_{DS} > V_{GS} - V_{TH\text{-}SAT}$, the $V_{TH\text{-}SAT}$ is obtained from the fitted-line intercept with the x-axis and the saturation mobility (μ_{SAT}) from the slope. From the maximum slope obtained from the derivative of the transfer curve in the logarithmic scale, the Subthreshold swing (SS) is extracted (Eq. 2).

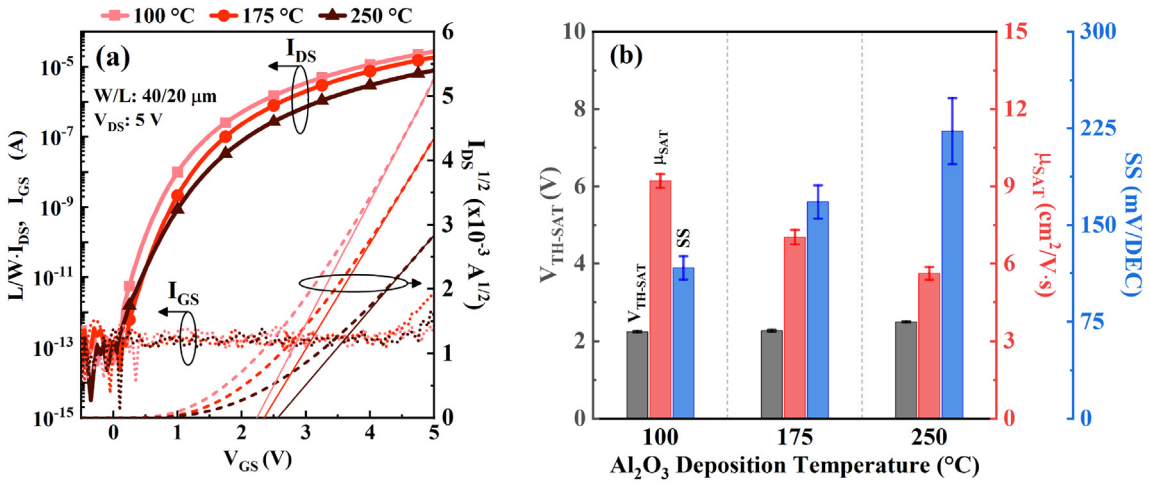

Fig. 2. (a) Representative normalized transfer characteristics for TFTs fabricated with 100, 175, and 250 °C Al_2O_3. (b) Evolution of the initial saturation mobility, saturation threshold voltage, and subthreshold swing as a function of the Al_2O_3 deposition temperature.

$$I_{DS} = \frac{\mu_{SAT} C_{OX} W}{2L}(V_{GS} - V_{TH-SAT})^2 \quad (1)$$

$$SS = \frac{dV_{GS}}{d(\log I_{DS})}\Big|_{MAX} \quad (2)$$

The oxide capacitance, C_{ox}, is obtained from MIM capacitors that are onto the same fabricated sample. Fig. S2a Shows the C-V characteristic for the different Al_2O_3 DT. The average Cox are 5.04×10^{-7}, 4.92×10^{-7}, and 4.98×10^{-7} F/cm^2. These results are in close agreement to the obtained capacitance density considering ideal parallel plate capacitors, the measured thickness, and a dielectric constant of 9. The capacitance density shows a small dispersion as a function of the frequency, that can be due to RC effects as a result of the contact resistance, or lower conductivity of ITO (compared to Al) used as the bottom contact.

Fig. 2b illustrates the evolution of the saturation mobility, threshold voltage, and subthreshold swing with the Al_2O_3 DT. Table S1 shows a detailed comparison of the TFT parameters extracted for the different Al_2O_3 DTs. The minimum subthreshold swing (SS) of 117 mV/DEC is for TFTs with Al_2O_3 deposited at 100 °C. The increase in DT increases SS 30% for 175 °C and 48% for 250 °C. The evolution of the SS with Al_2O_3 DT could be due to a rise in interface states [29]. Electron saturation mobility (μ_{SAT}) decreases linearly from 9.2 to 5.6 cm^2/V·s with increasing DT. V_{TH-SAT} at 100 °C is 2.24 V and increases 1.1% for 175 °C, and 10.2% for 250 °C. Since I_{ON} and μ_{SAT} are decreasing with increasing DT, V_{TH-SAT} is expected to increase. The study of the initial TFT behavior indicates that the increase of Al_2O_3 deposition temperature decreases device performance, and the increase in interface traps could be the origin.

3.2. TFT time zero instability

Fig. 3(a) to (c) illustrates the evolution of the I_{DS}-V_{GS} before (first cycle) and after (third cycle) acquiring the I_{DS}-V_{DS} characteristic for Al_2O_3 deposited at 100, 175 and 250 °C. The time zero electron trapping is evident with the V_{TH-SAT} shift, ΔV_{TH-SAT}. However, the transfer curve remains stable after the third cycle (fourth cycle = "After 2") for all DTs. This behavior indicates that the source of the instability happens during the second cycle (I_{DS}-V_{DS} data collection). This instability source is because of the I_{DS}-V_{DS} measurement act as positive bias stress during a short period.

The changes in the considered TFTs main parameters induced by the time-zero-instability electrical characterization are in Fig. 3d. The detailed value comparison of the changes in the TFT performance due to time-zero-instability as a function of Al_2O_3 deposition temperature is in Table S2. The difference between the threshold voltages extracted "Before" ($t = 0$ s or first cycle) and "After" third cycle for each dielectric condition is the time zero threshold voltage shifting, ΔV_{TH-SAT}. Changes in subthreshold swing and saturation mobility are extracted using the same procedure. ΔV_{TH-SAT} is positive for all situations. The smaller ΔV_{TH-SAT} of 88 mV was for Al_2O_3 deposited at 100 °C. The increase of DT increases ΔV_{TH-SAT} to 290 mV and 340 mV for 175 and 250 °C, respectively. SS improves for all the samples ($\Delta SS < 0$ mV/DEC), indicating a reduction of interface states. The increase of μ_{SAT} with DT might be related to a decrease of electron scattering due to the initially unoccupied states that are now occupied by electrons. Typically, ΔV_{TH-SAT} could be due to oxide states or interface states. The total oxide charge, Q_{OT}, can be determined using:

$$Q_{OT} = -C_{OX}\Delta V_{FB} \quad (3)$$

where ΔV_{FB} represents the flat-band voltage shift due to charge injection. Since a TFTs works in the accumulation mode, V_{FB} determines the voltage at which the channel starts accumulating; therefore, V_{ON} is the gate voltage corresponding to the flat band in the channel layer, which corresponds to the onset where I_{DS} values start increasing exponentially. Then, ΔV_{ON} could replace ΔV_{FB} in Eq. (4), and the change in dielectric trap density (ΔN_{OT}) due to the initial stress produced by the first and second cycle can be calculated using:

$$\Delta N_{OT} = -\frac{1}{q} C_{OX}\Delta V_{ON} \quad (4)$$

The change in the interface trap density, ΔD_{IT}, can be related to the shift of SS after the stress using:

$$\Delta D_{IT} = \frac{C_{OX}}{\ln(10) qkT}\Delta SS \quad (5)$$

The evolution of ΔD_{IT} and ΔN_{OT} as a function of Al_2O_3 DT is in Fig. 3d. ΔD_{IT} and ΔN_{OT} from metal-insulator-semiconductor (MIS) devices are calculated to corroborate the results. Fig. S2b shows the capacitance density for MIS capacitors at 1 kHz (low frequency) and 1 MHz (high frequency) for different Al_2O_3 DTs. Flat band voltage is obtained from the $d^2(1/C)^2/dV_{GS}^2$. V_{FB} corresponds to V_{GS} at which the maximum occurs, for n-type semiconductors. Eq. (4) allows the calculation of ΔN_{OT}. ΔD_{IT} is obtained by using the method proposed by Castagné and Vapaille [30] and illustrated in Eq. (6). D_{IT} and N_{OT} results extracted from the MIS are in Table S2. The evaluated trap states results agree with the results obtained from the time zero instability.

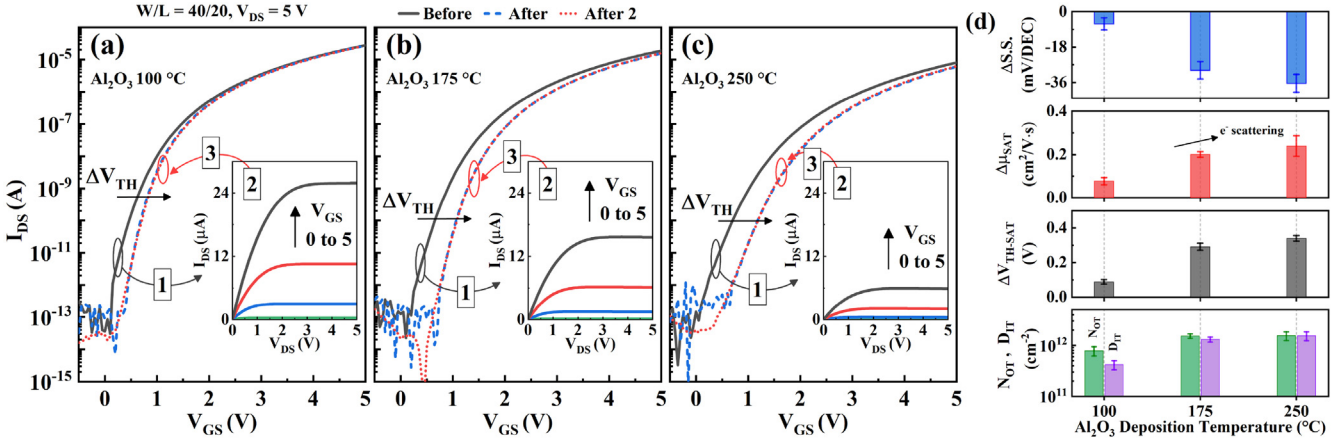

Fig. 3. TFT performance for the different Al_2O_3 DTs: (a) 100; (b) 175; and (c) 250 °C. Numbers indicate the measurement order. Electron trapping is evident by the positive ΔV_{TH} occasioned by the extraction of the I_{DS}-V_{DS} characteristic (Time Zero Instability). (d) The average change in main parameters and trap states with Al_2O_3 deposition temperature.

$$D_{IT} = \frac{C_{OX}}{q}\left(\frac{C_{lf}/C_{OX}}{1 - C_{lf}/C_{OX}} - \frac{C_{hf}/C_{OX}}{1 - C_{hf}/C_{OX}}\right) \quad (6)$$

The change in N_{OT} is more significant than the shift of D_{IT} for Al_2O_3 deposited at 100 °C. Nevertheless, ΔN_{OT} and ΔD_{IT} are comparable for 175 and 250 °C Al_2O_3. These results indicate that the device instability for 100 °C Al_2O_3 is mainly due to oxide states, but for higher temperatures, it is due to a combination of both interface states and oxide trap states. Nevertheless, ΔN_{OT} is the combination of fix charge states, oxide trap states, and interface states; therefore, the similar values of ΔN_{OT} and ΔD_{IT} for 175 and 250 °C indicates that the instability mechanism is potentially due to the change in interface states. Since these trap states are near or at the ZnO/Al_2O_3 interface, further investigation near this region is required to identify the instability origin potentially.

3.3. Interfacial characterization of the gate dielectric stack

Al_2O_3 surface morphology is studied on different film stacks to address: (1) Al_2O_3 roughness evolution with DT; (2) TFT substrate evolution with DT; and (3) Gate stack evolution with DT. For (1) high quality thermally growth SiO_2 is used. For (2) and (3) the same fabricated TFT samples are used. The surface topography for the different substrates/conditions (Rows) and Al_2O_3 deposition temperature (columns) is in Fig. 4a, The average roughness, R_a, is calculated from the arithmetic average of the absolute values of the profile height (peaks and valleys) deviations per pixel from the mean line, recorded within the scan length [31]. Eq. (7) is used to calculate R_a, where L is the scan length and Z the profile height as a function of the pixels. Fig. 4b shows the average roughness evolution after surface flatting and noise reduction.

$$R_a = \frac{1}{L}\int_0^L |Z(x)|\, dx \quad (7)$$

Comparison of subthreshold swing and change in subthreshold swing with the gate dielectric stack surface roughness. The linear dependence of SS with Ra suggest that roughness induced interfacial defects as the dominant mechanism of the TFT instability.

The evolution of the Al_2O_3/SiO_2 surface roughness with DT is negligible and averaged value of ~0.3 nm. The surface roughness of Al_2O_3/TFT-substrate are 1.0, 1.3, and 2.1 nm for 100, 175, and 250 °C, respectively; indicating a strong dependency with DT. Furthermore, the surface roughness of Al_2O_3/ITO/TFT-substrate (gate dielectric stack) increased 1 nm regardless of DT; consequently, Al_2O_3 is deposited conformally on the ITO/TFT-substrate stack. These results show that the increase in gate stack surface roughness is due to morphological and structural changes of the TFT-substrate with the increase in the

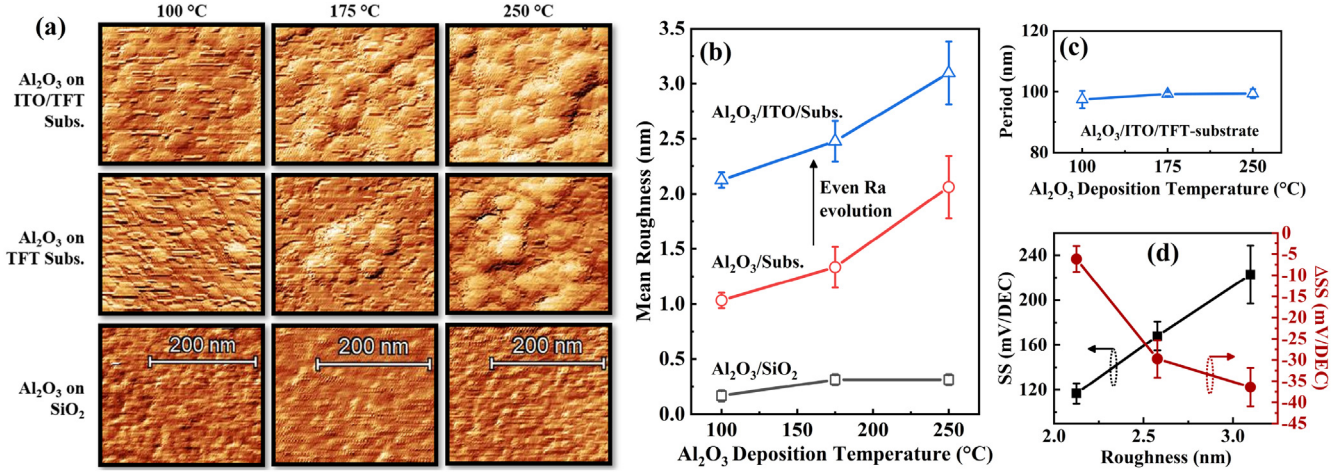

Fig. 4. Gate dielectric analysis on different substrates. (a) Surface topography images of Al_2O_3 deposition at different temperatures (columns) and different substrates (Rows). (b) Average roughness change as a function of the Al_2O_3 deposition temperature. Changes on glass substrate are responsible for the increase in gate dielectric stack (Al_2O_3/ITO/Glass) roughness. (c) Averaged roughness period as a function of Al_2O_3 DT. (d) Comparison of subthreshold swing and change in subthreshold swing with the gate-dielectric-stack surface roughness.

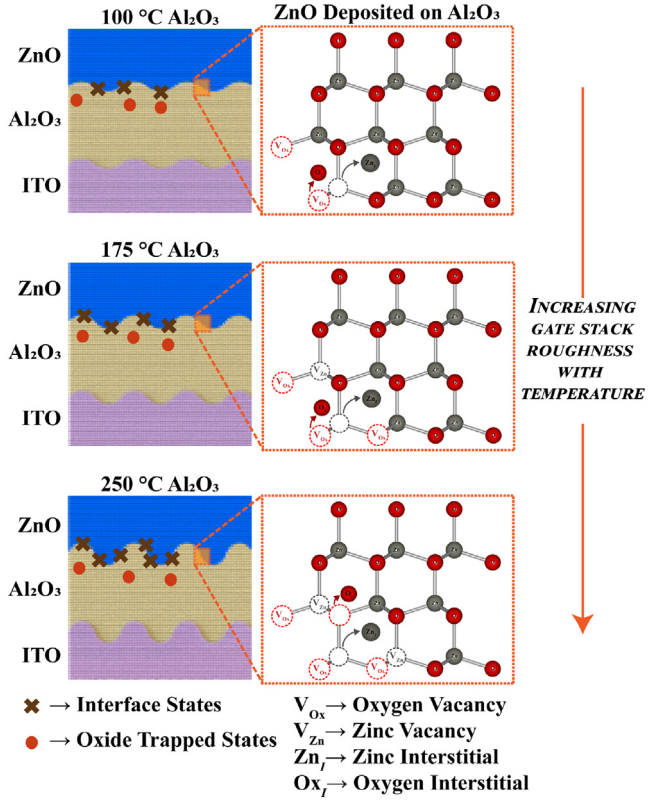

Fig. 5. The proposed instability mechanism induced by the change of Al_2O_3 DT on the TFTs. The deposition of ZnO in the rougher surface leads to dangling bonds, causing an increase in interface states.

deposition temperature.

The periodicity of the gate dielectric stack roughness, T_a, is in Fig. 4c. As shown, T_a is not changing with temperature; instead, only roughness is increasing with DT. Asenov and Kaya [32] reported that the largest charge concentration is in the middle of the well, causing a more significant increase in ΔV_{TH} with deeper wells (bigger roughness). Moreover, the change in roughness might induce surface trap states due to atomic lattice mismatch and fluctuations of the chemical composition of contacting materials leading to dangling interfacial bonds. The bigger the roughness, the more significant the induced interfacial states (dangling bonds, oxygen vacancies, zinc interstitials, and zinc vacancies) at the metallurgical junction [33].

Lee et al. reported the mobility dependence on surface roughness and surface energy for organic-based TFTs. They suggested that if R_a is more significant than the characteristic scattering length of majority carriers, the roughness has a significant impact on mobility for the same roughness periodicity. Usually, scattering length for ZnO deposited at low temperatures is $< < 1$ nm. Therefore, the increase of R_a from 1.8 to 3.2 nm with increasing Al_2O_3 DT reduces electron mobility, as shown in Fig. 2c. However, the improvement of mobility with temperature (Fig. 3d) indicates a reduction in scattering after the first and second cycle. Therefore, mobility instability observed for the initial TFT performance can be strongly dependent on gate stack roughness, but Coulombic scattering can be the dominant mechanism for the time zero instability.

Hence, the fact that the potential distribution is not equal within the well (maximum potential at the middle of the well) combined with roughness induced interface states can explain the instability observed with the increase in Al_2O_3 DT. The trapping of electrons in interface states reveals the increase in threshold voltage, as well. Furthermore, the reduction of interface states slightly improves mobility due to the reduction of the Coulombic scattering. Fig. 5 shows the proposed instability mechanism. The dependency of SS and ΔSS with average roughness is in Fig. 4d. The linear dependence of SS with R_a shows a direct correlation of initial SS (D_{IT}) with gate stack roughness. Furthermore, ΔSS shows an increasing reduction of interface traps with increasing roughness; since more interface states can be electrically active with the increase in roughness, the occupancy probability of those states increases.

4. Conclusions

The performance and the time zero or initial instability of nanocrystalline ZnO TFTs was presented using different Al_2O_3 deposition temperatures. Electrical results show that oxide states are the instability source of TFTs fabricated with 100 °C Al_2O_3. However, for TFTs fabricated with Al_2O_3 deposited at 175 and 250 °C instability is attributed to interface states. Morphological studies show that gate dielectric stack roughness is increasing with increasing deposition temperature due to structural or morphological changes occurring in the TFT-substrate. The increase in roughness can induce surface trap states due to atomic lattice mismatch and fluctuations of the chemical composition of contacting materials, leading to dangling bonds. The more significant interface states with increasing deposition temperature can increase the capture of electrons; consequently, negative charge trapping can explain the positive $\Delta V_{TH\text{-}SAT}$. The combination of roughness and roughness induced defects acting as electron trap states at the Al_2O_3/interface are responsible for the initial TFT performance and time-zero instability.

Declaration of Competing Interests

The authors declare that the validity of research, *is not* influenced by a secondary/financial interest.

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mee.2019.111114.

References

[1] G. Gutierrez-Heredia, I. Mejia, M.E. Rivas-Aguilar, N. Hernandez-Como, V.H. Martinez-Landeros, F.S. Aguirre-Tostado, M.A. Quevedo-Lopez, Fully patterned and low temperature transparent ZnO-based inverters, Thin Solid Films 545 (2013) 458–461.
[2] Y. Kawamura, M. Horita, Y. Ishikawa, Y. Uraoka, Effects of gate insulator on thin-film transistors with ZnO channel layer deposited by plasma-assisted atomic layer deposition, J. Disp. Technol. 9 (9) (2013) 694–698.
[3] M.S. Oh, W. Choi, K. Lee, D.K. Hwang, S. Im, Flexible high gain complementary inverter using n-ZnO and p-pentacene channels on polyethersulfone substrate, Appl. Phys. Lett. 93 (3) (2008) 033510.
[4] F.R. Libsch, J. Kanicki, Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors, Appl. Phys. Lett. 62 (11) (1993) 1286–1288.
[5] S. Masuda, K. Kitamura, Y. Okumura, S. Miyatake, H. Tabata, T. Kawai, C. N, Transparent thin film transistors using ZnO as an active channel layer and their electrical properties, J. Appl. Phys. 93 (3) (2003) 1624–1630.
[6] E. Fortunato, A. Pimentel, L. Pereira, A. Gonçalves, G. Lavareda, H. Águas, I. Ferreira, C.N. Carvalho, R. Martins, High field-effect mobility zinc oxide thin film transistors produced at room temperature, J. Non-Cryst. Solids 338-340 (2004) 806–809.
[7] S. Vallisree, R. Thangavel, T.R. Lenka, Comparative characteristics study of the effect of various gate dielectrics on ZnO TFT, International Conference on Energy,

Communication, Data Analytics and Soft Computing (ICECDS) 2017 (2017) 3909–3916.
[8] C.D. Young, R. Campbell, S. Daasa, S. Benton, R.R. Davila, I. Mejia, M. Quevedo-Lopez, Effect of dielectric thickness and annealing on threshold voltage instability of low temperature deposited high-k oxides on ZnO TFTs, IEEE International Integrated Reliability Workshop (IIRW) 2015 (2015) 34–36.
[9] F.H. Alshammari, P.K. Nayak, Z. Wang, H.N. Alshareef, Enhanced ZnO thin-film transistor performance using bilayer gate dielectrics, ACS Appl. Mater. Interfaces 8 (35) (2016) 22751–22755.
[10] S. Vyas, A.D.D. Dwivedi, R.D. Dwivedi, Effect of gate dielectric on the performance of ZnO based thin film transistor, Superlattice. Microst. 120 (2018) 223–234.
[11] K. Kandpal, N. Gupta, Investigations on high-κ dielectrics for low threshold voltage and low leakage zinc oxide thin-film transistor, using material selection methodologies, J. Mater. Sci. Mater. Electron. 27 (6) (2016) 5972–5981.
[12] Y. Nam, H.-O. Kim, S. Cho, S.-H. Park, Effect of hydrogen diffusion in an In–Ga–Zn–O thin film transistor with an aluminum oxide gate insulator on its electrical properties, RSC Adv. 8 (10) (2018) 5622–5628.
[13] I. Abdel-Motaleb, N. Shetty, K. Leedy, R. Cortez, Investigation of the drain current shift in ZnO thin film transistors, J. Appl. Phys. 109 (1) (2011) 014503.
[14] C.H. Ahn, B.H. Kong, H. Kim, H.K. Cho, Improved electrical stability in the Al doped ZnO thin-film-transistors grown by atomic layer deposition, J. Electrochem. Soc. 158 (2) (2011) H170–H173.
[15] E. Chong, K.C. Jo, S.Y. Lee, High stability of amorphous hafnium-indium-zinc-oxide thin film transistor, Appl. Phys. Lett. 96 (15) (2010) 152102.
[16] R. Navamathavan, E.-J. Yang, J.-H. Lim, D.-K. Hwang, J.-Y. Oh, J.-H. Yang, J.-H. Jang, S.-J. Park, Effects of electrical Bias stress on the performance of ZnO -based TFTs fabricated by RF magnetron sputtering, J. Electrochem. Soc. 153 (5) (2006) G385–G388.
[17] J.-S. Park, J.K. Jeong, H.-J. Chung, Y.-G. Mo, H.D. Kim, Electronic transport properties of amorphous indium-gallium-zinc oxide semiconductor upon exposure to water, Appl. Phys. Lett. 92 (7) (2008) 072104.
[18] J.J. Siddiqui, J.D. Phillips, K. Leedy, B. Bayraktaroglu, Illumination instabilities in ZnO/HfO2 thin-film transistors and influence of grain boundary charge, J. Mater. Res. 27 (17) (2012) 2199–2204.
[19] O. Lupan, T. Pauporté, L. Chow, B. Viana, F. Pellé, L.K. Ono, B. Roldan Cuenya, H. Heinrich, Effects of annealing on properties of ZnO thin films prepared by electrochemical deposition in chloride medium, Appl. Surf. Sci. 256 (6) (2010) 1895–1907.
[20] J.-W. Jo, K.-H. Kim, J. Kim, S.G. Ban, Y.-H. Kim, S.K. Park, High-mobility and hysteresis-free flexible oxide thin-film transistors and circuits by using bilayer sol–gel gate dielectrics, ACS Appl. Mater. Interfaces 10 (3) (2018) 2679–2687.
[21] C. Lin, C. Chien, C. Wu, H. Hsieh, C. Wu, Y. Yeh, C. Cheng, C. Lai, M. Yu, Top-gate staggered a-IGZO TFTs adopting the bilayer gate insulator for driving AMOLED, IEEE Transactions on Electron Devices 59 (6) (2012) 1701–1708.
[22] T. Waggoner, J. Triska, K. Hoshino, J.F. Wager, J.F.C. Jr, Zirconium oxide-aluminum oxide nanolaminate gate dielectrics for amorphous oxide semiconductor thin-film transistors, J. Vac. Sci. Technol. B 29 (4) (2011) 04D115.
[23] T.S. Kang, T.Y. Kim, G.M. Lee, H.C. Sohn, J.P. Hong, Highly stable solution-processed ZnO thin film transistors prepared via a simple Al evaporation process, J. Mater. Chem. C 2 (8) (2014) 1390–1395.
[24] T.S. Kang, J.H. Koo, T.Y. Kim, J.P. Hong, Electrical and structural analyses of solution-processed li-doped ZnO thin film transistors exposed to ambient conditions, Appl. Phys. Express 6 (1) (2013) 011101.
[25] K. Kim, S.Y. Park, K.-H. Lim, C. Shin, J.-M. Myoung, Y.S. Kim, Low temperature and solution-processed Na-doped zinc oxide transparent thin film transistors with reliable electrical performance using methanol developing and surface engineering, J. Mater. Chem. 22 (43) (2012) 23120–23128.
[26] T. Jun, K. Song, Y. Jeong, K. Woo, D. Kim, C. Bae, J. Moon, High-performance low-temperature solution-processable ZnO thin film transistors by microwave-assisted annealing, J. Mater. Chem. 21 (4) (2011) 1102–1108.
[27] A.L. Patterson, The Scherrer formula for X-ray particle size determination, Phys. Rev. 56 (10) (1939) 978–982.
[28] S.M. Sze, K.K. Ng, Physics of Semiconductor Devices, John Wiley & Sons, Inc, 2006.
[29] H.-N. Lee, J. Kyung, S.K. Kang, D.Y. Kim, M.-C. Sung, S.-J. Kim, C.N. Kim, H.G. Kim, S.-t. Kim, 68.2: 3.5 inch QCIF + AM-OLED panel based on oxide TFT backplane, SID Symposium Digest of Technical Papers 38 (1) (2007) 1826–1829.
[30] R. Castagné, A. Vapaille, Description of the SiO2 Si interface properties by means of very low-frequency MOS capacitance measurements, Surf. Sci. 28 (1) (1971) 157–193.
[31] A.S.o.M. Engineers, A.S.o.M.E.S.C.B. Classification, D.o.S. Qualities, A.N.S. Institutn, Surface Texture: Surface Roughness, Waviness and Lay, American Society of Mechanical Engineers, 2010.
[32] A. Asenov, S. Kaya, Effect of oxide interface roughness on the threshold voltage fluctuations in decanano MOSFETs with ultrathin gate oxides, 2000 International Conference on Simulation Semiconductor Processes and Devices (Cat. No.00TH8502), 2000, pp. 135–138.
[33] F.-H. Chen, M.-N. Hung, J.-F. Yang, S.-Y. Kuo, J.-L. Her, Y.H. Matsuda, T.-M. Pan, Effect of surface roughness on electrical characteristics in amorphous InGaZnO thin-film transistors with high-κ Sm2O3 dielectrics, J. Phys. Chem. Solids 74 (4) (2013) 570–574.