Performance and Reliability Comparison of ZnO and IGZO Thin-Film Transistors and Inverters Fabricated at a Maximum Process Temperature of 115 °C

R. A. Rodriguez-Davila, *Student Member, IEEE*, I. Mejia, *Senior Member, IEEE*, R. A. Chapman, *Fellow, IEEE*, C. D. Young, *Senior Member, IEEE*, and M. Quevedo-Lopez

***Abstract*— Performance and reliability comparison of oxide-based thin-film transistors fabricated at a maximum process temperature of 115 °C is presented. A fully patterned and passivated process was successfully evaluated and implemented using polycrystalline ZnO and amorphous indium–gallium–zinc–oxide (IGZO) as an active layer in glass substrates. Saturation mobilities of 14.2 and 9.0 $cm^2 \cdot V^{-1} \cdot s^{-1}$ were obtained for ZnO and IGZO, respectively, with threshold voltages of 2.2 and 2.0 V, an ON/OFF ratio $> 1 \times 10^8$, and an $I_{off} < 1 \times 10^{-12}$ A. The small mobility change in IGZO with gate voltage is due to its amorphous character. Longer variation is observed in polycrystalline ZnO due to its grain boundaries. Reliability studies show a threshold voltage shifting of 0.4 and 1.8 V for ZnO and IGZO devices, testing after 1200-s stress. Devices were successfully implemented in ZnO- and IGZO-based inverters using saturation and zero-drive structures, showing a maximum dc gain of 2.4- and 25-V/V, respectively.**

***Index Terms*— Inverters, passivation, photolithography, reliability, thin-film transistors (TFTs).**

I. Introduction

METAL–OXIDE–SEMICONDUCTORS have received a lot of attention due to their relatively high carrier mobility and low process temperature compared with hydrogen-doped amorphous silicon, a-Si:H, that is the material most often used in display circuit technology [1]. Recently, indium–gallium–zinc–oxide (IGZO) has being used in liquid crystal display (LCD) with ultrahigh pixel density [2].

Most of the oxide-based thin-film transistors (TFTs) reported in the literature use an inverted staggered structure with a common gate and/or a common semiconductor using shadow mask or liftoff processes to pattern source and drain (S–D) contacts [3]–[7]. Although these methods are simple and allow a faster evaluation of the materials, there are some drawbacks including the following.

1) Semiconductor is continuously exposed during the fabrication process, where changes in the atmosphere, chemicals, and plasma cleanings can influence the free carrier concentration negatively impacting device performance and stability of the TFTs [8], [9].
2) Features patterned using shadow masks are usually large (> 40 μm), making the fabrication of smaller feature size difficult.
3) The gap between the shadow mask and the substrate is difficult to control producing shadowing effects resulting in nonuniform shapes and material thicknesses, reducing yield.
4) Usually, these structures show gate currents comparable with the measured drain current, which reduces the confidence of the extracted TFT parameters [10], [11].

Implementation of these devices in complex circuits requires patterning the semiconductor layer to better isolate transistors while allowing to be individually addressed by the TFT gates. Fully patterned fabrication processes for TFTs using ZnO and IGZO have been extensively reported [12]–[19]. These reports show the ability to deposit the materials over large areas, mobilities larger than 1 $cm^2 \cdot V^{-1} \cdot s^{-1}$, and small geometrical dependence. However, plasma-assisted processes and temperatures above 200 °C are normally required during the fabrication process, which increase the production time and cost, that can make the process incompatible with different substrates and applications. Moreover, high-temperature processing and some atmospheres can damage the metal–oxide–semiconductor [20], [21]. For these reasons, it is imperative to maintain a low-temperature fabrication process that allows fully patterning the devices, while protecting the semi-

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R. A. Rodriguez-Davila, R. A. Chapman, C. D. Young, and M. Quevedo-Lopez are with the Materials Science and Engineering Department, The University of Texas at Dallas, Richardson, TX 75080 USA (e-mail: ra.rodriguezdavila@gmail.com).

I. Mejia was with the Materials Science and Engineering Department, The University of Texas at Dallas, Richardson, TX 75080 USA. He is now with the Division of Mircotechnologies, Center for Engineering and Industrial Development, Querétaro 76125, Mexico.

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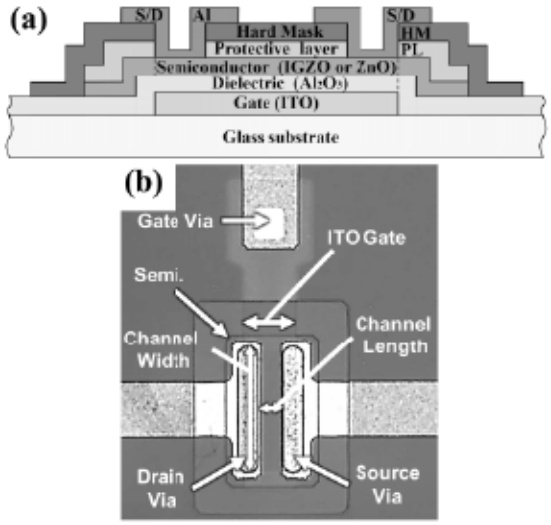

Fig. 1. (a) Cross section of a TFT. (b) Top view of a TFT with $W = 40\ \mu$m and L = 20 μm. The S/D vias are 5 μm wide with S–D metal overlap of 2.5 μm for alignment tolerance.

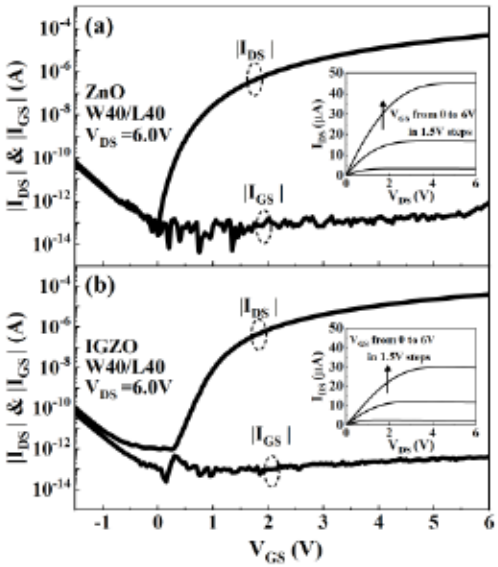

Fig. 2. Representative transfer characteristics for (a) ZnO- and (b) IGZO-based TFTs, respectively. Inset: I_D–V_D output characteristics for the respective TFT.

conductor from the chemicals and ambient normally used in the fabrication process, and its subsequent operation and storage. Furthermore, establishing a comparison with the most used metal–oxide–semiconductors, ZnO and IGZO, and understanding their performance difference and limitations while being fully patterned and fabricated under the same conditions and temperatures are the key for their selection and implementation in further electronic applications. In this article, a comparison of fully patterned and passivated amorphous IGZO and nanocrystalline ZnO TFTs is presented with a maximum process temperature of 115 °C. In addition to device performance comparison, the electrical stability under bias stress is also reported to quantify the robustness of the devices for digital electronics. To demonstrate and compare the integration capabilities of the obtained oxide-based TFTs, basic digital circuits including saturation and zero-drive inverters are fabricated on the same sample used for the TFT performance comparison.

II. TFT Fabrication

TFTs with the staggered bottom-gate/top-contact structure are fabricated using a seven-mask level conventional photolithography process, including the passivation level and an additional level for transparent material alignment. Fig. 1(a) shows a cross-sectional view of the fabricated TFTs. A glass with 135 nm of indium–tin–oxide (ITO) from Luminescence Technology Corp., New Taipei City, Taiwan, is used as the substrate and the gate electrode. Transparent materials are difficult to align when photolithography is used; for that reason, 30 nm of chromium is used as the reflective layer on the top of the alignment marks. The gate dielectric consists of 17.5-nm Al_2O_3 deposited by atomic layer deposition (ALD) at 100 °C. Then, a 45-nm-thick semiconductor is deposited by pulsed laser deposition (PLD) at 100 °C and at an oxygen (O_2) pressure of 20 mTorr. Either ZnO or IGZO (In_2O_3:Ga_2O_3:ZnO = 2:2:1 at.%) targets, with a purity of 99.99%, are used. The energy density to ablate the target is calibrated to 1 J/cm^2. A layer of 250 nm of poly-p-xylylene-C (Parylene-C) is deposited by chemical vapor deposition at room temperature (RT) to protect and passivate the top surface of the oxide semiconductor from the subsequent photolithography steps [protective layer (PL) in Fig. 1(a)]. After patterning the first Parylene layer, the second layer of 250 nm of Parylene-C is deposited as hard mask (HM) [HM in Fig. 1(a)] to protect the sides and fully encapsulate the semiconductor. Before patterning the S–D contacts, this second Parylene layer is patterned to extend 20 μm from the edges of the semiconductor. S–D vias are defined using oxygen-based reactive-ion etching. Finally, 150 nm of Al is deposited and patterned to define S–D contacts. Fig. 1(b) shows a top-view optical image. The active channel material (ZnO or IGZO) is the only variation in the fabrication process. The transfer characteristics of the devices were measured at RT in the dark using a probe station and a Keithley 4200-SCS meter.

III. Results

No sharp feature is observed in the X-ray diffraction (XRD) pattern obtained for IGZO/Al_2O_3/Glass, indicating the amorphous structure. According to JCPDS # 36-1451, ZnO/Al_2O_3/Glass film shows (0002) preferential orientation of the wurtzite structure. The mean crystallite size of the ZnO film is 45 ± 1.2 nm, calculated by means of Scherrer [22] equation and corroborated using transmission electron microscopy. The measured thicknesses for the different film used, as evaluated by ellipsometry, were 18 ± 0.1, 45 ± 0.8, 44 ± 0.5, 289 ± 0.4, and 294 ± 0.4 nm for Al_2O_3, ZnO, IGZO, first Parylene PL, and second-layer Parylene HM, respectively. The thicknesses, as measured by profilometry, for ITO and aluminum were 135 ± 1.5 and 154 ± 0.6 nm, respectively. Fig. 1(b) shows an optical image of the resulting TFTs. The designed channel lengths (L) were 10, 20, 40, 60, and 80 μm and the channel widths (W) were 40, 80, and 160 μm. No apparent damage from the processing is observed.

Fig. 2(a) and (b) shows the output characteristics and transfer curves of the fabricated ZnO and IGZO TFTs, respectively. Following the simplest analytic model for field-effect tran-

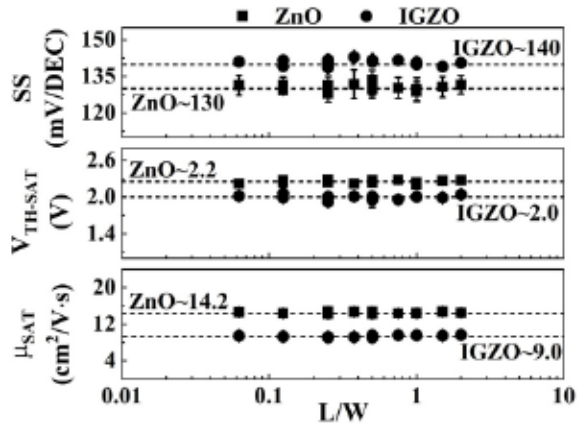

Fig. 3. Extracted saturation mobility, saturation threshold voltage, and SS as a function of the device aspect ratio. Dashed lines represent the average value. The horizontal trend suggests devices behaving normally with negligible parasitic effects.

sistors [23], the drain current in saturation can be expressed using (1), where C_{OX} is the gate dielectric capacitance per unit area and μ_{SAT} is the saturation mobility. By extrapolating $I_{DS}^{0.5}$ versus V_{GS} plot under the condition of $V_{DS} > V_{GS} - V_{TH-SAT}$, the V_{TH-SAT} is obtained from the intercept with the x-axis of the fitted line and calculated the saturation mobility (μ_{SAT}) from the slope. C_{OX} is obtained from capacitance versus voltage (C–V) measurements on metal–insulator–semiconductor (MIS) and metal–insulator–metal (MIM) capacitors fabricated in the same sample. C_{OX} agrees with the expected parallel plate capacitor capacitance by using the obtained thickness and a dielectric constant of 9. More details are provided in [14]

$$I_{DS} = \frac{\mu_{SAT} C_{OX} W}{2L}(V_{GS} - V_{TH-SAT})^2. \quad (1)$$

Three devices with the same geometry were measured using this method, for a grand total of 45 measured devices per sample. The threshold voltage was calculated to be 2.2 ± 0.1 and 2.0 ± 0.07 V for ZnO and IGZO, respectively. The saturation mobilities were 14.2 ± 0.9 for ZnO and 9.0 ± 1.0 $cm^2 \cdot V^{-1} \cdot s^{-1}$ for IGZO. At $V_{off} = 0$ V and $V_{on} = 6$ V, the current ratio was $> 1 \times 10^8$ for both the oxide semiconductors. Drain current in the OFF-state ($I_{DS,off}$) is as low as 10^{-12}A for both the semiconductors. The summary of the V_{TH-SAT}, μ_{SAT}, and subthreshold swing (SS) obtained for ZnO and IGZO is shown in Fig. 3 as a function of the TFT aspect ratio. The stability of the TFT performance as a function of the device geometry demonstrates the reproducibility and yield of fabricated devices.

SS was extracted from the maximum slope obtained from the derivative of the transfer curve using (2). The calculated SS for devices with ZnO and IGZO was 130 ± 10.1 and 140 ± 15.3 mV/decade, respectively. Such values ensure a low gate driving voltage for TFTs, which reduces the overall power consumption in circuits

$$SS = \left.\frac{dV_{GS}}{d(\log I_{DS})}\right|_{max} \text{ at constant } V_{DS}. \quad (2)$$

Fig. 4 compares the linear scale plots of $(W/L) \times I_{DS}$ versus V_{GS} for ZnO and IGZO at $V_{DS} = 0.1$ V. As explained in [14],

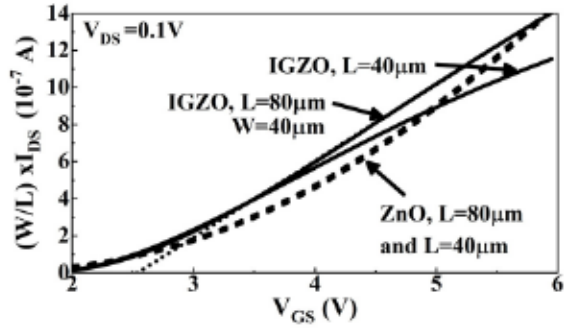

Fig. 4. Comparison of normalized I_{DS} versus V_{GS} at $V_{DS} = 0.1$ V for ZnO and IGZO at different channel lengths.

ZnO TFTs have small series resistance and mobility might increase with V_{GS} due to the nanocrystalline character of ZnO. This explains the increase in the slope of I_{DS} versus V_{GS} of ZnO. On the other hand, IGZO is amorphous, so mobility does not increase with V_{GS} and the slope of I_{DS} versus V_{GS} is constant for long-channel IGZO TFT ($L = 80$ μm). The slope of I_{DS} versus V_{GS} for IGZO decreases at large V_{GS} for short-channel TFTs ($L = 40$ μm) because of the IGZO series resistance. The S–D series resistance (R_s) was investigated using the method by Kazuo and Hiroki [24]. For TFTs with $W = 160$ μm, the series resistance was 0.2 ± 0.05 kΩ for ZnO and 12.2 ± 3.9 kΩ for IGZO. The transfer lengths obtained using this method were 1.1 and 2.6 μm for ZnO and IGZO, respectively. The large R_s obtained for IGZO might be due to oxygen migration at the S/D [19]. This oxygen migration can induce the formation of a thin Al_2O_3 layer that might increase the series resistance [25].

Gate and drain positive bias stress was used to evaluate the threshold voltage instability (ΔV_{TH-SAT}) after electrical stress to determine the reliability of the devices when implemented in digital circuitry. Gate and drain positive bias stress is performed by holding V_{GS} and V_{DS} at 6 V for a total of 1200 s and interrupted periodically to measure the transfer characteristics. The representative transfer characteristics after stress are shown in Fig. 5(a) and (b) for ZnO and IGZO, respectively. ΔV_{TH-SAT} is calculated as the difference between the threshold voltages extracted at each stress time step and the initial value at $t = 0$ s. Fig. 6 shows the induced ΔV_{TH-SAT}, SS, and μ_{SAT} as a function of the stress time.

For both the semiconductors, the transfer curves shift toward positive direction monotonically by incrementing the positive gate bias stress time, whereas SS does not show a clear change for ZnO and up to 740 s for the case of IGZO. At the end of the stress, ΔV_{TH-SAT} is about 0.4 and 1.5 V for ZnO and IGZO, respectively. Saturation mobility slightly decreases as a function of stress time.

Two main mechanisms for the ΔV_{TH-SAT} have been identified in the literature. One is the carrier trapping at the channel/dielectric interface [26], and the other the creation of additional states in the deep-gap states at or near the channel/dielectric interface [27]. The change in SS is directly proportional to the change in the dielectric–semiconductor interface defects [28]; therefore, we can analyze the trap change as a function of different stress times by monitoring the

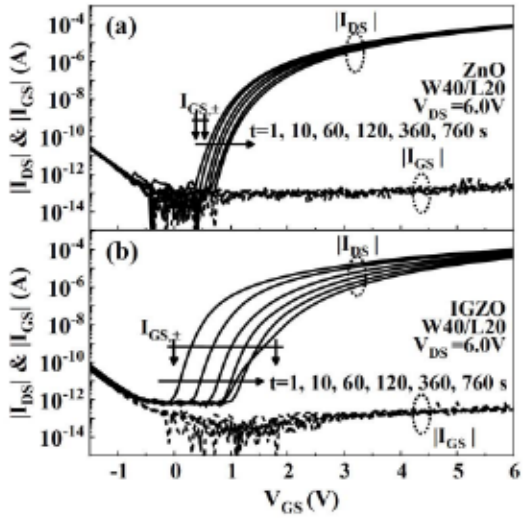

Fig. 5. Comparison of the representative transfer characteristic after the gate and drain bias stress cycles for (a) ZnO and (b) IGZO.

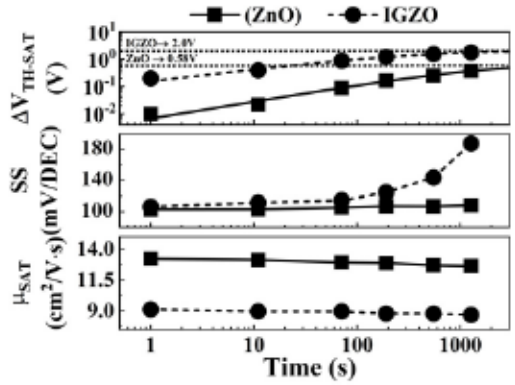

Fig. 6. Extracted saturation threshold voltage shift ($\Delta V_{\text{TH-SAT}}$), SS, and saturation mobility as a function of the stress time.

change in SS. Before stress, the SS is 130 and 138 mV/decade for ZnO and IGZO, respectively. After 1 s of stress, SS decreases to 103 and 106 mV/decade, respectively. At the end of the stress time (1200 s), the SS increases to 115 and 188 mV/decade for ZnO and IGZO, respectively. In both cases, the decrease in SS indicates that the defects already present in the semiconductor–dielectric interface are being filled [29]. Consequently, the positive $\Delta V_{\text{TH-SAT}}$ can be explained by negative charge screening of the applied gate bias [30].

Previous reports for a-IGZO TFTs have shown that the oxygen vacancy in a-IGZO can cause a decrease in film resistivity and a decrease in TFT subthreshold properties [31], [32]. These reported phenomena are similar to the a-IGZO I–V properties observed after long stress times (>740 s). However, the exact physical origin of this phenomenon is still unclear. Some authors suggest the meta-stable oxygen vacancies could be induced near the semiconductor/dielectric interface by prolonged stress [33]. Table I shows a comparison of the TFT parameters for each semiconductor.

The aging of the devices was studied by comparing the pristine TFT performance with that after six months of fabrication [Fig. 7(a) and (b)]. For the case of ZnO, there is a small decrease of 2.8%, 3.4%, and 2.6% in μ_{SAT}, $V_{\text{TH-SAT}}$, and SS, respectively. For IGZO, μ_{SAT} increases to 0.8%, despite $V_{\text{TH-SAT}}$ and SS decreasing to 5.4% and 23%, respectively. These results suggest that the protective and passivation layers (Parylene-C) are effective barriers against oxygen and water [34], even when they were deposited at RT. However, the improvement of SS and $V_{\text{TH-SAT}}$ in IGZO might be related to structure relaxation. Therefore, a soft-post IGZO and ZnO deposition anneal in oxygen could be further analyzed to minimize the aging effect and enhance the overall device stability.

TABLE I
ZnO and IGZO TFT Parameter Comparison

	ZnO	IGZO
$V_{\text{TH-SAT}}$ (V)	2.2 ± 0.1 V	2.0 ± 0.07
μ_{SAT} (cm^2/V^* s)	14.2 ± 0.9	9.0 ± 1.0
SS (mV/DEC)	130 ± 10.1	140 ± 15.3
I_{DS} at V_{GS}=V_{DS}=6 V (μA)	55.1 ± 2.2	29.9 ± 1.1
$V_{\text{TH-SAT},\infty}$ (V)	0.54	2.0
R_C (kΩ)	0.2 ± 0.05	12.2 ± 3.9
$R_{\text{SH-ON}}$ (kΩ/□)	47.1 ± 1.3	51.6 ± 2.2
$R_{\text{SH-OFF}}$ (GΩ/□)	400.9 ± 32.2	690.2 ± 30.1

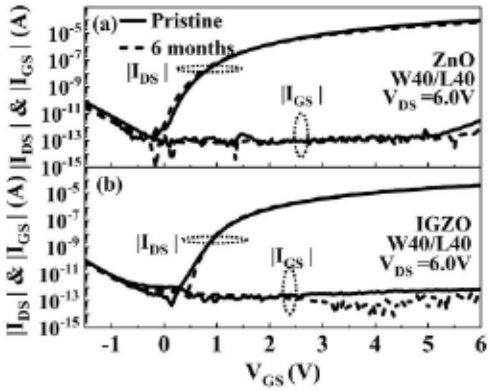

Fig. 7. Representative transfer characteristics comparison of pristine and 6 months after fabrication for (a) ZnO and (b) IGZO TFTs.

A. Inverters

To demonstrate the potential implementation and stability of the devices in digital electronics, active-load and saturation-load inverters were fabricated. The TFT dimensions for saturation load are 400/20 μm for drive and 20/20 μm for load (W/L). In the case of active load (zero drive), the load TFT dimension is 400/20 and 20/20 μm for the drive. The voltage transfer characteristics (VTCs) for the different inverter configurations are shown in Fig. 8(a) and (b).

The output voltage gain ($-dV_{\text{OUT}}/dV_{\text{IN}}$) is similar for both semiconductors: ~2.4 and ~25 V/V for saturation load and active load configurations, respectively. The input and output voltages at the high-state (V_{IH} and V_{OH}), low-state (V_{IL} and V_{OL}), and the undefined logic ($\text{NM}_H = V_{\text{OH}} - V_{\text{IH}}$ and $\text{NM}_L = V_{\text{IL}} - V_{\text{OL}}$) regions are shown in Table II. The output voltage at the high state and the low state were ~5.9 and

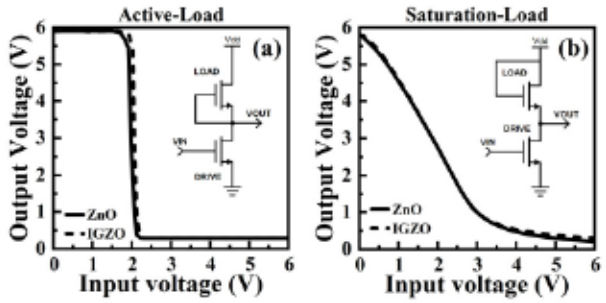

Fig. 8. DC response for logic inverters with (a) active load and (b) saturation load, respectively.

TABLE II
INPUT AND OUTPUT VOLTAGES AT HIGH AND LOW STATES

	Sat-Load ZnO	Act-Load ZnO	Sat-Load IGZO	Act-Load IGZO
V_{IH}	3.0	2.2	3.0	2.25
V_{IL}	1.7	1.85	1.8	1.95
V_{OH}	5.5	5.9	5.6	5.9
V_{OL}	0.25	0.3	0.27	0.3
NM_H	2.5	3.7	2.6	3.65
NM_L	1.45	1.55	1.53	1.65
DC Gain	2.4	24	2.3	26

0.3 V for active load and 5.5- and 0.25-V for saturation load. For each configuration, the inverting characteristic is similar regardless of the semiconductors; therefore, a more detailed analysis is required.

The saturation-load inverter uses a TFT as a load resistor in the saturation regimen ($V_{DD} = V_{GS}$). The load resistor remains in saturation regimen for all the inverting stages. During the low-input region ($V_{IN} \leq V_{IL}$), the load and drive TFTs are operating in the saturation regimen. In this regimen and for $0 \leq V_{GS} \leq V_{TH-SAT}$, the channel R_{SH} of the drive decreases with V_{IN} ($V_{IN} = V_{GS}$) causing a drop in V_{OUT} with increasing V_{IN}. Moreover, the transition region, $V_{IL} \leq V_{IN} \leq V_{IH}$, is dominated by the aspect ratio or geometry ratio of the inverter ($K_R = W_{Drive}L_{Load}/W_{Load}L_{Drive}$). The larger the K_R, the sharper the VTC. Nevertheless, the increase in K_R increases the area occupied by the inverter. A value of $K_R = (400/20)/(20/20) = 20$ is not clear enough to provide a sharp inverting transition for both semiconductors, as shown in Fig. 8(b). The combination of low K_R and subthreshold operation of the drive make V_{IL} to be independent of V_{TH-SAT}. In the high-input region, $V_{IN} \geq V_{IH}$, the drive TFT is in the linear regimen. Therefore, V_{OUT} is dependent on the linear-threshold voltage, V_{TE}. V_{TE} can be obtained with the transconductance method [28], which uses the linear extrapolation of $g_m - V_{GS}(V_{DS} = 0.1$ V) characteristic at its maximum first derivative point. The calculated V_{TE} values are 1.72 ± 0.12 and 1.76 ± 0.12 V for ZnO and IGZO, respectively. Since both semiconductors have similar V_{TE}, V_{IH} is expected to be similar, as shown in Fig. 8(b). The calculated value of V_{IH} is similar to the value experimentally obtained for both the semiconductors of ~3 V. The calculated value of V_{IL} is 1.7 and 1.8 V for ZnO and IGZO, respectively. However, because of the problems mentioned previously, this value is difficult to extract directly from the measured VTC.

The active load configuration provides an inverter with a higher gain having a sharper VTC, and hence increased noise margins. The low-input and high-input regions can be analyzed considering the load transistor in the linear region and the saturation, respectively. Similarly, the drive TFT is in the saturation region for the low-input region and in the linear regimen for the high-input region. The fast transition from V_{IL} to V_{IH} makes the regimen of the TFT to sharply change. Therefore, V_{IL} and V_{IH} are dominated by the combination of V_{TE} and V_{TH-SAT}, and not necessarily V_{TE} or V_{TH-SAT}, independently. The calculated V_{IL} are 1.9 and 2.0 V, and V_{IH} are 2.25 and 2.28 V for ZnO and IGZO, respectively. Calculated values are similar to measured values, as shown in Table II.

The fact that inverters behave alike even when IGZO has larger V_{TH} shifting, larger contact resistance, and smaller mobility than ZnO means that the overall dc performance of the inverters is relatively immune to the differences in the TFT performance, mainly due to range levels imposed on digital electronics. However, for continuous operation ($t \rightarrow \infty$), the circuit designer should consider the limits found previously for $\Delta V_{TH,\infty}$(0.58 V for ZnO and 2.0 V for IGZO), since this threshold shifting may compromise the electrical performance of the designed digital circuitry.

Being able to fabricate inverters (basics building blocks of digital electronics) immune to the TFT performance at such high yield and uniformity on the large substrate area is an advantage in the development of more complex digital circuitry involving more than two transistors, and even onto flexible substrates due to the low temperatures used for the fabrication process.

IV. Conclusion

A comparison of low-temperature fully patterned and passivated fabrication processes for oxide-based TFTs has been demonstrated. The fabricated TFTs demonstrated high yield and uniform TFT performance. The maximum process temperature of 115 °C makes this process suitable for flexible substrates. IGZO mobility is not largely dependent on gate voltage likely due to the lack of grain boundaries, which makes mobility dependent on V_{GS} for polycrystalline ZnO. The positive ΔV_{TH-SAT} obtained from reliability results is explained by negative-charge screening of the applied gate bias due to the filling of interface traps. The fully patterned fabrication process allows the fabrication of inverters (basic circuitry for digital electronics).

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