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# Relatively Low-Temperature Processing and Its Impact on Device Performance and Reliability

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Fabrication of $MoS_2$, ZnO, and IGZO transistors at low enough temperatures that are suitable for large-area/flexible electronics is presented. Evaluating critical processing conditions and approaches on device performance is critical to understanding and improving devices to enable large-area/flexible circuits for the IoT. For $MoS_2$, a study of the implications of photoresist residue on $MoS_2$ in the source/drain contact region was done. Results determined that an $O_2$ plasma exposure in this location can remove the resist residue and create a robust $TiOx/MoS_2$ contact, where an ~15x increase in mobility and ~20x reduction in contact resistance was achieved for $O_2$ plasma treated transistors. Thin-film transistor fabrication of ZnO and IGZO as the semiconductor yielded saturation mobilities of 14.2 and 9.0 $cm^2/V{\bullet}s$, respectively. Among other parameters, the contact resistance was noticeably lower for ZnO due to its polycrystalline morphology compared to the amorphous IGZO, which was determined to be more resistive.

## Introduction

Non-silicon, large-area/flexible electronics for the internet of things (IoT) has acquired substantial attention in recent years. Key electron devices to enable this technology include metal-oxide-semiconductor field effect transistors (MOSFETs), where ultra-thin and/or low-dimensional (i.e., 2D to a few layers) semiconductor materials may be required, like those found in thin-film transistors (TFTs) and transition metal dichalcogenide (TMD) FETs (1-8). Whether TFT or TMDFET, a relatively low-temperature process commensurate with large-area/flex applications to enable large (i.e., greater than 300 mm) and/or flexible substrate fabrication is required. Furthermore, TMD materials may be implemented as the channel semiconductor to function as an ultra-thin body to mitigate short channel effects and extend further scaling as the future progresses in CMOS scaling. In addition, the gate dielectric insulator is another vital component of any MOSFET that requires investigation as part of the MOS stack in these types of transistors. Lastly, semiconductor materials mentioned herein do not have a universally accepted way to introduce dopants to form sources and drains. Thus, metal-semiconductor contacts are employed where the interface region of the contact plays a critical role in determining the conductivity/resistivity of the contact. Moreover, how the metal-semiconductor interface is formed also impacts the quality of the contact. Therefore, exploration of low-temperature processing, interfaces, and their impact on device performance and reliability will be critical to eventual implementation in future

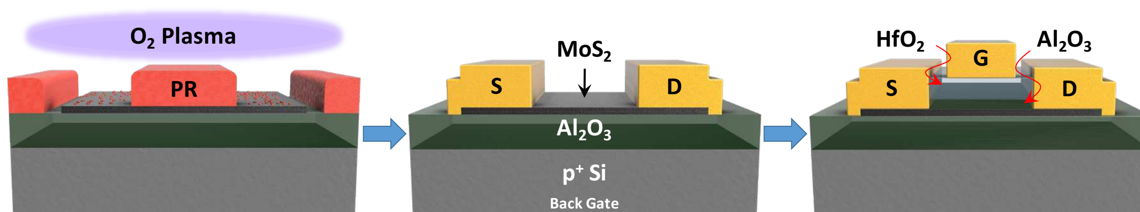


Fig. 1. Graphic illustrating the $O_2$ plasma exposure at the exposed contact areas after development of the photoresist, source/drain contact formation with back gate, and the final dual-gate FET.

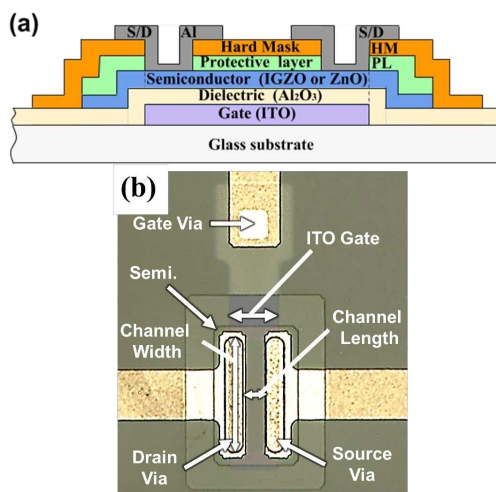


Fig. 2. a) Cross section of the thin-film transistor structure used in this work. b) The top view of a typical TFT measured. Measurements were made on similar devices with different channel lengths.

technologies. To ascertain the impact of low-temperature fabrication and critical interfaces, several process approaches and electrical characterization methods were employed (1, 2, 7-10) on molybdenum disulfide ($MoS_2$) or zinc oxide-based thin films serving as the semiconductor in field effect transistors.

## Experiment

### Fabrication

$MoS_2$ Field Effect Transistor (1). Initially, atomic layer deposition (ALD) of $Al_2O_3$ (27 nm) at 250°C onto a p+ Si wafer was performed with subsequent deposition of Al for a backside contact as well as a 400°C forming gas anneal to reduce charge traps. This backside layer serves as the 'substrate' for few-layer $MoS_2$ flakes (4-8 nm) (5). Using photolithography, source/drain contacts are defined and followed by e-beam evaporation of Ti/Au contacts with a lift-off process. For comparison, certain devices also had a direct $O_2$ plasma 5 sec exposure (“de-scum”) at 50W to remove any photoresist residue prior to contact metal deposition. Electrical back-gate measurements were performed. Then, a 300°C UHV anneal and 15 minute in-situ UV-ozone surface treatment was performed, followed by ALD of a $Al_2O_3/HfO_2$ (3nm/6nm) top-gate oxide at 200°C (11, 12) and Pd/Au top-gate electrode evaporation (Fig. 1).

ZnO-based Thin-film Transistor (2). TFTs were processed using a conventional, seven-mask photolithography fabrication flow that created a staggered bottom-gate/top-contact structure (Fig. 2). Initially, the process started with 135 nm of indium tin oxide (ITO) on a glass substrate. The ITO was patterned and used as the gate electrode. Next, an atomic layer deposited 17.5 nm aluminum oxide ($Al_2O_3$) at 100°C served as the gate dielectric. Then, a 45 nm ZnO-based thin film semiconductor is deposited by pulsed laser deposition (PLD) at 100°C with an oxygen pressure set at 20 mTorr. PLD requires targets to be ablated to form the semiconducting layers; therefore, zinc oxide (ZnO) and indium gallium zinc oxide (IGZO) targets (99.99% pure) were employed. Following the semiconductor deposition, a two-step passivation process using two depositions of parylene-C deposited by chemical vapor deposition at room temperature was executed (2). The first deposition passivated and protected the exposed top surface of the semiconductor from upcoming lithography. After lithographic patterning, the second layer of parylene-C was deposited as a hard mask to encapsulate the top and sides of the semiconductor. Finally, the source/drain vias are etched into the parylene-C by reactive ion etching followed by evaporation of 150 nm of aluminum (Fig. 2).

### Characterization

$MoS_2$ Field Effect Transistor. AFM and XPS were used to investigate the topographical and interfacial changes occurring on the $MoS_2$ layer throughout the contact formation process. A Keithley 4200 Semiconductor Characterization System was employed for the electrical characterization methodologies that included single-gate or double-gate (DG) bias sweeping of the top- and back-gate simultaneously during current – voltage (I-V) measurements.

ZnO-based Thin-film Transistor. A Keithley 4200 Semiconductor Characterization System executed I-V measurement methods and subsequent analysis of the TFTs under test.

## Results and Discussion

### Influence of Oxygen Plasma on Source and Drain Metal Contact Regions on $MoS_2$

As previously mentioned, the metal contact to the underlying semiconductor can have significant implications on the conductivity/resistivity of source and drain. Here, an evaluation of this metal – semiconductor interface that can be influenced by the source/drain contact process flow, as outlined in the experiment section, is conducted (1).

Without $O_2$ plasma exposure prior to Ti/Au deposition on $MoS_2$, the $I_D$-$V_D$ of $MoS_2$ FETs demonstrates non-linearity (Fig.3a, left), whereas those with exposure consistently showed linear behavior (Fig.3a, right) and higher saturation current (Fig.3b). This suggests that better carrier injection is achieved at the contacts as a result of the $O_2$ plasma exposure. AFM was used to investigate the $MoS_2$ surface as-exfoliated, post-photoresist development, and post-$O_2$ plasma exposure where the topographical images (Fig.4) indicate large photoresist island formation up to 20 nm in height and 50 nm in diameter during the lift-off process. This suggests the resist residue will likely cause discontinuous contact between the Ti contact metal and the underlying $MoS_2$. After $O_2$ plasma exposure, the large clusters of photoresist are removed, resulting in a roughness comparable to that of as-exfoliated $MoS_2$. This demonstrates that the 5 sec $O_2$ plasma

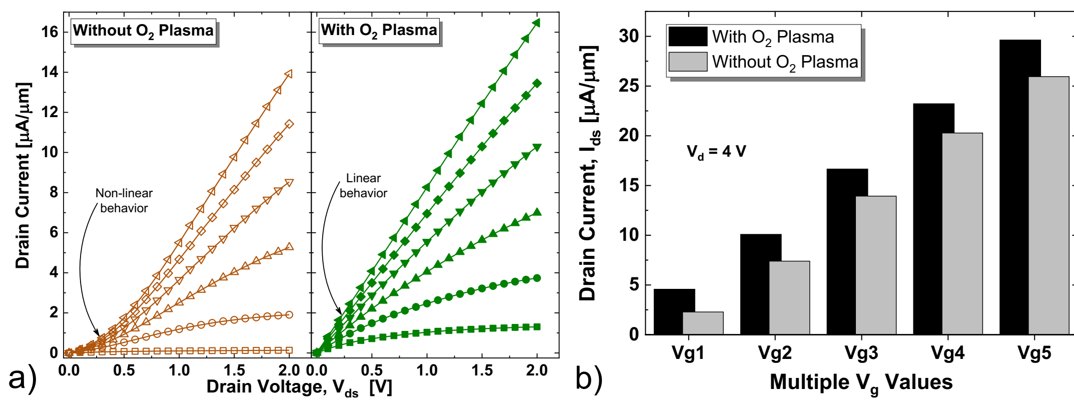


Fig. 3. a) Output characteristics ($I_{ds}$-$V_{ds}$) of $MoS_2$ FET with and without $O_2$ plasma. b) $I_d$ values extracted from $I_{ds}$-$V_{ds}$ data at 4 V, where the $O_2$ plasma results demonstrate better performance.

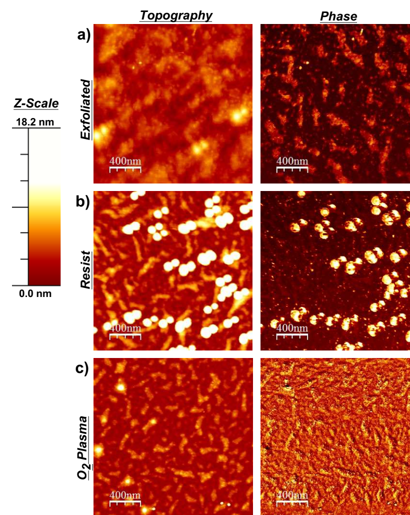


Figure 4. AFM topography and phase images obtained from a $MoS_2$ flake after (a) exfoliation, (b) photolithography processing, and (c) $O_2$ plasma exposure.

exposure post-development is enough to remove a majority of the residue prior to metal deposition. XPS analysis after exfoliation, development, plasma exposure, and Ti deposition in high-vacuum (HV) helps further elucidate the role of photoresist residue, $O_2$ plasma, and the subsequent chemistry formed after Ti deposition on $MoS_2$ (Fig. 5a-b). The initial comparison between as-exfoliated $MoS_2$ and after resist deposition/removal indicates a Fermi level shift towards the conduction band ($E_C$) edge, suggesting Fermi level pinning (FLP) near the $E_C$ is due to photoresist residue. Two different $MoS_2$ samples are used to demonstrate FLP at roughly the same energy near the $E_C$, regardless of the initial as-exfoliated $MoS_2$ Fermi level position (Fig. 5c). After $O_2$ plasma exposure, the XPS spectra indicates a Fermi level shift to its as-exfoliated value and formation of $MoO_x$ species. This suggests that a combination of hole injection by $MoO_x$ and removal of the residue causes the Fermi level shift towards the valence band after $O_2$ plasma. Subsequent Ti deposition indicates that the contact metal scavenges the oxygen species, reducing the $MoO_x$ to form $TiO_x$ (Fig. 5a-b), enhancing carrier injection likely due to a low conduction band offset of $TiO_2$ with $MoS_2$ (13). The removal of the residue coupled with the Ti oxygen gettering effect enables the dual-role of the short $O_2$ plasma exposure prior to contact metal deposition and formation of higher performing n-type contacts on

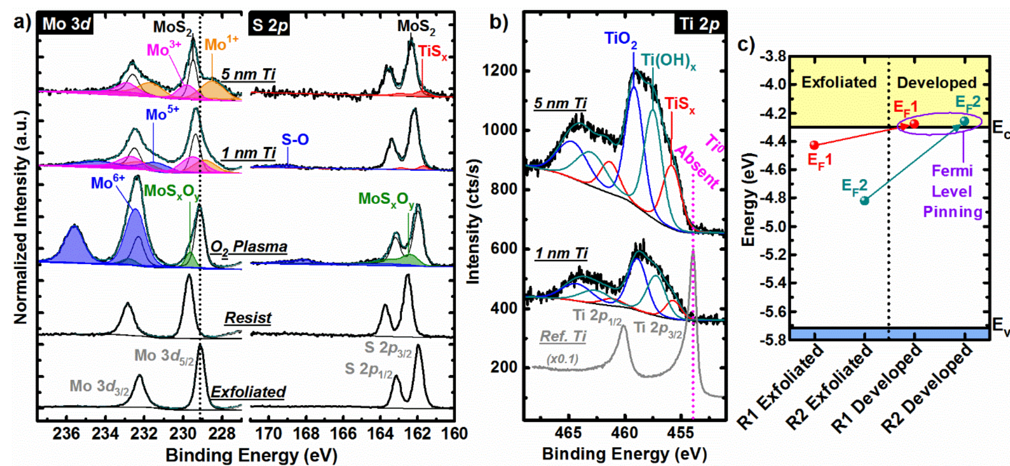


Figure 5. XPS core level spectra [(a) Mo 3*d*, S 2*p*, and (b) Ti 2*p*) obtained from bulk $MoS_2$ after exfoliation, photolithographic processing, 5 s $O_2$ plasma, 1 nm Ti deposition, and 5 nm Ti deposition. (c) Band alignment of two bulk $MoS_2$ crystals after exfoliation and photolithographic processing according to the measured valence band offset. [from (1)]

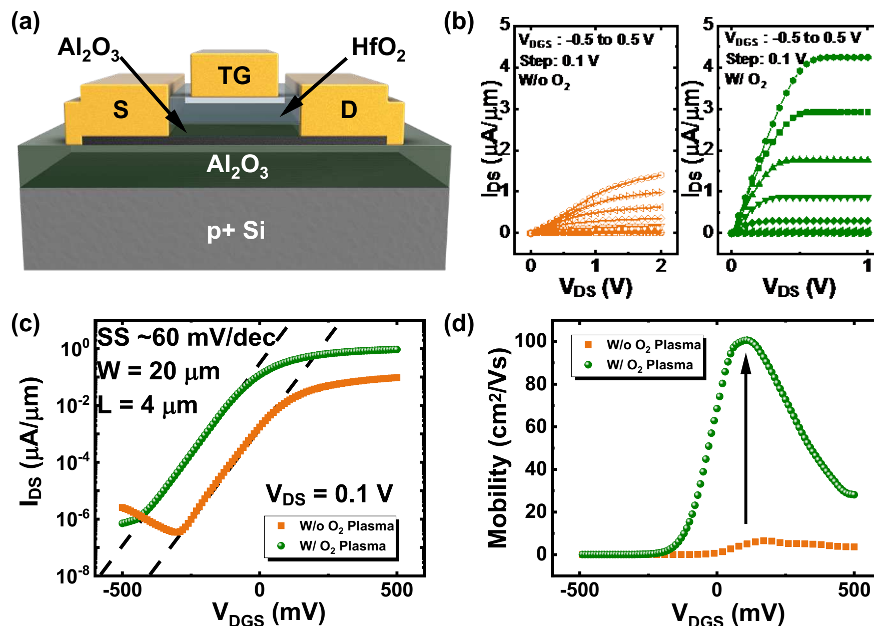


Figure 6. (a) Graphic cross-section of a DG $MoS_2$ FET.(b) Comparison of $I_D$-$V_D$ and **(c)** $I_D$-$V_G$ of DG $MoS_2$ FETs without and with $O_2$ plasma exposure at the contacts only. (d) Extracted mobility demonstrating a ~15× improvement. [from (1)]

contacts on $MoS_2$. After top-gate stack formation, DG $MoS_2$ FETs with and without $O_2$ plasma exposure at the contacts demonstrate non-linear and linear $I_D$-$V_D$ (Fig. 6b), respectively, even after the thermal heating from the UHV anneal and the ALD. Furthermore, the $I_D$-$V_G$ (Fig. 6c) shows major improvements in mobility (Fig. 6d) and $R_C$ due to formation of higher quality contacts.

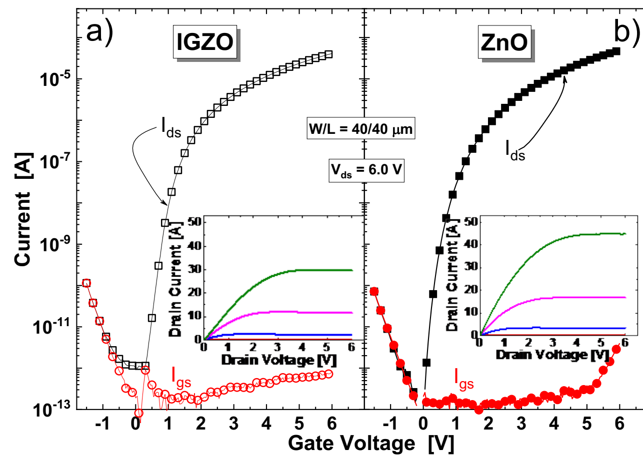


Figure 7. Typical transfer characteristics for a) IGZO and b) ZnO TFTs along with the respective $I_D$-$V_D$, where the ZnO TFT exhibits slightly lower off-state at $V_g = 0$ and gate leakage current ($I_{gs}$).

Comparison of Zinc Oxide and Indium Gallium Zinc Oxide Semiconductors in TFTs

In the quest for determining a semiconductor commensurate with low-temperature and/or flexible electronics, metal oxide semiconductors have garnered significant attention due to their relatively high carrier mobility and low process temperature compared to hydrogen-doped amorphous silicon, (a-Si:H) – the currently most used material in TFT display circuit technology (14). IGZO is currently being employed in liquid crystal display (LCD) technology with ultra-high pixel density (15). ZnO is another oxide-based semiconductor that is under intense investigation. However, ZnO and IGZO investigations at these necessary low temperatures require continued study. Therefore, the electrical performance characteristics of 100°C ZnO and IGZO with same $Al_2O_3$ gate dielectric, as outlined in the fabrication section, are presented herein.

First, X-ray diffraction of the PLD ZnO and IGZO was done in an effort to evaluate the morphology of the thin films. Results demonstrate that the ZnO is polycrystalline, and IGZO is amorphous. These findings were confirmed with transmission electron microscopy (not shown). The I-V characteristics are shown in Fig. 7, which clearly show transistor action. To determine the similarities and differences of ZnO and IGZO, further analysis was conducted using a straightforward model of the saturation drain current, $I_{d\text{-}sat}$ for FETs (eqn. 1), on experimental data from over 40 devices with varying channel lengths.

$$I_{ds} = \frac{\mu_{sat} C_{ox} W}{2L}\left(V_{gs} - V_{t-sat}\right)^2 \quad [1]$$

Here, $\mu_{sat}$ is the saturation mobility, W is the transistor width, L is the channel length, $C_{ox}$ is the gate dielectric capacitance, $V_{gs}$ is the applied gate voltage, and $V_{t\text{-}sat}$ is the saturation threshold voltage. From this equation and experimental data where $I_{ds}^{0.5}$ is plotted versus $V_{gs}$ (when $V_{gs} > V_{gs} - V_{t\text{-}sat}$), an extrapolation of a fitted line to the $I_{ds}^{0.5}$ data to the x-axis intercept defines the $V_{t\text{-}sat}$, and the slope of the line provides the saturation mobility when $C_{ox}$ is known. $C_{ox}$ is measured independently on metal- insulator-metal (MIM) devices that are fabricated on the same sample with the TFTs.

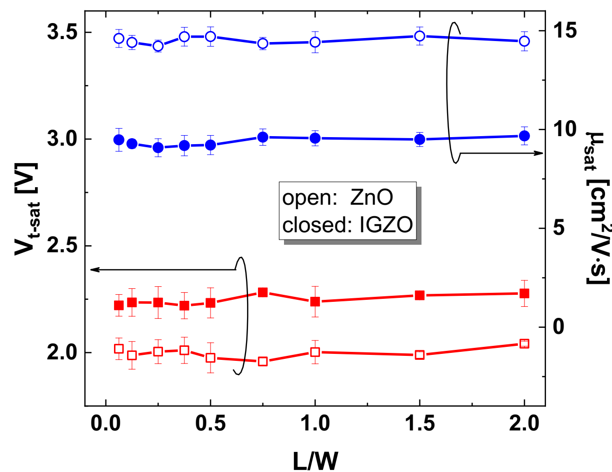


Figure 8. Extracted saturation threshold voltage ($V_{t\text{-}sat}$) and saturation mobility ($\mu_{sat}$) as a function of the device L/W.

Additional parameters of interest are the TFT on/off ratio, the subthreshold swing (SS), and series resistance. The on/off ratio is simply a way to assess the on-state current compared to the off-state current at an appropriate gate bias, respectively. For the off-state bias, 0 V was chosen while 6 V was selected for the on-state, and then on to off ratio was taken to provide the order of magnitude. Fig. 7 illustrates the off-state current at 0 V is around $10^{-12}$ A or less, which demonstrates relatively low leakage devices whether they are ZnO or IGZO, while both show quite similar on-state currents. Fig. 8 provides a comparison of the extracted $V_{t\text{-}sat}$ and $\mu_{sat}$ as a function of L/W.

When considering SS, providing information on the region of the $I_d$-$V_g$ data in which the SS is determined is necessary. Here, SS was extracted from the maximum slope of the derivative of this data using eqn. 2. Table I provides a summary of the extracted parameters for the ZnO and IZGO TFTs measured in this work.

$$SS = \frac{dV_{gs}}{d\left(\log I_{ds}\right)} \text{ at constant } V_{ds} \qquad [2]$$

Finally, Fig. 9 compares normalized, linear regime $I_d$-$V_g$ data of a few channel lengths at a drain bias of 0.1 V. The trends are within expectations, where the ZnO TFTs demonstrated lower series resistance and mobility that may increase with $V_{gs}$ due to the nanocrystalline nature of the ZnO (16). The electrical characteristics appear to corroborate this because the slope of $I_{ds}$ is increasing. Meanwhile, since the IGZO is amorphous, the mobility does not increase or may decrease with increasing $V_{gs}$ resulting in a constant or decreasing slope due to the S/D resistance in IGZO. Further investigation was conducted to determine the plausibility semiconductor morphology's role in the series resistance. The Terada and Muta method for S/D resistance extraction was implemented (17), and ZnO is a few orders of magnitude lower than IGZO (see Table I, $R_s$). Ref. (18) suggests that oxygen migration at the S/D regions induces a large $R_s$ due to a thin $Al_2O_3$ layer in the region.

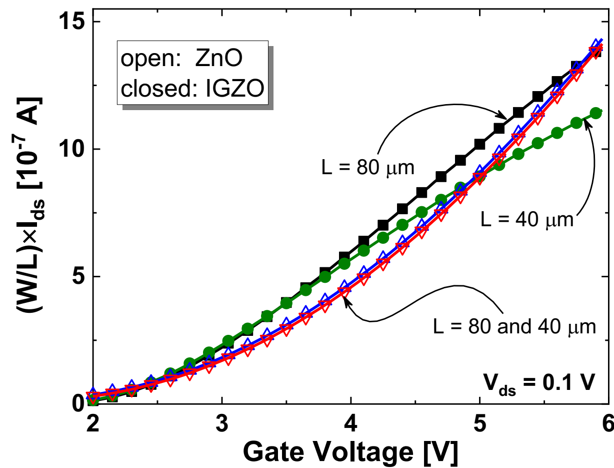


Figure 9. Normalized transfer characteristics in the linear regime ($V_{ds}$ = 0.1 V) for ZnO and IGZO TFTs.

**TABLE I.** Parameter comparison of ZnO and IGZO TFTs.

| Parameter | ZnO | IGZO |
|---|---|---|
| $V_{TH\text{-}SAT}$ (V) | 2.2 ± 0.1 V | 2.0 ± 0.07 |
| $\mu_{SAT}$ ($cm^2$/V·s) | 14.2 ± 0.9 | 9.0 ± 1.0 |
| SS (mV/DEC) | 130 ± 10.1 | 140 ± 15.3 |
| $I_{DS}$ at $V_{GS}$=$V_{DS}$=6 V (μA) | 55.1 ± 2.2 | 29.9 ± 1.1 |
| $V_{TH\text{-}SAT,\infty}$ (V) | 0.54 | 2.0 |
| $R_S$ (kΩ) | 0.2 ± 0.05 | 12.2 ± 3.9 |
| $R_{SH\text{-}ON}$ (kΩ/□) | 47.1 ± 1.3 | 51.6 ± 2.2 |
| $R_{SH\text{-}OFF}$ (GΩ/□) | 400.9 ± 32.2 | 690.2 ± 30.1 |

## Summary

For $MoS_2$ FETs, the results show that device fabrication induced contaminants, like photoresist residue, can substantially impact $MoS_2$ transistor performance if not properly eliminated. The $O_2$ plasma exposure in the S/D regions was quite effective in negating contaminates that would otherwise affect the S/D contacts leading to degraded performance. Thus, the combination of organic residue removal and high quality TiOx/$MoS_2$ contact formation demonstrates the benefits of the oxygen plasma exposure. The comparison of with and without $O_2$ plasma treatment shows an ~15x improvement in mobility and ~20x reduction in contact resistance when the plasma exposure is done. Also, a robust low temperature process for ZnO and IGZO TFTs was successfully demonstrated. ZnO TFTs achieved slightly better performance with a more appropriate Vt and higher mobility. In addition, the ZnO mobility increased with increasing $V_{gs}$, where the grain boundaries of the polycrystalline film was suspected to be the mechanism. The amorphous nature of IGZO is projected to be a more resistive material with higher series resistance thereby resulting in a decreasing mobility with increased $V_{gs}$. Continued investigations of process-induced effects are necessary to enable the best performance possible.

## Acknowledgments

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