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Transferred via contacts as a platform for ideal two-dimensional transistors

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Two-dimensional semiconductors have a number of valuable properties that could be used to create novel electronic devices. However, creating 2D devices with good contacts and stable performance has proved challenging. Here we show that transferred via contacts, made from metal embedded in insulating hexagonal boron nitride and dry transferred onto 2D semiconductors, can be used to create high-quality 2D transistors. The approach prevents damage induced by direct metallization and allows full glovebox processing, providing a clean, stable and damage-free platform for 2D device fabrication. Using the approach, we create field-effect transistors (FETs) from bilayer p-type tungsten diselenide (WSe_2) that exhibit high hole mobility and low contact resistance. The fabricated devices also exhibit high current and stability for over two months of measurements. Furthermore, the low contact resistance and clean channel allow us to create a nearly ideal top-gated p-FET with a subthreshold swing of 64 mV per decade at 290 K.

Two-dimensional (2D) materials, such as transition metal dichalcogenides (TMDCs), could be used to create electronic devices with unique capabilities. However, the difficulty of forming ohmic contacts to TMDC devices limits investigations of the fundamental properties of TMDCs and hinders fabrication of high-performance devices[1,2]. In addition, TMDC field-effect transistors (FETs) often degrade quickly, which further complicates the investigation of device properties because the measured characteristics vary over time, making parameter extraction and device comparisons difficult. Thus, the development of 2D devices requires reduced contact resistances and improved device stabilities.

Several techniques have been proposed to improve contacts to different TMDCs, including the use of tunnel barriers, contact-area doping and improved contact geometry[3–8]. Most of these techniques have been demonstrated on multilayer (more than five layers, 5L) TMDCs and cannot be easily scaled to few-layer devices due to the damage that occurs during processing. Moreover, the use of polymers, direct metallization and lack of effective passivation in previous methods result in Fermi-level pinning, threshold-voltage variation and unintentional doping and damage at the metal–semiconductor interface[9,10]. Device stability has been greatly improved through insulating hexagonal boron nitride (h-BN) encapsulation of 2D-material channels[11]. However, conventional metal evaporation, which is used to make contacts, often leads to significant damage and leaves polymer residue at the contacts, causing variable device performance over time.

In this Article, we report a platform for creating high-quality transistors made from 2D semiconductors using transferred via contacts (TVCs) made from metal-embedded h-BN. We show that our TVC platform provides multiple advantages over conventional 2D device fabrication: encapsulation of the 2D semiconductor, shielding the channel and contacts from contamination; full glovebox processing, providing a pristine channel for high-mobility FETs and a clean, polymer-free metal–semiconductor interface that reduces contact resistance; a damage-free contact by avoiding direct metallization of the semiconductor, enhancing device stability; a high-quality gate insulator, yielding a nearly ideal subthreshold swing for top-gated transistors.

We use bilayer tungsten diselenide (WSe_2) p-FETs as our testbed for the TVC platform, and perform detailed multi-terminal measurements—transfer length method (TLM), four-probe and Hall effect—to accurately extract the channel properties independent of the contacts, because contact resistance plays a large role in determining the measured transistor characteristics of 2D devices. We chose p-type WSe_2 because it complements n-type molybdenum disulfide (MoS_2) for the creation of p–n heterojunctions and complementary FET applications. Furthermore, bilayer WSe_2 has received significant research attention in the study of excitonic dynamics, spin-locking, piezoelectricity and the quantum Hall effect[12–15]. Bilayer WSe_2 is also notoriously difficult to contact, which makes it valuable in demonstrating the advantages of TVCs. Using the TVC plaform, we create a high-performance double-gated bilayer WSe_2 p-FET with a large on/off ratio (10^6), high on current ($5\,\mu A\,\mu m^{-1}$ for $V_{DS} = -100$ mV at 295 K; $200\,\mu A\,\mu m^{-1}$ for $V_{DS} = -1.5$ V at 14 K), a nearly ideal subthreshold swing (64 mV dec^{-1} at 290 K) and long device stability (more than 2 months).

The concept of transferred contacts to 2D materials has been reported recently in refs. [16,17]. In ref. [16], a polydimethylsiloxane (PDMS) stamp was used to transfer 50-nm-thick metal contacts embedded in polymer to multilayer (4–20 nm) MoS_2. The transferred contacts showed promising advantages compared to evaporated contacts, including a lack of visible damage in cross-sectional transmission electron microscope (TEM) images and greatly reduced Fermi-level pinning that enabled both p-type and

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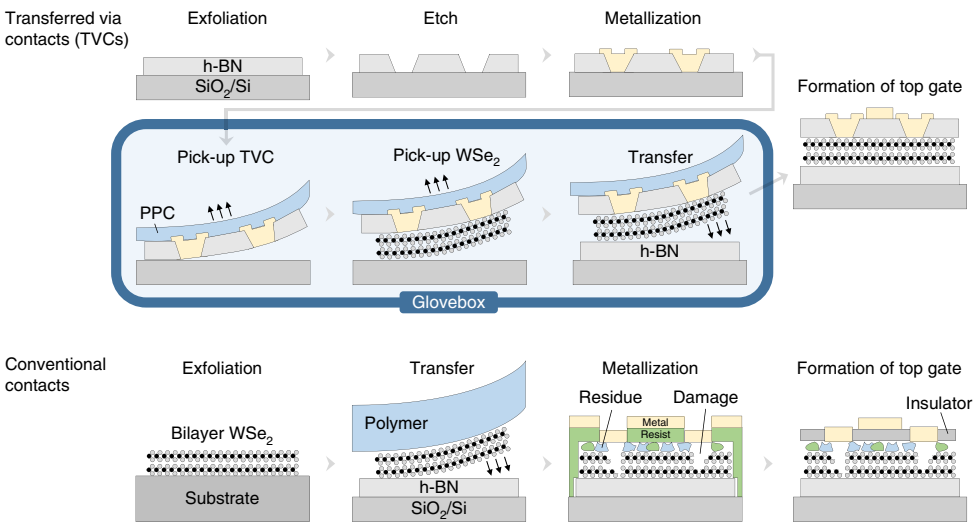

Fig. 1 | Fabrication process for TVCs and conventional contacts. TVCs are formed outside the glovebox and then transferred onto the semiconductor inside the glovebox. TVCs prevent contamination and damage to the 2D semiconductor surface that occur during fabrication of conventional contacts.

n-type characteristics by using metals with different workfunctions. However, the transferred contacts place a PDMS stamp in direct contact with the semiconductor channel, leading to potential contamination. Moreover, the focus of that work was on the Schottky-barrier extraction for different metals transferred onto relatively thick (6–30 layer) MoS_2. The work also did not use multi-terminal measurements (that is, four-probe and TLM), which prevented the extraction of contact resistance independent of the channel resistance. Reference [17] reports the development of TVCs, focusing on physical characterization (that is, the roughness and interface of the contacts), and shows good contact resistance to semimetallic graphene and superconducting $NbSe_2$ at both 1.7 and 300 K. The encouraging results of that work provide strong motivation to demonstrate the potential of the TVC platform on semiconducting 2D materials.

Transferred via contacts

Figure 1 highlights the major fabrication steps for TVCs and a conventional process with direct metallization. In our method, a 2D semiconductor is exfoliated inside a glovebox with an inert nitrogen ambient to minimize atmospheric contamination and prevent direct contact with the polymers and solvents used in material transfer and lithographic patterning. TVCs are prepared outside the glovebox and then brought inside to pick up the 2D semiconductor layer and transfer it onto a bottom h-BN layer, minimizing contamination of the metal surface. The top TVC and bottom h-BN provide atomically flat, ultraclean encapsulating surfaces for the 2D semiconductor. The process minimizes contamination between the metal–semiconductor interface, potentially minimizing traps at the contact. (Additional process details are provided in the Methods.)

In contrast to TVCs, conventional contacts introduce residue on the 2D material due to direct contact with polymers, such as PDMS, used to pick up the 2D semiconductor layer. The semiconductor is further contaminated by the chemicals and resist used in subsequent lithography steps. This contamination accumulates over the process steps as well as during exposure to the ambient, which may result in unintentional doping, defects, strain and, consequently, degradation in the quality of the 2D surface. The contaminants may also exist at the metal–semiconductor interface, thereby resulting in poor contacts that severely limit device performance. Moreover, it has been shown that direct metallization of thin layers of 2D material causes physical damage to the surface[9,16]. Thus, the conventional process prohibits fine control over the contact and channel quality, thereby yielding large variations and poor reliability from device to device.

Electrical properties of back-gated p-FETs with TVCs

We performed room-temperature electrical characterization of back-gated bilayer WSe_2 devices with TVCs, as shown in Fig. 2. Platinum was used for contacts to WSe_2 due to its large workfunction, inert behaviour and strong electronic coupling between Pt and WSe_2 (ref. [18]). Figure 2b shows the cross-sectional device schematic with electrical connections. Here, the back-gate voltage (V_{BG}) is applied across the WSe_2 through an ~30 nm h-BN/~285 nm SiO_2 dielectric stack. Figure 2c,d shows the output and transfer characteristics of a device with 1 μm channel length, measured while using the two leftmost contacts of Fig. 2a as the source and drain. The output characteristics show linear behaviour over a range of V_{DS} for various gate voltages. The transfer curves show clear p-type characteristics with high on current (5 μA μm^{-1} at $V_{DS} = -100$ mV), extremely low threshold voltage variation and a good subthreshold swing for a back-gated device, illustrating the high quality of devices made with the TVC platform.

To quantify the advantage of TVCs, we extracted the width-normalized contact resistance (R_c) for back-gated WSe_2 devices using the TLM. Figure 3a shows the output characteristics for devices with different channel lengths at $V_{BG} = -80$ V. For channel lengths greater than 3 μm, characteristics were measured across contacts as indicated in the inset of Fig. 3a. Here, we have assumed that the channel segments covered by the metal contact do not contribute to the overall channel length[19], which is reasonable given the excellent linear fit of Fig. 3b.

The total resistance normalized by width (R_{total}) was obtained from the slope of the I_D versus V_{DS} curve at low bias for different channel lengths. Figure 3b plots R_{total} as a function of channel length and shows an excellent linear fit to the data, indicating low variability among the contacts and channels. The y intercept of the linear fit yields the total contact resistance ($2R_c$) and the slope gives the sheet resistance of the channel (R_{sh}), as indicated in Fig. 3b. Using this methodology, we extract a low contact resistance of ~3.5 kΩ μm at $V_{BG} = -80$ V.

To further elucidate device behaviour, we performed four-probe measurements of the TLM structure to independently extract the channel (R_{ch}) and contact ($2R_c$) resistances as a function of V_{BG},

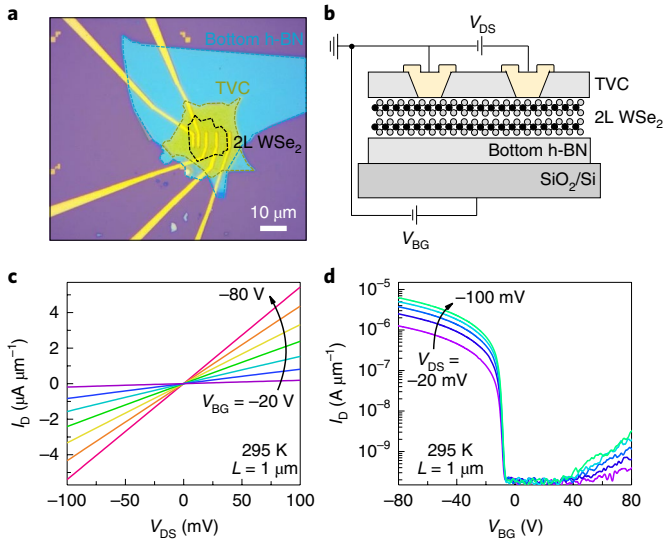

Fig. 2 | Electrical properties of bilayer WSe_2 with TVCs at 295 K. a, Optical microscope image of a bilayer WSe_2 back-gated p-FET with TVCs in a TLM arrangement. The metal width of the Pt TVCs is 6 μm. **b**, Schematic and circuit diagram of the device. **c**,**d**, Output (**c**) and transfer characteristics (**d**) for a device with 1 μm channel length.

as shown in Fig. 3c. For large negative V_{BG}, the device is channel-dominated as the channel resistance is significantly higher than the contact resistance. For $V_{BG} \gtrsim -38$ V, the device becomes contact-dominated as the contact resistance rises faster than the channel resistance. The four-probe data clearly show a contact-dominated turn-on of the device at $V_{BG} \sim -15$ V (Fig. 2d).

The R_{ch} and $2R_c$ extracted through the four-probe method corroborate the values extracted through TLM analysis. The four-probe measurements give $2R_c \sim 8\,k\Omega\,\mu m$, while TLM gives $7\,k\Omega\,\mu m$ at $V_{BG} = -80$ V. Similarly, four-probe and TLM measurements both yield $R_{ch} \sim 65\,k\Omega\,\mu m$ for a 6 μm channel at $V_{BG} = -80$ V.

Details of the four-probe extraction are provided in the Methods, and Supplementary Fig. 2 plots the raw data of the measured four-probe and two-probe resistances as a function of back-gate voltage.

We next compare the contact resistance for TVCs to WSe_2 with other contact methods. The contact resistance to TMDCs depends on several factors such as contact metal, channel thickness (that is, number of 2D layers) and layer doping (expressed by R_{sh}). Thus, for a fair and reliable comparison we plot the extracted contact resistances as a function of the number of layers (Fig. 3d) and channel sheet resistance (Fig. 3e). For the various published results, contact resistance was extracted using TLM[5,7], four-probe measurements[4,20–22] or on-resistance (assuming $R_{on} \approx 2R_c$ at high V_{BG})[23–27]. Our TVC technique provides the best contact resistance for thin (<10 layers) WSe_2, even while maintaining reasonable R_{sh} (10^3 to $3.5 \times 10^4\,\Omega\square^{-1}$). This twofold comparison is important, as many of the previous contact methods are based on degenerate doping of the channel, which leads to poor gate control. The contact resistance further improves as the temperature is reduced, which is discussed in detail in the section on low-temperature measurements and the transport model.

Layer dependence of WSe_2 FETs with TVCs

To explore the layer-dependence of TVCs, we fabricated monolayer (1L), six-layer (6L) and 13-layer (13L) WSe_2 devices, as shown in Supplementary Figs. 3–5. Structures for these devices were assembled inside the glovebox following the same process as used for bilayer devices.

As shown in Fig. 3d,e, the contact resistance for the 1L device ($2R_c \sim 100\,k\Omega\,\mu m$ from R_{ON} extraction) is considerably higher than that for the bilayer, probably due to the larger bandgap and lower-lying valence band edges that increase the contact barrier. Interestingly, the extracted R_c and R_{sh} for the 13L device are also higher compared to the bilayer ($2R_c = 7\,k\Omega\,\mu m$ for 2L at $V_{BG} = -80$ V versus $18\,k\Omega\,\mu m$ for 13L at $V_{BG} = -100$ V). We believe the increased R_c of the 13L device may be attributed to the interlayer resistance of the 13-layer stack because the back-gate accumulates holes on the bottom surface but the contacts are on the top surface, and the cumulative interlayer resistance from the top to the bottom of the device increases for thicker WSe_2. An increase in R_c with layer thickness has also been previously seen in Nb-doped WSe_2 top contacts (see supplementary fig. 4 of ref. [7]). Thicker channels also more effectively screen the back-gate field near the top contacts, such that the back-gate is less able to electrostatically dope the semiconductor immediately adjacent to the top contacts, further increasing contact resistance.

A comparison of transfer characteristics for different layer thicknesses of WSe_2 is shown in Supplementary Fig. 5. The bilayer device with TVCs shows the best electrical performance among the layer thicknesses that have been tested (1L, 2L, 6L and 13L); however, further experiments are needed to determine if the bilayer is truly a sweet spot in terms of device performance or if the TVC process can be further optimized for thicker multilayer channels to yield better transfer characteristics.

Low-temperature measurements and transport model

We also investigated the temperature dependence of our back-gated bilayer WSe_2 p-FETs with TVCs using low-temperature I–V characterization. Figure 4a shows the transfer characteristics at $V_{DS} = -100$ mV for multiple temperatures between 14 and 295 K. The data clearly depict that the subthreshold swing is nearly constant over the entire temperature range. Note that the device is contact-dominated for $V_{BG} \geq -38$ V (as shown in Fig. 3c), which encompasses the entire subthreshold regime. Therefore, the temperature-independent subthreshold swing provides strong evidence of tunnelling transport at the contacts[28,29].

The output curves maintain their linearity even at 14 K and show high saturation current ($-200\,\mu A\,\mu m^{-1}$ at $V_{DS} = -1.5$ V, $V_{BG} = -100$ V) as shown in Fig. 4b. Overall, the contact resistance is observed to halve as temperature is reduced from 295 to 14 K (Fig. 4c). This reduction in R_c supports our claim of tunnelling-dominated transport at the contact as a thermionic model would yield an exponential increase in R_c at low temperature due to there being fewer carriers with enough kinetic energy to surmount the Schottky barrier of the contact. Detailed calculations of transport at the contacts demands the development of new models that consider the distinct electrostatics of back-gated 2D devices as compared to 3D 'bulk' semiconductors[30].

To extract the hole field-effect mobility, we measured the transfer characteristics at small $V_{DS} = -20$ mV from which we calculated the transconductance ($g_m = \partial I_D / \partial V_{BG}$) at $V_{BG} = -80$ V, as shown in Fig. 4d. We used a large negative back-gate voltage to ensure that the device was channel-dominated (Fig. 3c) and biased in the linear regime of operation, as required for proper field-effect mobility extraction. The extracted hole sheet density (p_{2D}) and field-effect mobility (μ_{FE}) are shown in Fig. 4e,f. Details of the extraction procedure are provided in the Methods.

At 295 K, the extracted four-probe hole mobility is quite high ($\mu_{FE} = 195\,cm^2\,V^{-1}\,s^{-1}$ at $p_{2D} = 3 \times 10^{12}\,cm^{-2}$), especially considering the large hole density in the channel at $V_{BG} = -80$ V. The field-effect mobility increases to $1{,}155\,cm^2\,V^{-1}\,s^{-1}$ at 14 K but starts to saturate, suggesting the dominance of impurity scattering at very low temperatures[31]. The difference between the two-probe and four-probe measurements is small at high temperature because the channel

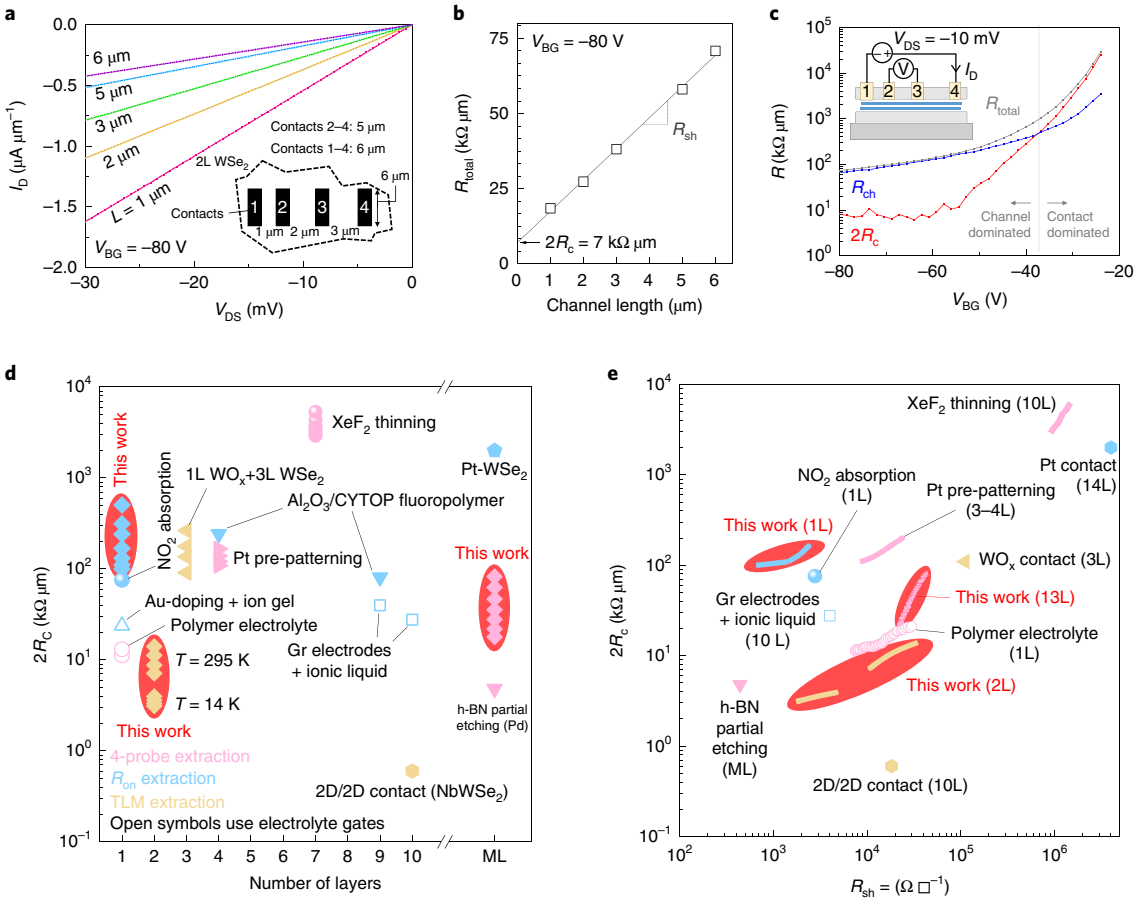

Fig. 3 | Contact properties of bilayer WSe_2 p-FETs with TVCs. TLM results are taken at 295 K. **a**, I_D–V_{DS} curves for different channel lengths at V_{BG} = −80 V. Inset: TLM contact numbers and spacing. **b**, Total resistance normalized by width (R_{total}) as a function of channel length, determined from the slopes of **a**. The *y* intercept yields twice the contact resistance ($2R_c$), and the slope yields the sheet resistance (R_{sh}). **c**, Extracted channel resistance (R_{ch}) and total contact resistance ($2R_c$) from the four-probe measurement depicted in the inset. The same structure from **a** was used for the measurement. Data for V_{BG} > −24 V cannot be reliably extracted due to the large contact resistance preventing accurate voltage measurements. **d**,**e**, Comparison of $2R_c$ as a function of the number of layers (**d**) and sheet resistance of WSe_2 (**e**).

resistance is considerably higher than the contact resistance, whereas it becomes larger at low temperature as $2R_c$ becomes a large fraction of the total resistance (Supplementary Fig. 6).

To provide further information on the mechanisms of device operation, we fabricated a Hall-bar structure and performed Hall-effect measurements to obtain the hole sheet density and mobility (shown in Supplementary Fig. 7). At 290 K, the hole sheet density for the Hall-bar structure ranges from 1 to 6×10^{12} cm^{-2} for V_{BG} = −60 to −100 V, which is in good agreement with the sheet density extracted from the transfer curves of the TLM structure (1.6 to 4.3×10^{12} cm^{-2} for V_{BG} = −60 to −100 V) (Fig. 4e). For the Hall-bar structure, the extracted room-temperature Hall mobility varies from 200 to 700 cm^2 V^{-1} s^{-1}) over the range of V_{BG} = −60 to −100 (Supplementary Fig. 7). (Although the extracted Hall mobility is higher than the field-effect mobility presented in Fig. 4e, we do not feature this data in the main manuscript due to the presence of a multilayer WSe_2 flake near two of the channel contacts, which may affect the uniformity of current flow through the structure.)

Effects of glovebox processing and metallization

So far, nearly all published research on WSe_2 has been conducted outside of the glovebox because WSe_2 is considered to be air stable. Furthermore, device fabrication of conventional contacts has necessitated exposing samples to air and photoresist during metallization. To evaluate the effects of different processing techniques, we fabricated bilayer WSe_2 p-FETs with three different processes for obtaining metal contacts: (1) a device with TVCs assembled inside the glovebox; (2) a device with TVCs assembled outside the glovebox; (3) a device with direct electron-beam metal evaporation through a window in h-BN. In the direct metallization process, h-BN was used to protect the channel during metallization so that any observed differences in the device characteristics could be attributed to the contact as opposed to the channel, which may be affected during conventional metallization of an unprotected channel.

Figure 5a presents a comparison of the transfer characteristics for devices made with the three different processes. Note that the applied V_{DS} is 10× larger for the devices fabricated outside the glovebox (−1 V versus −0.1 V) because they exhibited very small currents, and a larger drain voltage was necessary for accurate measurement.

The device with TVCs assembled inside the glovebox shows a p-type threshold voltage (V_T) near V_{BG} = −20 V, a good subthreshold slope for a back-gated device and a large on current. Weak n-type conduction is seen for V_{BG} ≥ 30 V. This behaviour is consistent with a close alignment of the Fermi level of the metal contact (Pt) with the WSe_2 valence band. The device with TVCs assembled outside the glovebox shows a −10 V shift in V_{BG} at the onset of both p-type and n-type conduction, significantly decreased p-type on current

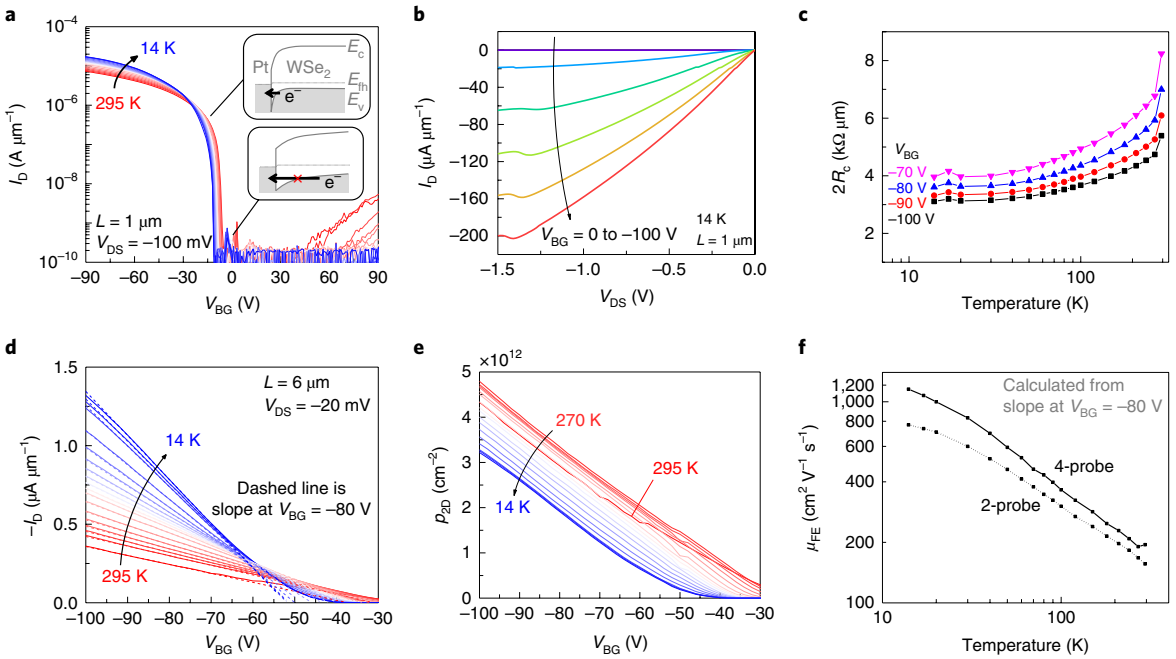

Fig. 4 | Low-temperature measurements for a back-gated bilayer WSe_2 p-FET with TVCs. a, Temperature-dependent transfer curves at $V_{DS} = -100$ mV. Inset: turn-on of tunnelling at the contacts. **b**, Output curves at 14 K for large $|V_{DS}|$. **c**, Contact resistance as a function of temperature. The decrease in R_c with decreasing temperature suggests that tunnelling occurs at the contacts, as opposed to thermionic emission. **d**, Linear-scale temperature-dependent transfer curves at $V_{DS} = -20$ mV. Dashed lines indicate the slope at $V_{BG} = -80$ V from which the hole sheet density and hole mobility are calculated. **e**, Extracted hole sheet density (p_{2D}) as a function of V_{BG} for different temperatures. **f**, Extracted field-effect mobility (μ_{FE}) as a function of temperature from two- and four-probe measurements. The four-probe measurement eliminates the impact of series resistance on mobility extraction.

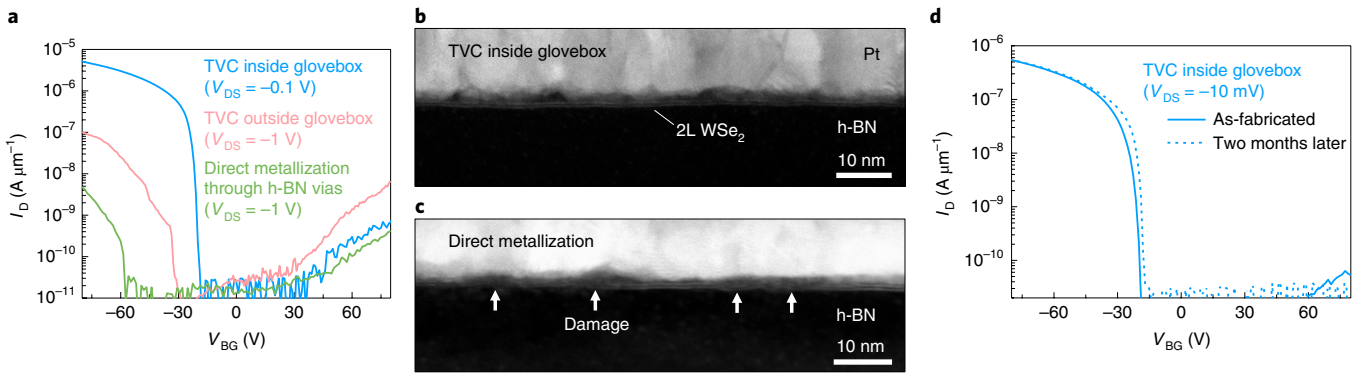

Fig. 5 | Effects of direct metallization and glovebox processing. a, Comparison of transfer characteristics for bilayer WSe_2 devices with different processing conditions. The top two curves are devices with TVCs. Complete glovebox processing with TVCs (blue curve) yields a high-quality device with a large on current. Device characteristics significantly degrade when the device is made outside the glovebox (pink curve) and further degrade when direct metallization (electron-beam evaporation) is used to form the contacts (green curve). **b**,**c**, TEM images of contacts to WSe_2 with TVCs inside the glovebox (**b**) and direct metallization (**c**). Damage is visible under the contact in the device with direct metallization. **d**, Stability of transfer characteristics of the transferred via-contacted device over time. (After two months, the device was sacrificed for TEM imaging.)

and a shallower subthreshold slope. These changes are consistent with a shift in the alignment of the Fermi level of the metal contact towards the mid-gap of the WSe_2, increasing the barrier for hole injection. Such a shift can occur due to interfacial contaminants, such as water and hydrocarbons, at the metal–semiconductor junction. Hysteresis in the transfer characteristics provides additional evidence of charge trapping caused by interfacial contamination. Such hysteresis is clearly present for devices assembled in air, while it is largely absent for devices with TVCs assembled inside the glovebox (Supplementary Figs. 8 and 9).

The device with direct metallization through windows in h-BN shows poorest performance, with very poor p-type device characteristics with only nanoamps of current in the on state (similar devices without h-BN encapsulation (shown in Supplementary Fig. 8) exhibit even worse characteristics and n-type behaviour). Interestingly, the device shows a wider off region than the TVC devices, with the threshold voltage for p-type conduction shifted downward to −60 V, whereas the threshold for n-type conduction is unchanged. This behaviour is consistent with metallization-induced mid-gap states in the semiconductor, which pin the Fermi

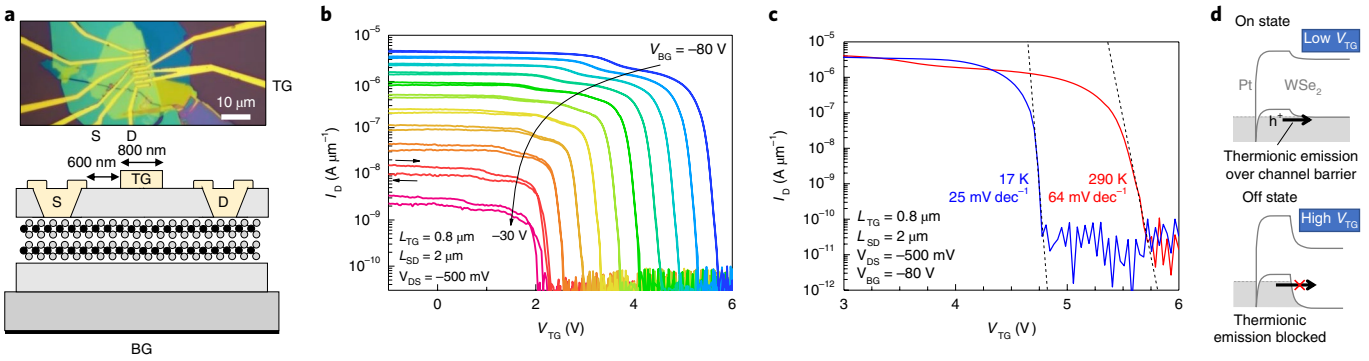

Fig. 6 | Double-gated bilayer WSe_2 with TVCs as a nearly ideal 2D p-FET. a, Optical-microscope image and schematic diagram. **b**, Top-gated transfer characteristics with V_{BG} varied from −30 to −80 V. Negligible hysteresis is shown for highly negative V_{BG}. **c**, Temperature-dependent transfer characteristics showing a subthreshold swing of 64 mV per decade at 290 K and 25 mV per decade at 17 K. **d**, Band diagram of the on and off states of the device. As V_{TG} increases, the barrier between the source and channel increases, blocking thermionic emission of holes into the channel and giving rise to a thermal dependence of the subthreshold swing.

level of the contact near the mid-gap and act as traps that widen the off region.

To explore how direct metallization might create mid-gap states, we acquired cross-sectional TEM images of the TVCs and direct metallization contacts, as shown in Fig. 5b,c (raw images are shown in Supplementary Fig. 10), to elucidate the physical differences between the two methods. No damage to WSe_2 is apparent under the metal in the device with TVCs; however, damage is observed for the direct metallization contact. WSe_2 appears discontinuous across the metallization region, which we believe is the main reason for the high R_c, large variability and the mid-gap states in directly metallized devices. These observations are consistent with recent studies comparing direct metallization to lamination of metal contacts[16]. Thus, direct metallization not only shifts V_T but also extends the V_{BG} window of the off state, suggesting that metallization-induced damage may create mid-gap traps that decrease gate efficiency.

Figure 5d shows the stability of the device characteristics over time for TVCs processed inside the glovebox. The device shows wonderful stability for two months after fabrication, which we attribute to the full h-BN encapsulation and glovebox processing, resulting in a clean and damage-free WSe_2 surface. After two months, the device—which was still working—was sacrificed for TEM imaging.

Double-gated device as a nearly ideal 2D p-FET

To further demonstrate the capabilities of TVCs as a device platform we fabricated double-gated devices featuring a local top gate on bilayer WSe_2. The top gate was formed directly on the h-BN of the TVCs (Fig. 6a). The top gate enables independent gating of the channel region, in contrast to the back gate, which modulates both the channel and contact regions. As shown in the optical image, the presence of a high-quality h-BN layer on top of the channel makes it easy to pattern the top gate using conventional lithography and metallization.

Figure 6b illustrates the top-gate transfer characteristics of the double-gated structure at different V_{BG}. The output characteristics of the same device show clear current saturation at large $|V_{DS}|$, as shown in Supplementary Fig. 11a. The increased on current and improved subthreshold swing of the top-gated device can be attributed to the high-quality h-BN–WSe_2 interface, which lacks dangling bonds and hence minimizes interface traps. The double-gated structure also enables V_T tunability by modifying the V_{BG}. V_T for the top gate shifts positively with more negative V_{BG} because a large negative back-gate voltage induces many holes in the channel and therefore requires a more positive top-gate voltage to deplete holes from the channel to turn the device off.

In these devices, the back gate is used to 'turn on' the contacts while the top gate is used to control the potential barrier of the channel, as illustrated in Fig. 6d. The device is on at $V_{TG}=0$ V—the potential barrier of the channel is minimal and the device current is limited by the contact resistance (which is dependent on V_{BG}, as shown in Fig. 3). The device is turned off as V_{TG} is increased—the potential barrier of the channel increases causing an exponential decrease in the drain current. In this configuration, the switching characteristics are due to the top-gate modulation of thermionic emission over a potential barrier, and hence, a thermal dependence of the subthreshold swing is expected. Indeed, the TVC top-gate devices show a nearly ideal subthreshold swing of 64 mV per decade at room temperature and 25 mV per decade at 17 K, as shown in Fig. 6c. The low-temperature subthreshold swing further decreases to 12 mV per decade at $V_{DS}=-10$ mV (Supplementary Fig. 11b). The characteristics show a negative V_T shift as the temperature is lowered, which is expected for switching based on thermionic emission of holes over the channel barrier. The minimal temperature dependence of the contact-limited on current further suggests that transport at the contacts is governed by tunnelling.

Conclusions

We have reported a device platform for achieving clean, stable and damage-free contacts to 2D semiconductors and nearly ideal transistor characteristics using transferred via contacts made from metal-embedded h-BN. With TVCs, metal is dry-transferred onto the 2D semiconductor, which prevents direct-metallization-induced damage and simultaneously provides encapsulation to protect the device. TVCs also allow full glovebox processing, which leads to clean and stable devices as verified by I–V characterization and TEM measurements. We used the approach to create high-quality back-gated bilayer WSe_2 p-FETs with low contact resistance at both room temperature and low temperature. Through temperature-dependent measurements, we have shown that transport at the contacts is due to carrier tunnelling as opposed to thermionic emission over a Schottky barrier. Finally, we demonstrated that the approach can be used to fabricate double-gated devices with a high on current and a nearly ideal subthreshold swing of 64 mV per decade at 290 K using the high-quality top h-BN as a local top gate. Our TVCs provide an effective, reliable process for the development of high-performance 2D devices.

Methods

Fabrication of TVCs. h-BN flakes were mechanically exfoliated onto SiO_2/Si substrates outside the glovebox. Flakes of the desired thickness (20 to 30 nm) and

length (15–40 μm) were identified with an optical microscope. Electron-beam lithography was used to define patterns for metal contacts on PMMA resist spin coated over the flakes followed by etching of h-BN in the exposed areas using an Oxford Plasma Pro 100 Cobra reactive-ion-etch (RIE) system with 30/10 s.c.c.m. flow of SF_6/O_2 gas at 20 W power for 1 min. Electron-beam metal evaporation was used to deposit 20 nm of Pt followed by 30 nm of Au to fill the etched regions in the h-BN. After liftoff of the metal from unwanted regions with acetone, the TVCs were moved into the glovebox for transfer onto the device.

Stacking and fabrication of double-gated FETs. Exfoliation and stacking of WSe_2 was performed inside the glovebox in a nitrogen environment to minimize contamination of the 2D surface. The H_2O and O_2 levels inside the glovebox were always maintained under 0.5 ppm and 3 ppm, respectively. WSe_2 (acquired from HQ Graphene) was exfoliated onto SiO_2/Si substrates. TVCs were picked up with a PDMS stamp coated with polypropylene carbonate (PPC) polymer at ~50 °C in the glovebox. TVCs on the polymer stamp were then used to pick up the WSe_2 flakes and transfer them onto the bottom h-BN flakes exfoliated on a separate SiO_2/Si chip. Once the TVC and WSe_2 stack had been transferred onto the bottom h-BN, the PPC on top of the stack was melted at ~120 °C and washed off with acetone. Large metal electrodes and pads for electrical measurements were fabricated using conventional electron-beam lithography followed by electron-beam metal deposition of Ti/Au (5/85 nm). For the double-gated device, the top gate was added as a post-process to a back-gated device. Electron-beam lithography followed by electron-beam metal deposition of Pd/Au (20/30 nm) was used to form the top-gate contact in between the source and drain contacts.

Material characterization and electrical measurements. The number of WSe_2 layers was confirmed after device fabrication using Raman and photoluminescence spectra measurements, as shown in Supplementary Fig. 1 (Renishaw system, 532 nm laser). The electrical measurements were conducted with a semiconductor parameter analyser (Keysight B1500A) in both a vacuum probe station and a vacuum cryostat with an adjustable magnetic field and temperature ranging from 14 K to room temperature. The Hall voltages for extraction of carrier density were measured with a lock-in amplifier connected to the cryostat.

Four-probe resistance extraction. The width-normalized total resistance, channel resistance and contact resistance are plotted in Fig. 3c. These quantities were calculated from four-probe measurements using the following expressions:

$$R_{\text{total}} = \left(\frac{V_{14}}{I_{\text{D}}}\right) W \tag{1}$$

$$R_{\text{ch}} = \left(\frac{V_{23}}{I_{\text{D}}}\right)\left(\frac{L_{14}}{L_{23}}\right) W \tag{2}$$

and

$$2R_{\text{c}} = R_{\text{total}} - R_{\text{ch}} \tag{3}$$

Here, V_{ij} is the potential difference between contacts i and j, L_{14} and L_{23} are the effective channel lengths between contacts 1 and 4 and contacts 2 and 3 (equal to 6 and 2 μm, respectively) and W is the width of the contacts (6 μm). The expression for equation (3) is only valid for low $|V_{\text{DS}}|$. At high $|V_{\text{DS}}|$, one of the Schottky contacts becomes forward-biased and $R_{\text{total}} - R_{\text{ch}}$ is approximately equal to R_{c}, not $2R_{\text{c}}$. In our measurement, we use a small V_{DS} so that the use of equation (3) is valid.

Hole mobility and sheet density extraction. To calculate the hole sheet density ($p_{2\text{D}}$) and field-effect mobility (μ_{FE}) we extracted the transconductance ($g_{\text{m}} = \partial I_{\text{D}}/\partial V_{\text{BG}}$) from the transfer curves in strong accumulation at $V_{\text{BG}} = -80$ V, as shown by the dashed lines in Fig. 4d. To avoid noise caused by numerical differentiation of the measurement data, we found g_{m} by calculating the slope of I_{D} from $V_{\text{BG}} = -90$ to -70 V.

Starting with the expression for the drain current of a p-MOSFET in the linear regime

$$I_{\text{D}} = -\frac{W}{L}\mu_{\text{FE}} C_{\text{ox}}(V_{\text{BG}} - V_{\text{T}})V_{\text{DS}} \tag{4}$$

we find that the transconductance is

$$g_{\text{m}} = \frac{\partial I_{\text{D}}}{\partial V_{\text{BG}}} = -\frac{W}{L}\mu_{\text{FE}} C_{\text{ox}} V_{\text{DS}} \tag{5}$$

The hole field-effect mobility is equal to

$$\mu_{\text{FE}} = -\frac{L}{WC_{\text{ox}}V_{\text{DS}}} g_{\text{m}} \tag{6}$$

and the hole sheet density is equal to

$$p_{2\text{D}} = -\frac{1}{q}C_{\text{ox}}(V_{\text{BG}} - V_{\text{T}}) = -\frac{1}{q}C_{\text{ox}}\frac{I_{\text{D}}}{g_{\text{m}}} \tag{7}$$

For the values extracted in this Article we use $C_{\text{ox}} = 1.1 \times 10^{-8}$ F cm^{-2}, which is equivalent to a combined dielectric of 285 nm of SiO_2 and 30 nm of h-BN with a relative permittivity of 4.

The great linear fits to the transfer characteristics, as presented in Fig. 4d, show that the transconductance is nearly constant over the range of $V_{\text{BG}} = -100$ to -65 V. From equation (6), the constant transconductance suggests that μ_{FE} is also nearly constant over this range, which makes the use of an average g_{m} appropriate.

We can recast equation (6) in terms of two-probe (2p) and four-probe (4p) mobilities using the variable definitions from four-probe resistance extraction:

$$\mu_{\text{FE,2p}} = -\frac{L_{14}}{WC_{\text{ox}}V_{14}} g_{\text{m}} \tag{8}$$

$$\mu_{\text{FE,4p}} = -\frac{L_{23}}{WC_{\text{ox}}V_{23}} g_{\text{m}} \tag{9}$$

Data availability

The data that support the findings within this paper are available from the corresponding authors on reasonable request.

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Author contributions

Y.J., M.S.C., J.H. and J.T.T. conceived the research and designed the experiments. Y.J. and M.S.C. fabricated and measured the devices under J.T.T.'s supervision. A.N. and A.B. contributed to the data analysis and manuscript revision. B.K. contributed to the Hall measurements. A.Z. performed TEM measurements. T.T. and K.W. contributed h-BN material. W.J.Y., J.H. and J.T.T. contributed to discussions of the results. Y.J., M.S.C. and J.T.T. wrote the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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