

Switching On/Off Negative Capacitance in Ultrathin Ferroelectric/Dielectric Capacitors

Jagaran Acharya,* Ryan Goul, Jamie Wilt, and Judy Wu*

Cite This: *ACS Appl. Mater. Interfaces* 2020, 12, 9902–9908

Read Online

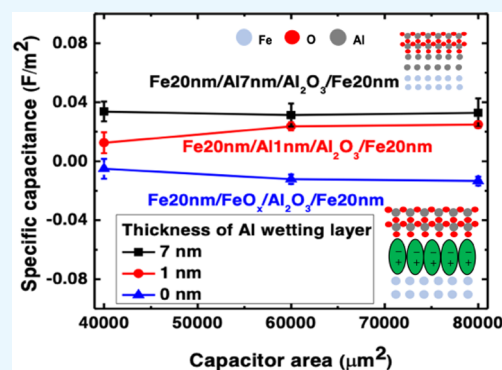
ACCESS |

Metrics & More

Article Recommendations

ABSTRACT: Ferroelectric (FE) and dielectric (DE) insulator bilayer stacks provide a promising gate for low-power microelectronic devices. To fully realize the FE polarization switching, the DE layer must be ultrathin in the FE/DE bilayer stack. Motivated by this, this work presents the first successful fabrication and characterization of Fe/FeO_x/Al₂O₃/Fe FE/DE bilayer capacitors using in vacuo atomic layer deposition (ALD) with a total FE/DE stack thickness <3–4 nm. A key tuning parameter in generating the FE/DE bilayer capacitors is the thickness of an Al wetting layer between the bottom Fe electrode and the ALD-Al₂O₃ DE layer. At a large thickness in exceeding 1.0 nm, high-quality conventional DE capacitors of 2.2 nm thick ALD-Al₂O₃ were obtained with dielectric constant (ϵ_r) $\sim$ 8.0 that is close to $\epsilon_r \sim$ 9.2 for the Al₂O₃ bulk single crystal with an effective oxide thickness of 1.0 nm. By reducing the Al wetting layer thickness to below 1.0 nm, a thin ferroelectric FeO_x interfacial layer of a thickness of 1–2 nm forms, enabling the achievement of a FeO_x/Al₂O₃ FE/DE bilayer capacitor with static negative capacitance. Since all ferroelectric materials are piezoelectric, we show that a dynamic switching on/off of the negative capacitance can be achieved under the application of an external force on the ultrathin FE/DE capacitors through manipulation of the electric dipoles. This result not only provides a viable approach for generating ultrathin FE/DE bilayer capacitors but also offers a promising solution to low-power consumption microelectronics.

KEYWORDS: atomic layer deposition, ultrathin film, ferroelectric interface, negative capacitance, interface, polarization switching



INTRODUCTION

Following empirical Moore's law, miniaturization of microelectronic devices has been the main driving force for advancement in the semiconductor industry and justifies an increasing demand for more densely integrated devices.^{1–4} One of the direct consequences of this demand is the need for a continuous reduction of the gate dielectric thickness. Unfortunately, for SiO₂ gates approaching the ultrathin thickness range of 2–4 nm, considerably increased leakage current density (J) up to 1–10 A/cm² occurs primarily due to the difficulties in controlling the defects in ultrathin SiO₂.⁵ This not only prevents the achievement of the required gate voltages for device operation but also exceeds the required threshold of $\sim 10^{-3}$ A/cm² for high-performance, low-power consumption microprocessors by several orders of magnitude.^{5–9} The difficulties in down-scaling the SiO₂ dielectric gates have motivated intensive research on high- K dielectric materials.^{10,11} With considerably higher dielectric constants (ϵ_{HfK}) than that of SiO₂ ($\epsilon_r \sim 3.9$), the high- K dielectric can achieve an effective oxide thickness (EOT = $t_{\text{HfK}} \times 3.9/\epsilon_{\text{HfK}}$) in the range ~ 1 –2 nm, with a larger thickness t_{HfK} to reduce J .^{12–14} For example, to achieve an equivalent SiO₂ dielectric of thickness $t_{\text{SiO}_2} \sim 1.5$ nm with the specific capacitance given as

($C_0 = C/A = \epsilon_0 \times 3.9/t_{\text{SiO}_2}$), the corresponding thickness of high- K material HfO₂ with $\epsilon_{\text{HfK}} \sim 20$ is ~ 7.7 nm for the same value of C_0 , which results in the lower $J \sim 10^{-5}$ A/cm².⁸ This allows the achievement of standby low-power ~ 1 μ W at an applied voltage of 1 V.⁸ Recent research explores the extensive use of Al₂O₃ dielectric in interface engineering for obtaining high-quality and thermodynamically stable Hf-based high- K dielectric leading to the suppression of interfacial capacitance with reduced defects and trap densities for their application in CMOS technology.^{15–19} Despite the progress made in ultrathin high- K gate dielectrics of a few nm in thickness, further reduction in their thickness remains challenging due to the difficulties in controlling defects, which is similar to the SiO₂ dielectric case.^{12,14}

A promising resolution to this issue is to stack a ferroelectric (FE) layer with the dielectric (DE) layer to make a FE/DE bilayer stack.^{20–28} FE materials can have significantly higher ϵ_r

Received: November 1, 2019

Accepted: February 5, 2020

Published: February 5, 2020

values by a few orders of magnitude than that of SiO_2 or many other DE materials.^{29–31} Using a FE gate only remains difficult due to the hysteretic current–voltage characteristics and unstable negative capacitance as shown in the $\text{FeHf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ (HZO).¹⁹ These issues could be minimized in the FE/DE bilayer stacks on which the polarization switching at a low applied voltage leads to an efficient control of gate switching on/off and hence low-power operation taking advantage of the negative capacitance in the FE layer.^{20–28} In a recent study, HZO/ Al_2O_3 FE/DE bilayers with a fixed FE layer thickness of 20 nm, Si et al. discovered that the DE layer thickness must be ≤ 4 nm to observe FE polarization switching.³² When the DE thickness exceeds 4 nm, they observed that the HZO/ Al_2O_3 FE/DE stack behaves like a regular DE layer with no polarization switching and transient negative capacitance.³² This observation has revealed the importance of the FE/DE interface on controlling the polarization switching in the PE layer through a balance of the gate voltages across the FE and DE layers in the FE/DE bilayer stack.^{32,33} Another related study on FE PbTiO_3 nanodot capacitors with their radii of 2, 5, and 10 nm.³⁴ An interesting correlation between the nanodot radius and the thickness was revealed from the observation of the static negative capacitance when the nanodots have comparable lateral and vertical dimensions.³⁴

In this work, we report a novel approach for the fabrication of ultrathin $\text{FeO}_x/\text{Al}_2\text{O}_3$ FE/DE bilayer capacitors with the total FE/DE stack thickness in the range 3–4 nm using an in vacuo atomic layer deposition (ALD) in combination with magnetron sputtering. FeO_x thin films exhibit a ferroelectric behavior at room temperature.^{35,36} The FE properties of the FeO_x have been investigated for potential future technological applications such as fast-writing, power-saving, and non-destructive data storage.^{36–38} On the other hand, high-quality, ultrathin dielectric ALD- Al_2O_3 of thickness as low as ~ 2.2 nm has been demonstrated recently in $\text{Al}/\text{ALD-}\text{Al}_2\text{O}_3/\text{Al}$ capacitors with high $\epsilon_r \sim 8.0$ that is close to the Al_2O_3 bulk crystal value of $\epsilon_r \sim 9.2$.³⁹ Using an Al wetting layer in the $\text{Fe}/\text{Al}/\text{ALD-}\text{Al}_2\text{O}_3$ (2.2 nm)/Fe capacitors, we show a transition from a DE only capacitor at Al thickness in exceeding 1.0 nm to an FE/DE bilayer capacitor at smaller Al thickness to promote the formation of ultrathin FeO_x of a thickness below 2 nm at the Fe and ALD- Al_2O_3 interface. This allows the observation of a transition from positive capacitance on DE only capacitors to negative capacitance on FE/DE bilayer capacitors. Furthermore, we show that switching on/off of the negative capacitance can be achieved using the piezoelectric effect of the FE layer in the ultrathin FE/DE bilayer capacitors via application of external mechanical deformation.

EXPERIMENTAL SECTION

The fabrication of the ultrathin capacitors was carried out in vacuo using a home-built integrated ultrahigh vacuum sputtering–ALD system.⁴⁰ Direct current (DC) magnetron sputtering was used to deposit all metal layers including Nb, Fe, and Al. The deposition rates for the Nb, Fe, and Al were 1.7, 1.1, and 0.5 nm/s, respectively. The bottom electrode of the ultrathin capacitors consists of a stack of Al (7–0 nm)/Fe (20 nm)/Nb (50 nm). On each sample, three bottom electrodes were defined using a shadow mask for an array of three capacitors on a Si/SiO_2 substrate. After the bottom electrode deposition, the sample was in vacuo transferred to the ALD chamber for the growth of 20 cycles ALD- Al_2O_3 . The thickness of the ALD Al_2O_3 film per ALD cycle was calibrated using ellipsometry to be 1.1–1.2 Å/cycle,^{40,41} which is consistent with the previous reports by other

groups.^{42–44} It should be noted that the thickness of the 20 cycles ALD- Al_2O_3 is in the range of 2.2–2.4 nm based on the growth rate of 1.1–1.2 Å/cycle.⁴¹ This is the smallest dielectric thickness for $\text{Al}/\text{ALD-}\text{Al}_2\text{O}_3/\text{Al}$ ultrathin capacitors architecture with negligible electron tunneling, which seems consistent to the observed high $\epsilon_r \sim 8.0$ that is close to the Al_2O_3 bulk crystal value of $\epsilon_r \sim 9.2$.³⁹ The ALD growth temperature was maintained at 200–220 °C, and an optimal heating time of 15 min was employed to prevent the formation of a defective metal/insulator interfacial layer (IL).^{39,45} The growth of ALD- Al_2O_3 films was carried out by sequential exposure of the sample surface to relevant precursor pulses via ligand exchange.⁴⁶ For ALD- Al_2O_3 , trimethylaluminum (TMA, Sigma-Aldrich) and H_2O (Ultima grade, Fischer Scientific) were selected as the precursors for Al and O, respectively. The precursor sources were maintained at room temperature during the ALD- Al_2O_3 growth. The precursor pulse durations and heights were 1 s and 700 mTorr for the TMA and 2 s and 850 mTorr for H_2O pulses, respectively. Each precursor pulse was followed with a purge of N_2 gas (5 sccm) for 35 s to prevent unwanted precursor reactions in the ALD chamber.⁴² To obtain capacitors, the top electrode consisting of a stack of Fe (20 nm)/Nb (25 nm) in thickness was sputtered after the growth of the ALD- Al_2O_3 through another shadow mask to define the three capacitors of the lateral dimensions of 200×200 , 200×300 , and $200 \times 400 \mu\text{m}^2$, respectively, on the same sample. Capacitance–voltage (C–V) and the leakage current vs voltage (I–V) measurements were carried out on the capacitors using tungsten probes (25 μm in diameter, Lakeshore) in a probe station and an Agilent B1500A semiconductor analyzer.³⁹ The cyclic voltammetry I–V measurements were carried out using a potentiostat (model 660 B, CH Instruments Inc.) with a maximum potential range of up to 10 mV (corresponding to an electric field ~ 5 MV/m) to avoid dielectric breakdown.⁴⁷ Three thicknesses of the Al wetting layer were selected at 7, 1, and 0 nm to systematically control the capacitors from DE only on the 7 nm Al wetting layer, to the DE/FE bilayer on the 1 or 0 nm Al wetting layer. In situ scanning tunneling spectra (STS) were taken on the half-cell M (bottom electrode)/I samples with the three different Al wetting layers, while the “I” layer regards a total five cycles of ALD- Al_2O_3 .^{28,29,32} STS I–V and dI/dV spectra were collected simultaneously using a lock-in amplifier with a voltage modulation of 30 mV at 5 kHz, with a set-point bias of 2.0 V and current ~ 200 pA to assure the STS tip would not crash. The conduction band maxima, denoted as tunnel barrier height (E_b), were estimated by the intersection of two bisquare-method linear fits to $\ln(dI/dV)$ similar to the method previously reported.⁴⁸ One line fits the band gap regime, and the other fits the conduction band since in the log scale, these two regions are roughly linear. This $\ln(dI/dV)$ linear fit method was chosen over I–V or $(dI/dV)/(I/V)$ fit methods for its insensitivity to high noise in the STS spectra.^{49,50}

RESULTS AND DISCUSSION

Figure 1a,b illustrates the schematic of the ultrathin capacitors of the Nb (25 nm)/Fe (20 nm)/ALD- Al_2O_3 (2.2 nm)/Al (7 or 0 nm)/Fe (20 nm)/Nb (50 nm) structure with and without a 7 nm thick Al wetting layer, respectively. With the 7 nm thick Al wetting layer, the bottom Fe electrode is protected from oxidation⁴¹ and the interface between $\text{Al}/\text{Al}_2\text{O}_3$ has been found to have a negligible AlO_x interface at the optimal ALD growth condition, as illustrated schematically in Figure 1c.^{45,46} When the Al wetting layer is removed, reduced E_b for ALD- Al_2O_3 was observed, suggesting that an IL may form at the Fe/ Al_2O_3 interface, most probably through the formation of FeO_x , as shown in Figure 1d.⁵¹ Comparing to Al, Fe is a stronger oxygen getter, which means that FeO_x is more likely to form than AlO_x at a given dielectric growth condition. The Al wetting layer of thickness in exceeding 1.0 nm seems adequate to prevent oxidation of Fe as illustrated with comparable to the optimal $E_b \sim 1.55$ – 1.66 eV of the ALD- Al_2O_3 .⁵¹ At smaller Al

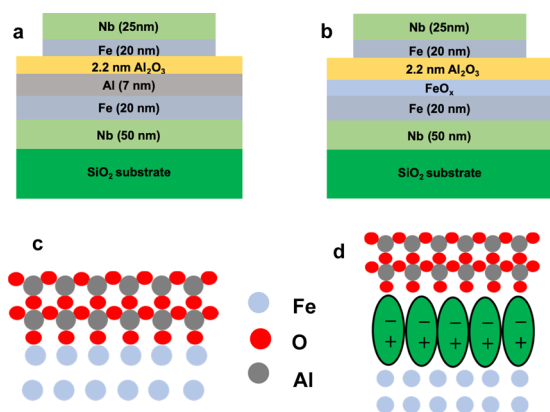


Figure 1. Schematic of the ultrathin capacitors with: (a) a thick 7 nm Al wetting layer; and (b) no Al wetting layer forming the FeO_x interfacial layer. The schematic description of the M-I interface for (c) ALD-Al₂O₃/Al (7 nm) with pure dielectric ALD-Al₂O₃ and (d) Al₂O₃/Fe with a ferroelectric FeO_x interface in series with the ALD-Al₂O₃ dielectric layer forming FeO_x/Al₂O₃/Fe bilayer Fe/DE capacitors.

wetting layer thicknesses, the E_b shows monotonic decrease to 1.40 eV at ~ 1 nm thick Al wetting layer on Fe and 1.30 eV when the Al wetting layer is completely removed. This trend can be attributed to the formation of a native FeO_x oxide IL at the Fe/ALD-Al₂O₃ interface when the Al wetting layer is very thin or absent.⁴⁶ This means, instead of forming a simple Al/Al₂O₃/Al DE capacitor (Figure 1c), an FE FeO_x capacitor is added to the Fe/FeO_x/ALD-Al₂O₃/Fe capacitors that can be viewed as two capacitors in series: a ultrathin FE FeO_x capacitor and a 2.2 nm thick DE ALD-Al₂O₃ capacitor, as depicted in Figure 1b,d. It should be noted that the small thicknesses of both FE and DE layers are critical to the observation of the negative capacitance in the obtained FeO_x/ALD-Al₂O₃ FE/DE bilayer capacitors.^{32,34,52}

Figure 2a shows a comparison of the specific capacitance ($C_0 = C/A = \epsilon_0 \epsilon_r / t$, where t is the thickness of the dielectric) for the three sets of the ultrathin capacitors of Nb (25 nm)/Fe (20 nm)/ALD-Al₂O₃ (2.2 nm)/Al (7, 1 or 0 nm)/Fe (20 nm)/Nb (50 nm). Each set has three devices with junction areas of 200×200 , 200×300 , and $200 \times 400 \mu\text{m}^2$, respectively, for examination of the sample uniformity. The three samples would be otherwise identical except they have different Al

wetting layer thicknesses of 7 nm (black), 1 nm (red), and zero (blue). As shown in Figure 2b, with a 7 nm thick Al wetting layer, the value of C_0 is around $0.032\text{--}0.040 \text{ F/m}^2$ on chip with uniformity of $\sim 15\%$. This is an indication of negligible IL formation at the Al/ALD-Al₂O₃ interface. However, with the reduction in the Al wetting layer thickness to 1 nm, the value of C_0 decreases considerably to $0.021\text{--}0.016 \text{ F/m}^2$ on chip with variation $\sim 23.8\%$. Interestingly, with the complete removal of the Al wetting layer, C_0 becomes negative in the range of -0.005 to -0.015 F/m^2 . Figure 2c shows dielectric constant (ϵ_r) derived from $\epsilon_r = C_0 t / \epsilon_0$. Two considerations were taken in selecting the ALD Al₂O₃ DE layer thickness of 2.2 nm in the FE/DE bilayer capacitors. One is based on the recent works with the DE layer being as thin as possible, in the range of a few nm, is critical to the observation of negative capacitance.^{32,34,52} The other is based on our recent study on the thickness dependence of the dielectric properties of the ALD Al₂O₃ in Al/ALD-Al₂O₃ (4.4–1.1 nm)/Al capacitors.³⁹ We have found that the ALD-Al₂O₃ thickness in the range of 2.2–4.4 nm can effectively prevent electron tunneling as illustrated in the dielectric constant (ϵ_r) $\sim 8.0\text{--}9.0$ that is close to that of the bulk single-crystal Al₂O₃ in the thickness range of 2.2–4.4 nm. In fact, an ALD-Al₂O₃ of 2.2 nm thickness has an EOT $\sim 1.0 \text{ nm}$,³⁹ which is comparable to the EOT $\sim 0.9 \text{ nm}$ for a 4.5 nm high- K HfO₂ film.⁵³

It should be noted that the observation of smaller and even negative ϵ_r on capacitors with 1 or 0 nm Al wetting layer cannot be attributed to the poorer quality of the ALD-Al₂O₃ DE layer at the thinner Al wetting layer based on our earlier investigation of the ALD-Al₂O₃ tunnel barriers (thickness from 0.1 to 1.0 nm) on the Fe electrodes, which showed $E_b \sim 1.3 \text{ eV}$ and ALD-Al₂O₃ coverage comparable to samples with an Al wetting layer.³⁷ In other words, leak-free ALD-Al₂O₃ tunnel barriers can form on an Fe electrode even without the Al wetting layer.³⁷ However, the slightly lower $E_b \sim 1.3 \text{ eV}$, as compared to the optimal value of $E_b \sim 1.5\text{--}1.6 \text{ eV}$ measured on ALD-Al₂O₃ tunnel barriers on Al electrodes, suggests that a minor IL, most probably FeO_x due to the subtle effect of the surface structure of Fe on the hydroxylation during the first H₂O pulse, forms at the Fe/ALD-Al₂O₃ interface.^{45,46,51} While in many other devices, the native oxide IL is unfavorable, the ferroelectric FeO_x IL formed at the Fe/ALD-Al₂O₃ interface^{45,46,51} provides an excellent opportunity to achieve ultrathin FE/DE bilayer capacitors connected in series of a

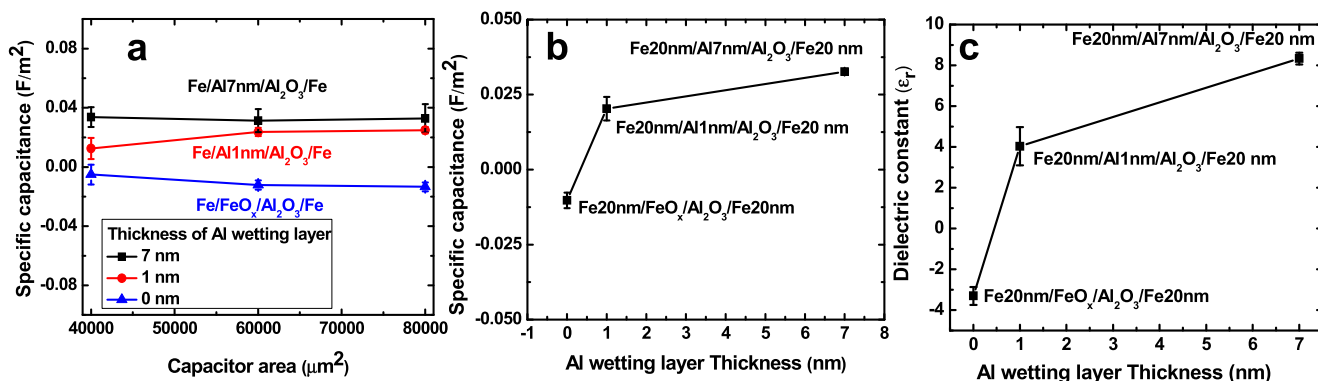


Figure 2. Variation of (a) specific capacitance with three different junction areas 200×200 , 200×300 , and $200 \times 400 \mu\text{m}^2$ for 2.2 nm ALD Al₂O₃ showing the dependence of capacitance on the Al wetting layer thickness range 0–7 nm, (b) specific capacitance with the thick 7 nm Al wetting layer, thin 1 nm Al wetting layer, and without the Al wetting layer, and (c) calculated dielectric constant (ϵ_r) for ultrathin capacitor for 2.2 nm ALD-Al₂O₃.

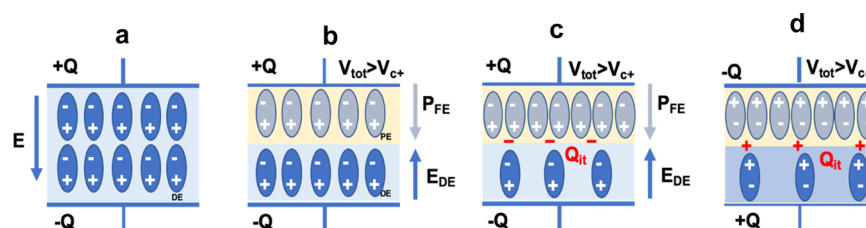


Figure 3. Working principle of (a) Fe/Al/FeO_x/Al₂O₃/Fe dielectric (DE) capacitor under application of an external electric field, i.e., blue ovals represent electrical dipoles aligned under the E field, (b) Fe/Al/FeO_x/Al₂O₃/Fe ferroelectric/dielectric (FE/DE) bilayer capacitor with blue and light blue ovals represent electrical dipoles and polarization aligned under E field at $V_{\text{tot}} > V_{\text{c}+}$ before switching. (c) Increase in FE capacitance due to external E field or via external deformation leading to an increase in interfacial charges at the FE/DE interface at $V_{\text{tot}} > V_{\text{c}+}$. (d) Leakage current-assisted polarization switching with a change in interfacial charges in FE/DE bilayer capacitors $V_{\text{tot}} > V_{\text{c}-}$ after switching.

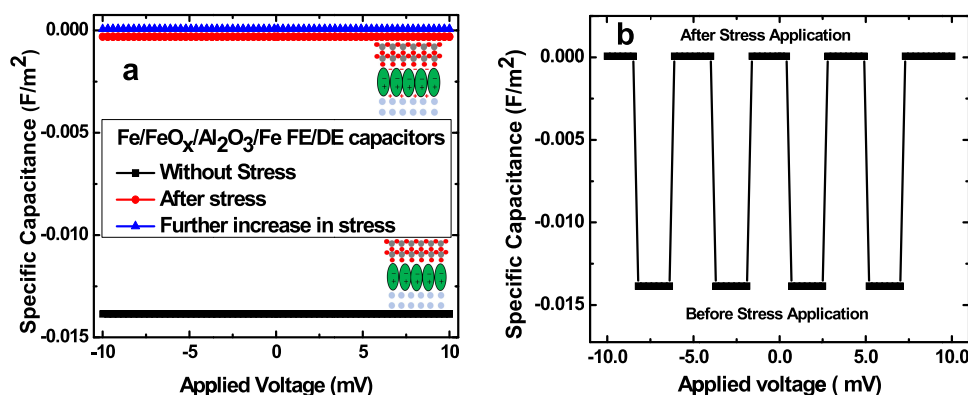


Figure 4. (a) Comparison of the C - V curve for the ultrathin capacitor without the Al wetting layer as measured and under the application of the external force showing a change in capacitance and (b) dynamic response curve for the ultrathin capacitor before and after application of the external force.

total thickness smaller than 3–4 nm, allowing direct observation of the static negative capacitance.^{32,34,52} This means that the measured C_0 and ϵ_r on these ultrathin FE/DE bilayer capacitors must be considered as the combined effect of the constituent FE and DE capacitors as we shall discuss in the following.

Figure 3a illustrates the working principle of the ultrathin Fe/Al/ALD-Al₂O₃/Fe pure DE capacitors under the application of an external electric field (E). The blue ovals represent electrical dipoles aligned in response to the external E field. Figure 3b shows the electrical dipoles in the Fe/FeO_x/ALD-Al₂O₃/Fe FE/DE bilayer capacitors with coercive voltage (V_c) of a few mV for polarization switching in the FE material much smaller than total external applied external voltage (V_{tot}). At this ultrathin 2.2 nm thick ALD-Al₂O₃ with ultrathin FE FeO_x, the presence of stable negative capacitance is possibly due to formation of regular, nanoscale stable domains with the same orientation of the electric polarization that makes the FE layers extremely polarizable as shown as P_{FE} under the application of E across the FE/DE stack. For ultrathin FE/DE capacitors, the interfacial effects are more pronounced. Thus, FE/DE stack capacitor fundamentally differs from just only the series combination of ferroelectric capacitance (C_{FE}) and dielectric capacitance ($C_{\text{Al}_2\text{O}_3}$).^{54,55} Considering pure dielectric as in the case of Al/Al₂O₃/Al ultrathin capacitors, the stored charges in DE are $Q_{\text{Al}_2\text{O}_3}$. However, the FE layer shows polarization under external applied field with $Q_{\text{FE}} = Q_{\text{p}} + Q_{\text{i}}$, where Q_{p} and Q_{i} corresponds to the polarized charges in FE material and induced or interfacial trapped charges respectively. For a simple approximation, the Fe/FeO_x/ALD-Al₂O₃/Fe ultrathin capacitors can be considered as the two capacitors in series:

DE ALD-Al₂O₃ capacitor and FE FeO_x capacitor, which can be estimated using $\frac{1}{C_{\text{T}}} = \frac{1}{C_{\text{Al}_2\text{O}_3}} + \frac{1}{C_{\text{FE}}}$, where C_{T} is the total capacitance of the FE/DE stack. With observed values of $C_{\text{Al}_2\text{O}_3} \sim 0.04 \text{ F/m}^2$ and $C_{\text{T}} \sim -0.015 \text{ F/m}^2$, the C_{FE} is estimated to be $\sim -0.010 \text{ F/m}^2$, which is one-fourth of C_{FE} but with opposite polarization. Thus, the thickness of FE (t_{FE}) is approximated from equation $t_{\text{FE}} = \epsilon_0 \epsilon_r / C_0 \sim 0.88\text{--}1.77 \text{ nm}$ corresponding to $\epsilon_{\text{r,FE}} \sim -1$ to -2 . This indicates that the total thickness of the FE/DE stack varies from 3–4 nm, which is ultrathin as compared to previous studies.^{32,52} However, at this ultrathin DE thickness of $\sim 2.2 \text{ nm}$ in the presence of a FE layer in the FE/DE bilayer stack, there is the possibility of leakage current due to the trapped charges at the FE/DE interface. Figure 3c shows the increase in the polarization of FE under the application of an external electric field or via external mechanical deformation in the FE/DE bilayer capacitors. The induced charge at the FE/DE interface Q_{i} adds to Q_{p} that increases the total polarization charges of Q_{FE} . The increase in the polarization of the FE material corresponds with the decrease in DE contribution resulting in stable negative capacitance. Figure 3d shows leakage current-assisted polarization switching behavior in FE/DE capacitors with the polarization switching effect, which is in agreement with previous studies on a HZO/Al₂O₃ FE/DE structure.^{32,52} The DE material thickness has the determinant impact on the FE polarization switching effect, at DE thickness $> 4 \text{ nm}$, HZO/Al₂O₃ stacks behaves like pure DE insulators with no polarization switching of HZO.³² However, at the ultrathin DE thickness $< 4 \text{ nm}$, HZO/Al₂O₃ stacks exhibit a FE effect

with stable and switchable electrical polarization resulting in negative capacitance.³²

Since all ferroelectric materials are piezoelectric, the response of FE/DE stacks with FE FeO_x would provide an interesting application for memory and sensor device applications through manipulation of electric dipoles.⁵⁶ Figure 4 shows the variation of specific capacitance with and without external deformation on a FE/DE stack. Before external deformation, total capacitance is dominated by a series combination of FE and DE capacitors resulting in total negative capacitance (black), as shown in Figure 4a. However, after the application of external force in FE/DE capacitors, the contribution from DE remains the same but there is an increase in the FE capacitance due to a piezoelectric effect showing an increase in polarized charges at the FE/DE interface, which corresponds to the reduction in total negative capacitance (red) for FE/DE stack. The further increase in the external force makes the total capacitance a small positive value (blue). Quantitatively, this shows that changes in capacitance under external deformation are the manifestation of the change in polarization switching behavior in ultrathin FE/DE capacitors. Figure 4b shows the dynamic reproducible polarization switching on/off of negative capacitance corresponding to before/after the external deformation in FE/DE ultrathin capacitors. This indicates that the capacitance can be tuned with external force, which would find potential applications in nonvolatile memory and piezoelectric force sensor applications through the manipulation of the electric dipoles in FE/DE ultrathin capacitors.

To validate the presence of the FeO_x IL in ultrathin FE/DE capacitors, Figure 5 shows the dependence of E_b on the Al

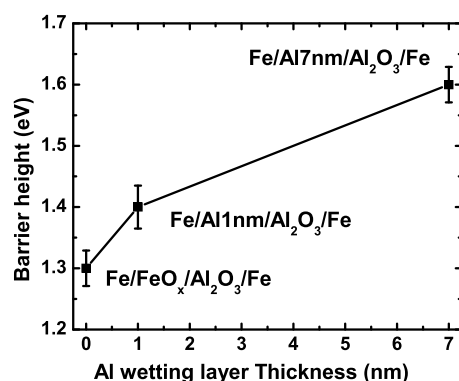


Figure 5. STS measured tunnel barrier heights for ultrathin dielectric half-cells made for three different configurations with different thickness of the Al wetting layer of 7, 1, and 0 nm.

wetting layer using the ALD- $\text{Al}_2\text{O}_3/\text{Al}$ (7, 1, or 0 nm)/Fe (20 nm)/Nb (50 nm) half-cell structure studied using STS. Our previous STS study suggests that compared to Al, Fe is a stronger oxygen getter, which means the oxidation of Fe forming FeO_x is more likely than AlO_x at a given ALD- Al_2O_3 growth condition.⁵¹ The Al wetting layer greater than 1 nm can result in negligible AlO_x and can prevent the oxidation of Fe with $E_b \sim 1.55\text{--}1.66$ eV for five cycles ALD- Al_2O_3 on Fe.⁵¹ However, with a 1 nm thick Al wetting layer, there is monotonic decrease in E_b to 1.40 and 1.30 eV when the Al wetting layer is completely removed. This trend can be attributed to the formation of a native FeO_x oxide interface layer at the Fe/ALD- Al_2O_3 interface when the Al wetting layer is very thin or absent.^{46,51} Specifically, the presence of FeO_x IL

affects the E_b of ALD- Al_2O_3 in a similar way to the native AlO_x case.⁴⁶ The dependence of E_b on the Al wetting layer thickness gives insight into the E_b for both pure Al/ Al_2O_3 /Al capacitors and the FE/DE bilayer Fe/ FeO_x /ALD- Al_2O_3 /Fe structure. However, the decreasing trend in E_b with the Al wetting layer thickness confirms our assumption of the formation of an IL FeO_x resulting in a FE/DE stack.

To extract further information about properties of ultrathin FE/DE capacitors, these were studied using I - V measurement. Figure 6 provides two important pieces of information: (1) a

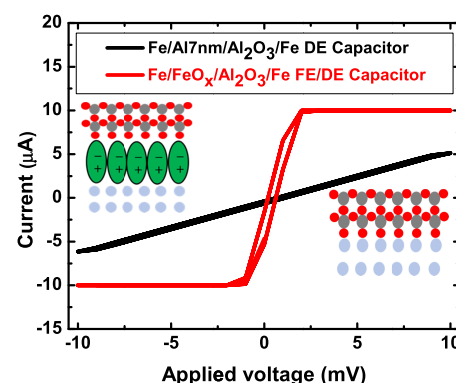


Figure 6. Comparison of I - V curves measured on the ultrathin Fe/ FeO_x /ALD- Al_2O_3 /Fe FE/DE capacitor (red) and the Fe/Al/ALD- Al_2O_3 /Fe DE capacitor (black).

hysteretic I - V loop for ultrathin FE/DE capacitors that shows strong evidence for the formation of FeO_x IL with ferroelectric polarization switching behavior at an ultralow applied voltage of a few mV and (2) linear I - V for 2.2 nm DE devices showing quantum tunneling behavior. This observation shows that a key tuning parameter in generating the FE/DE bilayer capacitors is the thickness of an Al wetting layer between the bottom Fe electrode and the ALD- Al_2O_3 DE layer. This work demonstrates the feasibility of the successful fabrication and characterization of Fe/ FeO_x /ALD- Al_2O_3 /Fe FE/DE ultrathin capacitors using an in vacuo ALD method. This observation of static negative capacitance with FE/DE ultrathin capacitors finds potential application for lowering the switching energy of transistors and improved power dissipation with the possibility for ultralow-power devices,^{20–24} piezoelectric sensors, and nonvolatile memory applications.^{36–38}

CONCLUSIONS

In summary, in vacuo ALD provides a unique approach to fabricate high-quality ultrathin capacitors and has been applied for the first time in this work to generate FE/DE bilayer capacitors with a total FE/DE thickness $<3\text{--}4$ nm. Specifically, the capacitors consist of a Nb (25 nm)/Fe (20 nm)/ALD- Al_2O_3 (2.2 nm)/Al(7, 1, or 0 nm)/Fe (20 nm)/Nb (50 nm) stack, and the Al wetting layer was employed as the tuning mechanism to obtain either DE only capacitors at the Al thickness >1 nm or FE/DE bilayer capacitors at thinner or no Al wetting layers. The obtained DE only capacitors exhibit high $\epsilon_r \sim 8.0$, which represents the best so far achieved on ultrathin capacitors of the DE thickness around 2 nm. In fact, this value is close to the Al_2O_3 bulk single-crystal value of $\epsilon_r \sim 9.2$. Interestingly, an ultrathin FeO_x FE layer can form on the surface of the Fe bottom electrode when the Al wetting layer is thinner or completely removed. This could be attributed to the

minor interaction of the first ALD H₂O pulse with the Fe surface through partial dissociations of the H₂O monolayer into atomic oxygen. The obtained FE/DE bilayer capacitors show a dynamic switching on/off of the negative capacitance that can be achieved under the application of an external force. This result not only provides a viable approach for generating ultrathin FE/DE bilayer capacitors but also offers a promising solution to low-power consumption microelectronics and piezoelectric sensors applications.

AUTHOR INFORMATION

Corresponding Authors

Jagaran Acharya – Department of Physics and Astronomy,
University of Kansas, Lawrence, Kansas 66045, United States;
orcid.org/0000-0003-1129-0974; Email: jagaran@ku.edu

Judy Wu – Department of Physics and Astronomy, University of
Kansas, Lawrence, Kansas 66045, United States; Email: jwu@
ku.edu

Authors

Ryan Goul – Department of Physics and Astronomy, University
of Kansas, Lawrence, Kansas 66045, United States

Jamie Wilt – Department of Physics and Astronomy, University
of Kansas, Lawrence, Kansas 66045, United States;
orcid.org/0000-0003-0913-2889

Complete contact information is available at:
<https://pubs.acs.org/10.1021/acsami.9b19789>

Author Contributions

J.A. and J.Z.W. designed the experiment. J.A. prepared the samples and performed the measurement and property characterization with most of the analysis. R.G. contributed with STS sample fabrication and measurement. All authors contributed to the discussion of results. J.A. and J.Z.W. led the effort in the development of the manuscript.

Funding

This research was supported in part by NSF contracts Nos. NSF-DMR-1508494, NSF-ECCS-1809293, and NSF-DMR-1909292 and ARO contract No. W911NF-16-1-0029.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

The authors acknowledge support in part by NSF contracts Nos. NSF-DMR-1508494, NSF-ECCS-1809293, and NSF-DMR-1909292 and ARO contract no. W911NF-16-1-0029.

REFERENCES

- (1) Theis, T. N.; Solomon, P. M. It's Time to Reinvent the Transistor! *Science* **2010**, 327, 1600–1601.
- (2) Aitken, R.; Chandra, V.; Myers, J.; Sandhu, B.; Shifren, L.; Yeric, G. In *In Device and Technology Implications of the Internet of Things*, Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers; IEEE, 2014; pp 1–4.
- (3) Fuketa, H.; Yasufuku, T.; Iida, S.; Takamiya, M.; Nomura, M.; Shinohara, H.; Sakurai, T. In *Device-Circuit Interactions in Extremely Low Voltage Cmos Designs*, International Electron Devices Meeting; IEEE, 2011; pp 25.21. 21–25.21. 24.
- (4) Fuketa, H.; Iida, S.; Yasufuku, T.; Takamiya, M.; Nomura, M.; Shinohara, H.; Sakurai, T. In *A Closed-Form Expression for Estimating Minimum Operating Voltage (V_{Dmin}) of Cmos Logic Gates*, Proceedings of the 48th Design Automation Conference; ACM, 2011; pp 984–989.
- (5) Green, M. L.; Gusev, E. P.; Degraeve, R.; Garfunkel, E. L. Ultrathin (<4 nm) SiO₂ and Si–O–N Gate Dielectric Layers for Silicon Microelectronics: Understanding the Processing, Structure, and Physical and Electrical Limits. *J. Appl. Phys.* **2001**, 90, 2057–2121.
- (6) Schulz, M. The End of the Road for Silicon? *Nature* **1999**, 399, 729–730.
- (7) Packan, P. A. Pushing the Limits. *Science* **1999**, 285, 2079.
- (8) Gargini, P. In *The International Technology Roadmap for Semiconductors (Itrs): "Past, Present and Future"*, GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuits Symposium. 22nd Annual Technical Digest 2000. (Cat. No.00CH37084), Nov 5–8, 2000; pp 3–5.
- (9) Lee, B. H.; Song, S. C.; Choi, R.; Kirsch, P. Metal Electrode/High- κ Dielectric Gate-Stack Technology for Power Management. *IEEE Trans. Electron Devices* **2008**, 55, 8–20.
- (10) Wallace, R. M.; Wilk, G. D. High- κ Dielectric Materials for Microelectronics. *Crit. Rev. Solid State Mater. Sci.* **2003**, 28, 231–285.
- (11) Auth, C.; Cappellani, A.; Chun, J.; Dalis, A.; Davis, A.; Ghani, T.; Glass, G.; Glassman, T.; Harper, M.; Hattendorf, M.; Hentges, P.; Jaloviar, S.; Joshi, S.; Klaus, J.; Kuhn, K.; Lavric, D.; Lu, M.; Mariappan, H.; Mistry, K.; Norris, B.; Rahhal-orabi, N.; Ranade, P.; Sandford, J.; Shifren, L.; Souw, V.; Tone, K.; Tambwe, F.; Thompson, A.; Towner, D.; Troeger, T.; Vandervoorn, P.; Wallace, C.; Wiedemer, J.; Wiegand, C. In *45 nm High- κ + Metal Gate Strain-Enhanced Transistors*, Symposium on VLSI Technology, June 17–19, 2008.
- (12) Wilk, G. D.; Wallace, R. M.; Anthony, J. M. High- κ Gate Dielectrics: Current Status and Materials Properties Considerations. *J. Appl. Phys.* **2001**, 89, S243–S275.
- (13) Buchanan, D. A. Scaling the Gate Dielectric: Materials, Integration, and Reliability. *IBM J. Res. Dev.* **1999**, 43, 245–264.
- (14) Robertson, J.; Wallace, R. M. High- κ Materials and Metal Gates for Cmos Applications. *Mater. Sci. Eng., R* **2015**, 88, 1–41.
- (15) He, G.; Deng, B.; Chen, H.; Chen, X.; Lv, J.; Ma, Y.; Sun, Z. Effect of Dimethylaluminumhydride-Derived Aluminum Oxynitride Passivation Layer on the Interface Chemistry and Band Alignment of Hf₂O₃-InGaAs Gate Stacks. *APL Mater.* **2013**, 1, No. 012104.
- (16) He, G.; Gao, J.; Chen, H.; Cui, J.; Sun, Z.; Chen, X. Modulating the Interface Quality and Electrical Properties of Hf₂O₃-InGaAs Gate Stack by Atomic-Layer-Deposition-Derived Al₂O₃ Passivation Layer. *ACS Appl. Mater. Interfaces* **2014**, 6, 22013–22025.
- (17) He, G.; Liu, J.; Chen, H.; Liu, Y.; Sun, Z.; Chen, X.; Liu, M.; Zhang, L. Interface Control and Modification of Band Alignment and Electrical Properties of Hf₂O₃/GaAs Gate Stacks by Nitrogen Incorporation. *J. Mater. Chem. C* **2014**, 2, S299–S308.
- (18) He, G.; Chen, X.; Sun, Z. Interface Engineering and Chemistry of Hf-Based High- κ Dielectrics on III–V Substrates. *Surf. Sci. Rep.* **2013**, 68, 68–107.
- (19) Zhang, J.; He, G.; Zhou, L.; Chen, H.; Chen, X.; Chen, X.; Deng, B.; Lv, J.; Sun, Z. Microstructure Optimization and Optical and Interfacial Properties Modulation of Sputtering-Derived HfO₂ Thin Films by TiO₂ Incorporation. *J. Alloys Compd.* **2014**, 611, 253–259.
- (20) Salahuddin, S.; Datta, S. Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices. *Nano Lett.* **2008**, 8, 405–410.
- (21) Salvatore, G. A.; Bouvet, D.; Ionescu, A. M. In *Demonstration of Subthreshold Swing Smaller Than 60mV/Decade in Fe-Fet with P(Vdf-Trfe)/SiO₂ Gate Stack*, IEEE International Electron Devices Meeting, Dec 15–17, 2008; pp 1–4.
- (22) Rusu, A.; Salvatore, G. A.; Jiménez, D.; Ionescu, A. M. In *Metal-Ferroelectric-Meta-Oxide-Semiconductor Field Effect Transistor with Sub-60mV/Decade Subthreshold Swing and Internal Voltage Amplification*, 2010 International Electron Devices Meeting, Dec 6–8, 2010; pp 16.13.11–16.13.14.
- (23) Ionescu, A. M.; Riel, H. Tunnel Field-Effect Transistors as Energy-Efficient Electronic Switches. *Nature* **2011**, 479, 329.
- (24) Khan, A. I.; Chatterjee, K.; Wang, B.; Drapcho, S.; You, L.; Serrao, C.; Bakaul, S. R.; Ramesh, R.; Salahuddin, S. Negative Capacitance in a Ferroelectric Capacitor. *Nat. Mater.* **2015**, 14, 182.

- (25) Dubourdieu, C.; Bruley, J.; Arruda, T. M.; Posadas, A.; Jordan-Sweet, J.; Frank, M. M.; Cartier, E.; Frank, D. J.; Kalinin, S. V.; Demkov, A. A.; Narayanan, V. Switching of Ferroelectric Polarization in Epitaxial BaTiO₃ Films on Silicon without a Conducting Bottom Electrode. *Nat. Nanotechnol.* **2013**, *8*, 748.
- (26) Islam Khan, A.; Bhowmik, D.; Yu, P.; Joo Kim, S.; Pan, X.; Ramesh, R.; Salahuddin, S. Experimental Evidence of Ferroelectric Negative Capacitance in Nanoscale Heterostructures. *Appl. Phys. Lett.* **2011**, *99*, No. 113501.
- (27) Appleby, D. J.; Ponon, N. K.; Kwa, K. S.; Zou, B.; Petrov, P. K.; Wang, T.; Alford, N. M.; O'Neill, A. Experimental Observation of Negative Capacitance in Ferroelectrics at Room Temperature. *Nano Lett.* **2014**, *14*, 3864–3868.
- (28) Gao, W.; Khan, A.; Marti, X.; Nelson, C.; Serrao, C.; Ravichandran, J.; Ramesh, R.; Salahuddin, S. Room-Temperature Negative Capacitance in a Ferroelectric–Dielectric Superlattice Heterostructure. *Nano Lett.* **2014**, *14*, 5814–5819.
- (29) Park, M. H.; Kim, H. J.; Kim, Y. J.; Lee, W.; Moon, T.; Hwang, C. S. Evolution of Phases and Ferroelectric Properties of Thin Hf_{0.5}Zr_{0.5}O₂ Films According to the Thickness and Annealing Temperature. *Appl. Phys. Lett.* **2013**, *102*, No. 242905.
- (30) Acharya, J.; Ma, C.; Brown, E.; Li, J.; Wu, J. Probing Effect of Temperature on Energy Storage Properties of Relaxor-Ferroelectric Epitaxial Pb_{0.92}La_{0.08}Zr_{0.52}Ti_{0.48}O₃ Thin Film Capacitors. *Thin Solid Films* **2016**, *616*, 711–716.
- (31) Brown, E.; Ma, C.; Acharya, J.; Ma, B.; Wu, J.; Li, J. Controlling Dielectric and Relaxor-Ferroelectric Properties for Energy Storage by Tuning Pb_{0.92}La_{0.08}Zr_{0.52}Ti_{0.48}O₃ Film Thickness. *ACS Appl. Mater. Interfaces* **2014**, *6*, 22417–22422.
- (32) Si, M.; Lyu, X.; Ye, P. D. Ferroelectric Polarization Switching of Hafnium Zirconium Oxide in a Ferroelectric/Dielectric Stack. *ACS Appl. Electron. Mater.* **2019**, *1*, 745–751.
- (33) Hoffmann, M.; Fengler, F. P. G.; Max, B.; Schroeder, U.; Slesazeck, S.; Mikolajick, T. Negative Capacitance for Electrostatic Supercapacitors. *Adv. Energy Mater.* **2019**, *9*, No. 1901154.
- (34) Luk'yanchuk, I.; Tikhonov, Y.; Sené, A.; Razumnaya, A.; Vinokur, V. M. Harnessing Ferroelectric Domains for Negative Capacitance. *Commun. Phys.* **2019**, *2*, No. 22.
- (35) Gich, M.; Fina, I.; Morelli, A.; Sánchez, F.; Alexe, M.; Gázquez, J.; Fontcuberta, J.; Roig, A. Multiferroic Iron Oxide Thin Films at Room Temperature. *Adv. Mater.* **2014**, *26*, 4645–4652.
- (36) Rao, C.; Sundaresan, A.; Saha, R. Multiferroic and Magneto-electric Oxides: The Emerging Scenario. *J. Phys. Chem. Lett.* **2012**, *3*, 2237–2246.
- (37) Eerenstein, W.; Mathur, N.; Scott, J. F. Multiferroic and Magnetoelectric Materials. *Nature* **2006**, *442*, 759.
- (38) Pyatakov, A. P.; Zvezdin, A. K. Magnetoelectric and Multiferroic Media. *Phys.-Usp.* **2012**, *55*, 557.
- (39) Acharya, J.; Wilt, J.; Liu, B.; Wu, J. Probing the Dielectric Properties of Ultrathin Al/Al₂O₃/Al Trilayers Fabricated Using in Situ Sputtering and Atomic Layer Deposition. *ACS Appl. Mater. Interfaces* **2018**, *10*, 3112–3120.
- (40) Elliot, A. J.; Malek, G. A.; Lu, R.; Han, S.; Yu, H.; Zhao, S.; Wu, J. Z. Integrating Atomic Layer Deposition and Ultra-High Vacuum Physical Vapor Deposition for in Situ Fabrication of Tunnel Junctions. *Rev. Sci. Instrum.* **2014**, *85*, No. 073904.
- (41) Elliot, A. J.; Malek, G.; Wille, L.; Lu, R.; Han, S.; Wu, J. Z.; Talvacchio, J.; Lewis, R. M. Probing the Nucleation of in Atomic Layer Deposition on Aluminum for Ultrathin Tunneling Barriers in Josephson Junctions. *IEEE Trans. Appl. Supercond.* **2013**, *23*, 1101405.
- (42) George, S. M. Atomic Layer Deposition: An Overview. *Chem. Rev.* **2010**, *110*, 111–131.
- (43) Groner, M.; Elam, J.; Fabreguette, F.; George, S. M. Electrical Characterization of Thin Al₂O₃ Films Grown by Atomic Layer Deposition on Silicon and Various Metal Substrates. *Thin Solid Films* **2002**, *413*, 186–197.
- (44) Barbos, C.; Blanc-Pelissier, D.; Fave, A.; Botella, C.; Regreny, P.; Grenet, G.; Blanquet, E.; Crisci, A.; Lemiti, M. Al₂O₃ Thin Films Deposited by Thermal Atomic Layer Deposition: Characterization for Photovoltaic Applications. *Thin Solid Films* **2016**, *617*, 108–113.
- (45) Wilt, J.; Gong, Y.; Gong, M.; Su, F.; Xu, H.; Sakidja, R.; Elliot, A.; Lu, R.; Zhao, S.; Han, S.; Wu, J. Z. Atomically Thin Al₂O₃ Films for Tunnel Junctions. *Phys. Rev. Appl.* **2017**, *7*, No. 064022.
- (46) Wilt, J.; Sakidja, R.; Goul, R.; Wu, J. Z. Effect of an Interfacial Layer on Electron Tunneling through Atomically Thin Al₂O₃ Tunnel Barriers. *ACS Appl. Mater. Interfaces* **2017**, *9*, 37468–37475.
- (47) Brown, E.; Ma, C.; Acharya, J.; Ma, B.; Wu, J.; Li, J. Controlling Dielectric and Relaxor-Ferroelectric Properties for Energy Storage by Tuning Pb_{0.92}La_{0.08}Zr_{0.52}Ti_{0.48}O₃ Film Thickness. *ACS Appl. Mater. Interfaces* **2014**, *6*, 22417–22422.
- (48) Ugeda, M. M.; Bradley, A. J.; Shi, S.-F.; Felipe, H.; Zhang, Y.; Qiu, D. Y.; Ruan, W.; Mo, S.-K.; Hussain, Z.; Shen, Z.-X.; et al. Giant Bandgap Renormalization and Excitonic Effects in a Monolayer Transition Metal Dichalcogenide Semiconductor. *Nat. Mater.* **2014**, *13*, 1091–1095.
- (49) Feenstra, R. M.; Gaan, S.; Meyer, G.; Rieder, K. Low-Temperature Tunneling Spectroscopy of Ge (111) C (2 × 8) Surfaces. *Phys. Rev. B* **2005**, *71*, No. 125316.
- (50) Dorneles, L.; Schaefer, D.; Carara, M.; Schelp, L. The Use of Simmons' Equation to Quantify the Insulating Barrier Parameters in Al/Alo_x/Al Tunnel Junctions. *Appl. Phys. Lett.* **2003**, *82*, 2832–2834.
- (51) Wilt, J.; Goul, R.; Acharya, J.; Sakidja, R.; Wu, J. Z. In Situ Atomic Layer Deposition and Electron Tunneling Characterization of Monolayer Al₂O₃ on Fe for Magnetic Tunnel Junctions. *AIP Adv.* **2018**, *8*, No. 125218.
- (52) Müller, J.; Böschke, T. S.; Bräuhäus, D.; Schröder, U.; Böttger, U.; Sundqvist, J.; Kücher, P.; Mikolajick, T.; Frey, L. Ferroelectric Zr_{0.5}Hf_{0.5}O₂ Thin Films for Nonvolatile Memory Applications. *Appl. Phys. Lett.* **2011**, *99*, No. 112901.
- (53) Kim, H.; McIntyre, P. C. Atomic Layer Deposition of Ultrathin Metal-Oxide Films for Nano-Scale Device Applications. *J. Korean Phys. Soc.* **2006**, *48*, 5–17.
- (54) Sun, F.-C.; Kesim, M.; Espinal, Y.; Alpay, S. Are Ferroelectric Multilayers Capacitors in Series? *J. Mater. Sci.* **2016**, *51*, 499–505.
- (55) Liu, Z.; Bhuiyan, M.; Ma, T. In A Critical Examination of 'Quasi-Static Negative Capacitance' (Qsnc) Theory, IEEE International Electron Devices Meeting (IEDM); IEEE, 2018; pp 31.32. 31–31.32. 34.
- (56) Wang, X.-H.; Chen, I. W.; Deng, X.-Y.; Wang, Y.-D.; Li, L.-T. New Progress in Development of Ferroelectric and Piezoelectric Nanoceramics. *J. Adv. Ceram.* **2015**, *4*, 1–21.