

A Continually-Stepped Variable-Gain LNA in 65-nm CMOS Enabled by a Tunable-Transformer for mm-Wave 5G Communications

Sheikh Nijam Ali^{#\$1}, Md Aminul Hoque[#], Srinivasan Gopal^{#\$*}, Mohammad Chahardori[#], Mohammad Ali Mokri[#], Deukhyoun Heo[#]

[#]School of EECS, Washington State University, Pullman, Washington, USA

^{\$}Skyworks Solutions Inc., San Jose, California, USA

^{*}Intel Corporation, Hillsboro, Oregon, USA

¹sheikh.ali@skyworksinc.com

Abstract—This paper presents a new continually-stepped variable gain low-noise-amplifier (CSVG-LNA) for millimeter-wave (mm-wave) 5G communications. The proposed variable-gain functionality in a two-stage LNA is achieved by incorporating a tunable-transformer at the 2nd-stage. The tunability in coupling-coefficient of the transformer allows to change the output matching of the LNA in a continuous fashion thus enabling a design of CSVG-LNA. The proposed CSVG-LNA alleviates high power consumption and large noise-figure (NF) variation problems in traditional approaches. To validate the proposed idea, we fabricated a CSVG-LNA in 65-nm CMOS process. The CSVG-LNA achieves measured 6.2dB of gain-tunability range while producing 18.2dB of peak S21 and <4.1dB of NF 28GHz. Further, the NF variation is only ~0.2dB across the entire 6.2dB gain-tuning range. The 3dB bandwidth of CSVG-LNA is about 12GHz (22-34GHz) while it consumes only 9.8mW of dc power. The CSVG-LNA occupies a compact core area of 0.2mm². The proposed CSVG-LNA achieves 1.5X improvement in FoM in comparison to state-of-the-arts mm-wave variable-gain CMOS LNAs.

Keywords—Low noise amplifier (LNA), 65nm CMOS, variable gain amplifier (VGA), noise figure (NF), low power, wideband, tunable transformer, tunable coupling coefficient, tunable inductor, tunable neutralization, 28GHz, 37GHz, 5G communications, receivers, mm-wave, phased-arrays.

I. INTRODUCTION

Concurrent fulfillment of low noise-figure (NF), low-power consumption and compact-chip area is critical for next-generation millimetre-wave (mm-wave) 5G phased-array receivers. Conventional receiver architecture employs a low noise amplifier (LNA) and a variable-gain amplifier (VGA) separately to control the overall gain of the receiver. Because of the use of two dedicated blocks, this approach increases the power consumption, area and design complexity in the receiver chain. In contrast, the integration of a variable-gain functionality in an LNA is an attractive choice to control the gain in a 5G phased-array receivers [1]–[3]. Because this approach can omit the need for a dedicated VGA in each phased-array receiver chains, thus, dramatically reducing power consumption, chip area and cost.

Recently demonstrated variable-gain LNAs at mm-wave frequencies use a coarse gain tuning mechanism by controlling bias supplies and/or tunable resistors [1]–[3]. These approaches are prone to frequency-shift across gain states and compromise NF in their low-gain configuration due to noise

mismatches. In addition, they are susceptible to process-voltage-temperature (PVT) variations because of the change in bias conditions for various gain states.

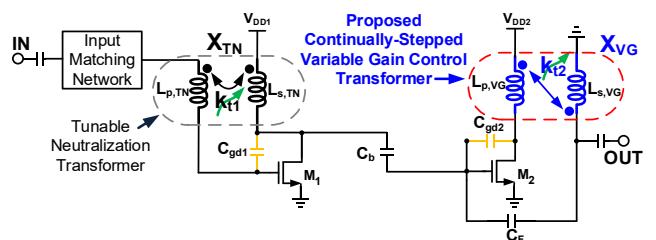


Fig. 1: Simplified circuit diagram of the proposed CSVG-LNA.

To achieve a variable-gain functionality in LNA without degrading NF or introducing additional design complexity, we present a new two-stage continually-stepped variable-gain LNA (CSVG-LNA) architecture as shown in Fig. 1 using compact low-loss tunable coupling-coefficient based transformers. The functionality of the tunable transformer (XVG) in the 2nd-stage is to achieve gain tunability while the tunable transformer (XTN) in the 1st-stage helps to enhance reverse isolation thus improvement in forward gain and NF. The proposed CSVG-LNA alleviates high power consumption and large NF variation problems in traditional approaches. The fabricated CSVG-LNA in 65-nm CMOS technology achieves measured 6.2dB of gain control while producing 18.2dB of peak gain and only 3.9–4.1dB of NF at 28GHz. The NF variation is only ~0.2dB across the entire gain-tunability range. The proposed CSVG-LNA achieves 1.5X improvement in FoM in comparison to state-of-the-arts mm-wave variable-gain CMOS LNAs.

II. PROPOSED CONTINUALLY-STEPPED VARIABLE-GAIN LNA

Fig. 1 shows the simplified circuit diagram of the proposed two-stage CSVG-LNA where both stages utilize a common-source (CS) configuration. The continually-stepped variable-gain functionality is achieved by incorporating a transformer (XVG) with a tunable coupling-coefficient (k_{12}) at the 2nd-stage. The primary coil ($L_{p,VG}$) of the transformer is connected to the device's (M_2) drain and supply (V_{DD2}) terminal while the secondary coil ($L_{s,VG}$) is connected to the output and ground terminal. The tunability of the coupling-coefficient in XVG

allows to change the matching network in a continuous fashion at the 2nd stage, thus enabling continual variation in gain of the LNA. We used a switched substrate-shield layout technique to achieve a tunable coupling coefficient in X_{VG} . The design methodology and the layout technique for the X_{VG} with tunable coupling coefficient can be found in [4].

Further, the X_{VG} generates a 180° phase shift of the signal as similar in the differential design with a cross-coupled capacitive feedback to the gate [5]. An additional feedback capacitance (C_F) is applied in between the gate of M_2 and the $L_{S,VG}$ of the X_{VG} to achieve the proper replica of a differential operation. In comparison to cross-coupled differential LNAs, this topology is capable to achieve 4-5dB higher G_{max} [5].

In a CS LNA the feedback caused by device parasitic gate-drain capacitance (C_{gd}) degrades the LNA's gain and reverse isolation (S_{12}). Neutralization is very effective way to mitigate this detrimental effect of C_{gd} with improvement in forward gain (S_{21}) and no penalty in power consumption. In literature cross-coupled capacitances [1] and transformer feedback [6] methods are applied to achieve neutralization. Cross-coupled capacitive neutralization can be only applied to a differential pair where the chip area and power consumption is large. In a single-ended design transformer feedback is an attractive way to neutralize C_{gd} by providing a magnetic feedback between the drain and gate of the device. Here, the phase of the magnetic feedback is opposite, but the magnitude is same in comparison to the unwanted C_{gd} coupling. However, this conventional transformer feedback neutralization with a fixed magnetic-coupling is not suitable at mm-wave frequencies where the net C_{gd} can be varied due to PVT variations, inaccuracies in electromagnetic (EM) simulation and interconnect modeling. As a result, there is a clear need of a tunable magnetic coupling in LNAs to address the unexpected change in C_{gd} .

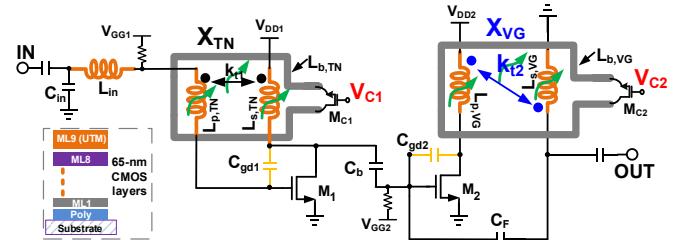
An effective neutralization approach for mm-wave LNAs using a tunable transformer (k_{t1}) is adopted in the 1st-stage as shown in Fig. 1. This tunable neutralization technique is widely used in mm-wave CMOS power amplifiers (PA) [4], [7-11] to improve stability, gain and efficiency, and but the use in an LNA is never reported. This technique can precisely neutralize the adverse effects of C_{gd} while achieving significant improvement in forward-gain, stability, and NF in an LNA.

The proposed CSVG-LNA offers three key benefits in the context of conventional topologies. First, this approach can omit frequency shift problem in conventional variable-gain LNAs with bias voltage change approach. Second, this proposed technique can reduce power consumption significantly due to the combined variable gain stage. Third, due to the compact area of the transformer the overall area of the CSVG-LNA is small as a result a compact phased-array receiver size can be realized.

III. IMPLEMENTATION AND SIMULATION RESULTS

A 65-nm CMOS technology is used to implement the proposed two-stage CSVG-LNA. Fig. 2 shows the complete circuit diagram with component values. Total device width of

50μm and 64μm is used for M_1 and M_2 respectively. Both tunable transformers utilize bottom coils ($L_{b,TN}$, $L_{b,VG}$) in metal-1 layer (ML1) to modulate the inductance of their primary ($L_{p,TN}$, $L_{p,VG}$) and secondary ($L_{s,TN}$, $L_{s,VG}$) coils. The $L_{b,TN}$ and $L_{b,VG}$ are connected to switch, M_{c1} and M_{c2} respectively. If the control voltages (V_{c1} and V_{c2}) of these switches are turned-on it reduces the inductance values in their primary and secondary coils of X_{VG} and X_{TN} [4]. In contrast, if the switches are turned-off the primary and secondary coils of X_{VG} and X_{TN} remains unchanged. As a result, this inductance modulation creates the coupling coefficient change in the transforms [4]. The post layout simulation results show change in k_{t1} and k_{t2} of 0.1 to 0.2 and 0.3 to 0.7 respectively. The quality factors of the X_{CV} , X_{TN} are always better than 18.



$W_{M1, M2}$ (μm)	$L_{p,TN}$ (pH)	$L_{s,TN}$ (pH)	$L_{p,VG}$ (pH)	$L_{s,VG}$ (pH)	C_F (fF)	L_{in} (pH)	k_{t1}	k_{t2}
50/64	260	240	250	200	9	235	0.1-0.2	0.3-0.7

Fig. 2. Complete circuit diagram of the proposed CSVG-LNA. The switched substrate shield layout technique for X_{TN} and X_{VG} is not shown here and can be found in [4].

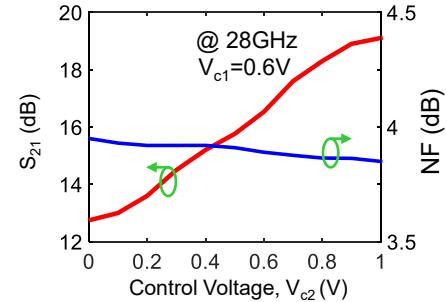


Fig. 3: Post-layout simulation results of S_{21} and NF at 28GHz for various V_{c2} of X_{VG} while keeping $V_{c1}=0.6V$.

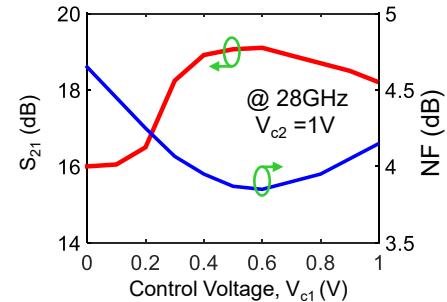


Fig. 4: Post-layout simulation results of S_{21} and NF at 28GHz for various V_{c1} of X_{VG} while keeping $V_{c2}=1V$.

With the selected device size and passive component values the two-stage LNA provides about 19dB of peak gain and 4dB of NF while consuming 9mW of power. Fig. 3 shows the post-layout simulation result of the CSVG-LNA's gain and NF across the control voltage (V_{c2}) of X_{VG} . As V_{c2} increases the gain increases because k_{t2} increases. Also, the gain drops with decrease in V_{c2} as k_{t2} decreases. For full range of V_{c2} the gain changes about 6.4dB (19-12.6) at 28GHz. Notice that the NF only changes by 0.2dB across this entire 6.4dB of gain-tuning range showing the merit of this proposed technique. Fig. 4 shows post-layout simulation result of the CSVG-LNA's gain and NF across the control voltage (V_{c1}) of X_{TN} while keeping $V_{c2} = 1V$. The 1st -stage requires a certain k_{t1} to neutralize the effect of C_{gd} . For this design at V_{c1} of 0.6V the LNA shows peak S_{21} of 19dB. This V_{c1} condition correspond to k_{t1} of 0.17. At this point the NF is also minimum which is about 3.9dB. Since $V_{c1} = 0.6V$ produces peak S_{21} and minimum NF, this setting is used for the plot in Fig. 3. The gain-tuning range can be increased further (i.e., 10-12dB) by incorporating a third-stage with proposed X_{VG} and/or increasing the k_{t2} (i.e., 0.1-0.9) range.

IV. EXPERIMENTAL RESULTS

Fig. 5 shows the chip prototype in 65-nm CMOS which occupies an active area of 0.16mm². The measurement results of the S_{21} across frequency for V_{c2} of 1 to 0V with a step of 0.2V are plotted in Fig. 6. A peak S_{21} of 18.2dB for $V_{c2} = 1V$ while a S_{21} of 12dB is achieved for $V_{c2} = 0V$ at 28GHz resulting about 6.2dB of gain tuning range. Note that the S_{21} can be reconfigured in a continuous fashion at band of interest by providing a finer step of V_{c2} . The S_{12} was better than -35dB with a setting of V_{c1} of 0.6V showing the effectiveness of tunable neutralization in a CS configuration. The stability factor is better than 5.5 from DC to 34GHz across all the gain states. Fig. 7 shows the measured S_{22} and S_{11} across frequency with various V_{c2} . With the change in V_{c2} the S_{22} changes as expected while the change in S_{11} small. As a result, the proposed technique is capable to show low NF variations which is shows in Fig. 8.

Only 0.2dB of NF variation is achieved at 28GHz while maintaining NF of 3.9-4.1dB (Fig. 8). Moreover, the NF is <4.3dB across 24-32GHz. At 28GHz the input 1-dB point (IP_{1dB}) is -15dB for $V_{c1}=0.6V$ and $V_{c2}=1V$ while consuming only 9.8mW of power (P_{dc}). Table 1 shows the performance summary and comparison with state-of-the-arts variable gain LNAs at mm-wave. The proposed CSVG-LNA is capable to achieve lowest NF variations while consuming significantly lower power. As a result, a 1.5X improvement in FoM is achieved. The FoM definition [2] is provided in (1).

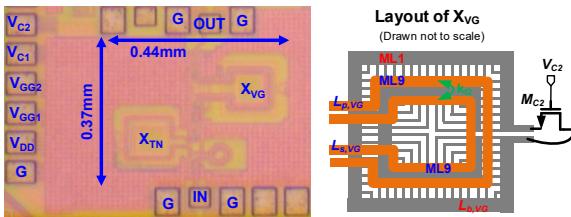


Fig. 5: Die micrograph and layout of X_{VG} in 65nm CMOS technology.

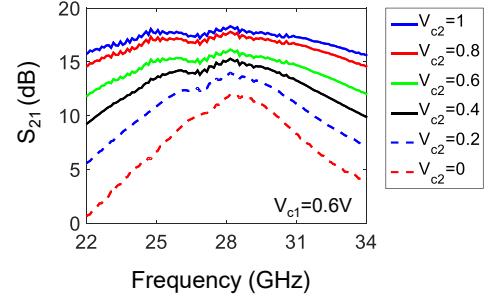


Fig. 6: Measurement results of S_{21} across frequency for various V_{c2} .

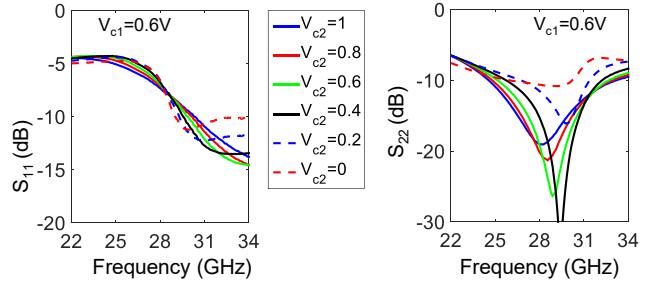


Fig. 7: Measurement results of S_{22} and S_{11} across frequency.

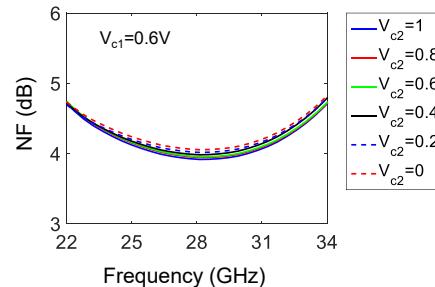


Fig. 8: Measurement results of NF for various V_{c2} .

Table 1. Performance summary and comparison with state-of-the-arts mm-wave CMOS variable gain LNAs

Parameters	Our Work	[2] MWCL'18	[1] ISSCC'16	[3] ESSCIRC'14
CMOS Tech.	65nm	40nm	28nm	28nm
Freq. (GHz)	28	27.5	82.3	79
# of Stages	2 (CS)	3 (Differ.)	3 (Differ.)	3 (Differ.)
Gain & Range (dB)	18.2-12	27.1-18.4	29.6-18	19.3 -23.8
3dB BW* (GHz)	12	9.3	28.3	10
NF (dB)	3.9-4.1	3.4-4.4	6.4-8.2	4.9-5.6
P _{dc} * (mW)	9.8	21.5	31.3	30.6
Supply (V)	1	1.1	0.9	0.9
IP _{1dB} * (dBm)	-15	-13.4	-28.1	-18.5
Area ⁺ (mm ²)	0.16	0.26	0.25	0.15
FoM*	1758	1152	380	530

*maximum gain condition, +active area only

$$\text{FoM [MHz]} = \frac{\text{Gain}_{\text{peak}}[\text{ratio}] \text{ BW}[{\text{MHz}}]}{F_{\text{min}} - 1} \times \frac{I_{\text{P}_{\text{1dB}}[\text{mW}]} }{P_{\text{dc}}[\text{mW}]} \quad (1)$$

V. CONCLUSION

A new continually-stepped variable gain low-noise-amplifier (CSVG-LNA) for mm-wave 5G receivers is proposed. The tunability in coupling-coefficient of the transformer allows to change the output matching of the LNA in a continuous fashion resulting a continuous gain-variation. The proposed technique alleviates high power consumption and large NF variation problems in traditional designs. A prototype in 65-nm CMOS achieves measured 6.2dB of gain control while producing 18.2dB of S_{21} and 3.9-4.1dB of NF 28GHz resulting only ~ 0.2 dB NF deviation. The chip occupies a compact core area of 0.2mm^2 and consumes only 9.8mW of power. As a result, a 1.5X improvement in FoM in comparison to state-of-the-arts mm-wave variable-gain CMOS LNAs are achieved. The proposed CSVG-LNA presents an attractive solution for next-generation compact and low-cost 5G phased-array receivers.

ACKNOWLEDGEMENT

This work was supported in part by the U.S. National Science Foundation (NSF) under Grant CNS-1564014 and CNS-1705026, and in part by the NSF Center for Design of Analog Digital Integrated Circuits (CDADIC) and in part by the Joint Center for Aerospace Technology Innovation (JCATI).

REFERENCES

- [1] M. Vigilante and P. Reynaert, "A 68.1-to-96.4GHz variable-gain low-noise amplifier in 28nm CMOS," in *IEEE ISSCC*, 2016, pp. 360–362.
- [2] M. Elkholby, S. Shakib, J. Dunworth, V. Aparin, and K. Entesari, "A wideband variable gain LNA with high OIP3 for 5G using 40-nm bulk CMOS," *IEEE MWCL*, vol. 28, no. 1, pp. 64–66, Jan. 2018.
- [3] A. Medra, V. Giannini, D. Guermandi, and P. Wambacq, "A 79GHz variable gain low-noise amplifier and power amplifier in 28nm CMOS operating up to 125°C," in *ESSCIRC*, 2014, pp. 183–186.
- [4] S. N. Ali *et al.*, "A 40% PAE frequency-reconfigurable CMOS power amplifier with tunable gate-drain neutralization for 28-GHz 5G radios," *IEEE TMTT*, vol. 66, no. 5, pp. 2231–2245, May 2018.
- [5] E. Cohen, O. Degani, and D. Ritter, "A wideband gain-boosting 8mW LNA with 23dB gain and 4dB NF in 65nm CMOS process for 60 GHz applications," in *IEEE RFIC*, 2012, pp. 207–210.
- [6] D. J. Cassan and J. R. Long, "A 1-V transformer-feedback low-noise amplifier for 5-GHz wireless LAN in 0.18um CMOS," *IEEE JSSC*, vol. 38, no. 3, pp. 427–435, Mar. 2003.
- [7] S. N. Ali *et al.*, "A 28GHz 41%-PAE linear CMOS power amplifier using a transformer-based AM-PM distortion-correction technique for 5G phased arrays," in *IEEE ISSCC*, 2018, pp. 406–408.
- [8] S. N. Ali *et al.*, "A 25-35 GHz neutralized continuous Class-F CMOS power amplifier for 5G mobile communications achieving 26% modulation PAE at 1.5 Gb/s and 46.4% peak PAE," *IEEE TCAS-I: Regular Papers*, pp. 1–14, 2018.
- [9] S. N. Ali, P. Agarwal, S. Mirabbasi, and D. Heo, "A 42-46.4% PAE continuous class-F power amplifier with Cgd neutralization at 26-34 GHz in 65 nm CMOS for 5G applications," in *IEEE RFIC*, 2017, pp. 212–215.
- [10] S. N. Ali, P. Agarwal, J. Baylon, and D. Heo, "Reconfigurable high efficiency power amplifier with tunable coupling coefficient based transformer for 5G applications," in *IEEE MTT-S IMS*, 2017, pp. 1177–1180.
- [11] P. Agarwal, S. N. Ali, and D. Heo, "Reconfigurable phased-array design techniques for 5G and beyond communications," in *IEEE RFIT*, 2017, pp. 53–55.