# A Ka-Band Dual-Band Digitally Controlled Oscillator With —195.1-dBc/Hz FoM<sub>T</sub> Based on a Compact High-Q Dual-Path Phase-Switched Inductor

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Abstract—In this paper, a compact, low-loss, dual-path phaseswitched inductor suitable for millimeter-wave (mmWave) transceiver subblocks is proposed. The signal path through the structure is determined by the relative polarity of two differential excitation signals applied to the four-port structure. Because inductance is varied by altering signal path through the inductor, signal-path MOSFET switches are avoided. The inductor, therefore, demonstrates high, mode-invariant quality factor, facilitating the design of high-performance dual-band mmWave transceiver subblocks. Based on the proposed inductor, a dualband Ka-band oscillator is designed in a 65-nm CMOS technology which covers two frequency bands from 14.8 to 18.7 GHz and from 20.8 to 26.6 GHz. The proposed inductor facilitates a widely tunable, dual-band frequency range while maintaining the state-of-the-art phase noise, power consumption, and figure of merit (FoM). The oscillator achieves measured fractional tuning ranges of 23.3% and 24.5% and phase noise of -115.1 dBc/Hz at 2-MHz offset while consuming only 4.8-mW dc power. A peak tuning-range FoM of -195.1 and -194.9 dBc/Hz is demonstrated across the low- and high-frequency bands.

Index Terms—Fractional tuning range (FTR), inductive frequency tuning, millimeter wave (mmWave), phase-switched inductor, voltage-controlled oscillator (VCO).

## I. Introduction

WITH the advent of the 5G era, wideband transceiver hardware design at millimeter-wave (mmWave) frequencies is more important than ever [1]. While spectrum allocation for next-generation cellular has largely focused on a

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28-GHz frequency band, expansion is likely to continue into frequency bands ranging across the mmWave spectrum [2]. Furthermore, modern mobile communications' applications require the use of cellular and ISM frequency bands ranging across single-digit GHz frequencies. The hardware requirements for next-generation wireless and cellular communication present conflicting design challenges of low power operation for mobile applications, excellent noise performance for reliable communication with complex modulation schemes, and modular or frequency reconfigurable designs for compact, low-cost solutions in a dynamic wireless environment with numerous disparate frequency bands [3], [4]. Generation of mmWave local oscillator (LO) signals which meet the requirements of next-generation cellular hardware remains a particularly difficult design challenge.

Wideband frequency-reconfigurable signal source circuits suited for next-generation wireless systems must simultaneously minimize power consumption and noise. Variable capacitors designed using analog-tuned varactors or MOSFET switch-based digital capacitor banks are traditionally used to facilitate tunability across a range of frequencies. However, in this architecture, low noise performance and low power consumption require designing for narrowband performance, and wide tunability can only be accomplished at the expense of noise and power [5]. The increased effect of parasitic behaviors at mmWave frequencies significantly degrades power and noise performance and tuning range of mmWave voltage-controlled oscillators (VCOs).

To address the challenges of multi-band mmWave transceiver and transceiver subblock design, we present a dual-path phase-switched inductor with a compact layout and excellent quality factor with minimal variation between the two excitation modes utilizing a simple control methodology. Unlike recent research into transformer-coupling-based variable inductor designs [6]–[11] which degrade quality factor and limit frequency of operation, the proposed inductor uses the relative polarity of two excitation signals to determine the signal path through the innovative layout structure. This improves quality factor, allows a large variability in effective inductance, and maintains a compact layout and

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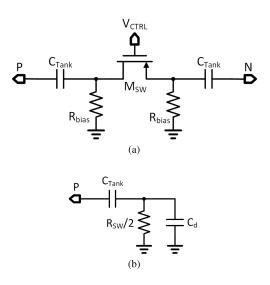


Fig. 1. (a) Schematic of a digitally controlled switched capacitor traditionally used in VCOs. (b) Equivalent simplified half-circuit model.

simple control scheme. While the proposed inductor can facilitate dual-band design for many transceiver subblocks, this paper presents a widely tunable dual-band digitally controlled oscillator (DCO). The average tuning-range figure of merit (FoM) (FoM $_T$ ) of -190.5 and -192.3 dBc/Hz in the low- and high-frequency bands, respectively, demonstrates the potential for high-performance dual-band mmWave design.

The rest of this paper is organized as follows. Section II discusses traditional capacitive tuning along with the recently developed inductive tuning techniques. Section III presents the proposed inductor topology with analysis and simulated results. Section IV presents a dual-band signal source based on the proposed dual-path phase-switched inductor. Section V presents the measured results of the proposed signal source circuit. Section VI discusses conclusions.

## II. WIDEBAND OSCILLATOR DESIGN

Traditional capacitively tuned signal source circuits rely on digitally tuned capacitor banks controlled with metal-oxidesemiconductor field-effect transistor (MOSFET) switches, as in Fig. 1(a). R<sub>bias</sub> is used to set the dc voltage of the source and drain nodes of  $M_{SW}$ , typically chosen as a large value to ensure minimal impact on the RF performance. This technique introduces a stringent design tradeoff between noise performance and tuning range. The MOSFET switch used in these digitally controlled capacitor banks can be modeled as a digitally controlled resistance in parallel with a parasitic capacitance, as shown in Fig. 1(b). Note that the value of  $R_{\rm SW}$  is dominated by the switch channel resistance rather than  $R_{\rm bias}$ . The resistance of the switch in the ON state is roughly inversely proportional to the width of the switch. However, the effective parallel parasitic capacitance increases roughly linearly with width. In the OFF state, this parasitic capacitance increases the capacitance presented to the tank, decreasing the  $C_{\rm ON}/C_{\rm OFF}$  ratio. Therefore, increasing switch size improves the quality factor of the tank but decreases the achievable tun-

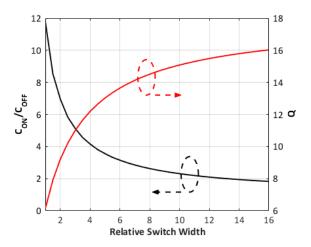


Fig. 2. Capacitance tuning ratio,  $\eta$ , of the switched capacitor bank shown in Fig. 1.

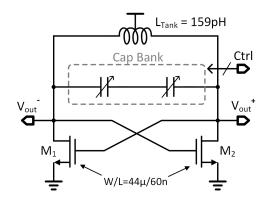


Fig. 3. Schematic of the simulated capacitively tuned 20-GHz signal source.

ing range. Conversely, decreasing switch size allows improved tuning range, but the quality factor of the capacitor bank is reduced.

Spectre simulations performed in Cadence Virtuoso of the capacitor network shown in Fig. 1(a) demonstrate the impact of this tradeoff. Fig. 2 shows the capacitance tuning ratio  $C_{\rm ON}/C_{\rm OFF}$  ( $\eta$ ) and the quality factor (Q), both observed at 20 GHz, resulting from varying the width of the switches with constant minimum length of 60 nm. The switch transistor width is varied by adjusting the number of fingers while maintaining a constant finger width. A large  $\eta$  requires extreme comprise of Q, and a large Q requires severely degraded  $\eta$ . At mmWave frequencies, the frequency tunability of this architecture further degrades, as parasitic capacitance has an increased impact.

The quality factor of the resonant tank directly impacts both the noise and power consumption of a VCO circuit [12]. To demonstrate the impact of capacitive tuning tradeoff, the signal source circuit shown in Fig. 3 was also simulated in Spectre using a 65-nm CMOS process. A resonant tank with a center frequency of approximately 20 GHz was constructed using a postlayout simulated single-turn inductor implemented in the ultrathick top metal layer of the CMOS process. Fig. 4 shows the VCO's FoM, calculated as in (1), with varying

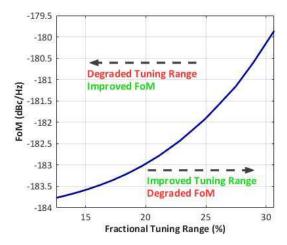


Fig. 4. Simulated FoM, calculated as in (1), of the oscillator shown in Fig. 3. Power consumption and phase noise both increase with increased tuning range, degrading the FoM.

fractional tuning range (FTR) accomplished by changing the switch size

$$FoM = PN - 20 \cdot \log_{10} \left( \frac{f_c}{\Delta f} \right) + 10 \log_{10} \cdot \left( \frac{P_{DC}}{1 \text{ mW}} \right). \quad (1)$$

In (1),  $f_c$  is the oscillator's center frequency, PN is the phase noise,  $\Delta f$  is the offset frequency at which phase noise is observed (1 MHz in this simulation), and  $P_{\rm dc}$  is the power consumption of the oscillator. This metric accounts for both the degradation of phase noise and power consumption; therefore, a strong correlation between FoM and tuning range is observed.

The strong correlation of FoM with tuning range underscores the limitations of wideband signal source design with the traditional capacitive tuning paradigm.

#### A. Tunable Inductors

Recently, significant research has targeted tunable or switchable inductors [6]–[11], [13]–[19]. Some previous attempts at switchable inductors leverage MOSFET switches in the signal path [18]–[20]. While a large FTR is possible with such an approach, signal path switches severely degrade the quality factor (*Q*) of the inductor. Alternative approaches leverage magnetically coupled secondary structures which reduce the effective inductance of the primary inductor [6]–[11], [21]. While these avoid direct signal path switches and, therefore, can achieve improved quality factor, an MOSFET switch is still typically required on the secondary structure to enable tuning, resulting in increased loss.

Alternative approaches have been proposed recently, which avoid the use of signal path switches by the use of mode-controlled passive structures [14], [22], [23]. For example, [14] leverages mode switching in an innovative inductor topology to achieve octave tuning across a continuous frequency range. An innovative series resonator is proposed, which allows dramatically increased tuning range controlled by activating and deactivating the active  $G_m$  cells in the oscillator core. While the oscillator achieves good wideband performance at around 10 GHz, the complex layout and control scheme

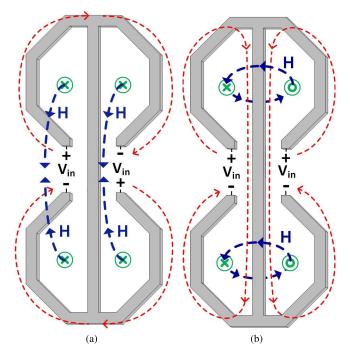


Fig. 5. Proposed dual-path phase-switched inductor with (a) odd- and (b) even-mode excitation. Signal path and representative magnetic field (H) flux lines are shown in red and blue, respectively.

limit application and performance. The signal source proposed in [23] uses an innovative inductor topology to achieve good tuning performance at mmWave frequencies. However, the 4-core structure and the corresponding control circuitry result in increased design complexity and power consumption.

Yet another design [11] leverages a phase-based switching architecture, which uses a magnetically coupled secondary inductor structure excited by the inductors of two identical oscillator tanks. This approach allows two inductance states controlled without signal path switches, allowing a 21.7% tuning range at the fundamental frequency of 85 GHz. However, the use of transformer coupling increases sensitivity to layout parasitics and degrades self-resonant frequency of the inductor. Additionally, the magnetically coupled structure simultaneously increases resistive losses and decreases reactive impedance. Both factors decrease the quality factor of the tank corresponding to the high-frequency state of the oscillator.

While the recent developments in tunable and switchable inductors have demonstrated the possibility of improving signal source tuning range with minimal performance overhead, broad adoption requires additional breakthroughs.

# III. DUAL-PATH PHASE-SWITCHED INDUCTOR

We propose a dual-path phase-switched inductor which augments traditional capacitive frequency tuning by introducing a low-loss dual-path inductor with large fractional tunability.

As shown in Fig. 5, the switchable inductance is achieved by controlling the relative phases of the two differential ports of the inductor, thereby changing the signal path through the inductor. When the two inputs are out of phase (odd mode), as in Fig. 5(a), the signal path passes from the positive node of the left input to the negative node of the right, passing

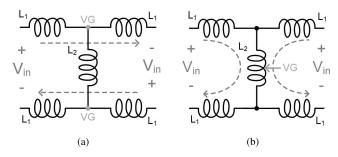


Fig. 6. Equivalent simplified model of the proposed dual-path phase-switched inductor under (a) odd- and (b) even-mode excitation. Changing the relative phase of the input signals alters the signal path and VG locations, changing the effective inductance.

only through the respective loops on the top and bottom of the inductor. However, if the relative phase of the right input is switched, giving in-phase (even mode) inputs, the return path passes through the long center trace connecting the top and bottom loops, as in Fig. 5(b). This gives a significant increase in effective inductance. Moreover, because the inductance value is controlled simply by the relative phase, the loss of the inductor remains low in both states. The schematic equivalent configurations of the proposed inductor under odd- and even-mode excitation are shown in Fig. 6(a) and (b), respectively. Under odd-mode excitation, the lowest impedance signal path crosses between the two excitation signals, giving an effective odd-mode inductance of  $L_{eq,odd} =$  $2 \cdot L_1$ . Furthermore, by symmetry, the vertical center line between the two excitation signals forms a virtual ground. The center connection between the two loops, therefore, does not contribute to the inductance of the resulting network, as shown in Fig. 6(a).

Under even-mode excitation, only symmetry between the top and bottom halves is maintained, rotating the primary axis of symmetry to a line separating the positive and negative terminals of the excitation signal. The corresponding signal path now extends through the long trace connecting the center points of the two loops. The resulting equivalent even-mode inductance is  $L_{\rm eq,even} = 2 \cdot L_1 + L_2$ . If the contributions of  $L_1$  can be minimized, the tuning range of the switchable inductance is maximized.

The proposed inductor architecture offers an additional benefit of mutual coupling between the inductor halves in each excitation state. As shown in the representative flux lines shown in blue in Fig. 5, the layout of the inductor is designed such that flux adds destructively in odd-mode excitation but adds constructively in even-mode excitation.

Inductance is defined by the relationship between magnetic flux and excitation current [24] ( $\Phi$  and  $i_e$ , respectively), as in (2).  $H(i_e)$  is the magnetic field strength resulting from an excitation current  $i_e$ . Dividing H by the magnetic permeability  $\mu$  gives the magnetic flux density, which is integrated over the area of the inductor to give the magnetic flux excited by  $i_e$ 

$$L_{eq} \equiv \frac{\Phi}{i_e} = \frac{1}{i_e} \cdot \oint_{S} \frac{H(i_e)}{\mu} \cdot dA. \tag{2}$$

The impact of flux sharing is easily observed under oddmode excitation. The effective inductance in the absence

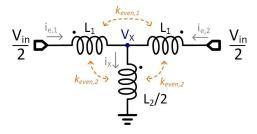


Fig. 7. Equivalent coupled inductor half-circuit model of the even-mode inductance.

of coupling is approximately  $2 \cdot L_1$ , and a small negative coupling coefficient results from flux sharing between the two equivalent inductors, as shown in Fig. 5(a). If the proportion of shared flux is denoted  $k_{\rm odd}$ , the resulting mutual inductance is given as

$$L_{\text{odd}} = \frac{1}{i_e} \cdot \oint_S \frac{H(i_e) - k_{\text{odd}} \cdot H(i_e)}{\mu} \cdot dA$$
$$= 2 \cdot L_1 \cdot (1 - k_{\text{odd}}). \tag{3}$$

Note that the excitation current used for calculating the coupled flux term is the same as the original excitation current, resulting from the second (identical) oscillator. The corresponding inductance in odd-mode operation is decreased.

The effective even-mode inductance is best considered by breaking the effect of mutual coupling on each inductance term in an equivalent half-circuit observed between one input and the virtual ground node at the center of  $L_2$ , as shown in Fig. 7. Accounting for the coupling terms shown,  $V_X$  can be calculated in terms of the excitation current as

$$V_X = \frac{L_2}{2} \cdot \frac{di_X}{dt} + M_{1,2} \cdot \frac{di_{e,1}}{dt} + M_{1,2} \cdot \frac{di_{e,2}}{dt}$$
(4)

where

$$M_{1,2} = k_{\text{even},2} \cdot \sqrt{\frac{L_1 \cdot L_2}{2}}.$$
 (5)

 $V_{\rm in}$  is calculated from  $V_X$  and the excitation currents as in (6). Because the current through  $L_2$  is a result of current from both inputs, only half of  $V_X$  and  $i_X$  are included to account only for the voltage from one input

$$\frac{V_{in}}{2} = \frac{V_X}{2} + L_1 \cdot \frac{di_{e,1}}{dt} + M_{1,1} \cdot \frac{di_{e,2}}{dt} + \frac{M_{1,2}}{2} \cdot \frac{di_X}{dt}$$
 (6)

where

$$M_{1,1} = k_{\text{even},1} \cdot L_1. \tag{7}$$

Noting that  $i_{e,1} = i_{e,2} = i_X/2$ , the effective half-circuit input voltage  $V_{\text{in}}/2$  resulting from an excitation current  $i_{e,1}$  can be calculated from (4) and (6) as follows:

$$\frac{V_{in}}{2} = \frac{di_{e,1}}{dt} \cdot \left(L_1 + \frac{L_2}{2} + 2 \cdot M_{1,2} + M_{1,1}\right). \tag{8}$$

The net inductance is calculated from (7), (5), and (8) as

$$L_{\text{even}} = 2 \cdot L_1 \cdot (1 + k_{\text{even},1}) + L_2 + 4 \cdot k_{\text{even},2} \cdot \sqrt{\frac{L_1 \cdot L_2}{2}}.$$
 (9)

The influence of the coupling factors in even-mode operation has a significant impact on the equivalent

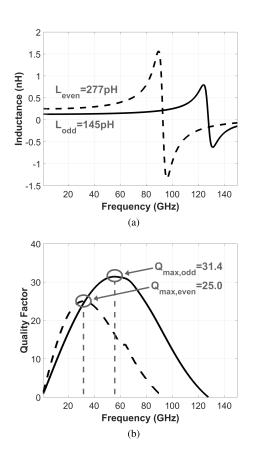


Fig. 8. Simulated (a) inductance and (b) quality factor of the proposed inductor under even- and odd-mode excitation. Dashed (solid) lines: inductor's performance under even- (odd-) mode excitation.

even-mode inductance, improving the inductance range possible with the proposed structure. Simulated results discussed in Section III-A demonstrate the inductance variation in a practical design.

## A. Simulated Inductor Performance

The inductor architecture of Fig. 5 has been implemented in a 65-nm CMOS process. The structure was simulated using Keysight's ADS Momentum 2.5D EM simulator, and the resulting inductance and quality factor in the two excitation states are shown in Fig. 8(a) and (b), respectively. These values were simulated by differentially exciting one input with an ac voltage signal, while exciting the second input for either even- or odd-mode behavior. The resulting current from each source was divided by 2 to account for the dual excitation and was then used to compute effective impedance. The inductance ranges from 145 to 277 pH, a 91% range, and the peak quality factor exceeds 25 in both states. Note that the quality factor under odd-mode excitation is slightly higher, resulting from the smaller diameter-to-area ratio compared to that of the evenmode excitation signal path, slightly improving performance in higher frequency operation.

The coupling factor can be observed from simulated results by comparing the inductance of one loop with and without secondary loop excitation. The simulated coupling factor between the two inductors is 0.33 and 0.03 in even- and odd-mode operations. Odd-mode excitation will typically observe a lower

coupling factor than even-mode operation, but the size, aspect ratio, and location of the loops can be adjusted if higher coupling (and corresponding reduced inductance) is desired in the odd-mode operation. Note nonetheless that both coupling factors play favorably into the achievable change in inductance.

Such a topology requires generation of two signals and control of the relative phase between in-phase and antiphase. The method by which these in-phase and antiphase signals are generated and applied to the four terminals of the dual-path inductor will depend heavily on the application and system context in which it is used. A cross-coupled switch network, for example, is suitable for low-loss, simple phase control in a dual-core, dual-band mmWave oscillator. Such a topology is discussed in Section IV. The proposed dual-path inductor improves the feasibility of inductively tuned oscillators by introducing a compact, high-Q, widely tunable inductor.

# B. Oscillator LC Tuning

The FTR for a signal source is calculated in (10), (11), and (12), where  $C_{\rm tank,min}$  is the minimum tank capacitance excluding parasitic effects. The introduction of inductive tuning dramatically improves the tuning range tradeoff discussed in Section II. For example, if an  $\eta$  of 2 is chosen for the capacitor bank, and a modest parasitic capacitance ( $C_P$ ) of 20% of the resonant tank's maximum capacitance is assumed, capacitive tuning gives the FTR of 26.8% from (10). When inductive tuning is introduced and the simulated 91% relative inductance variation is assumed, the FTR improves to 53.5%

$$FTR = \frac{\Delta f}{f_c}$$

$$= 2 \cdot \frac{\sqrt{L_{\text{even}} \cdot C_{\text{max}}} - \sqrt{L_{\text{odd}} \cdot C_{\text{min}}}}{\sqrt{L_{\text{even}} \cdot C_{\text{max}}} + \sqrt{L_{\text{odd}} \cdot C_{\text{min}}}}.$$
(10)

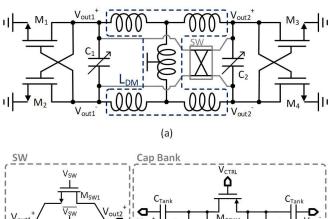
$$C_{\text{max}} = \eta \cdot C_{\text{tank,min}} + C_P. \tag{11}$$

$$C_{\min} = C_{\tanh,\min} + C_P. \tag{12}$$

If needed, the FTR can be further improved by the introduction of a capacitor between the positive input of the left (right) half and negative input of the right (left) half in the even-mode operation [see Fig. 5(b)], similar to the coupling capacitors used in [25]. In the odd-mode operation, this capacitor has no voltage across it, and loading in the high-frequency mode is minimal. In the even-mode operation, the full input voltage is seen across this capacitor, decreasing the resonant frequency of the tank. This decreases the achievable minimum resonant frequency without impacting the maximum frequency of operation.

# IV. PROPOSED DUAL-BAND OSCILLATOR

An oscillator designed to satisfy the requirements discussed in Section I is designed which leverages the proposed dualpath phase-switched inductor. The schematic and implementation details of the proposed dual-band oscillator are shown in Fig. 9. A simple cross-coupled pair is used to generate the negative transconductance required to counteract the loss of the *LC* tank. This requires only a single NMOS device



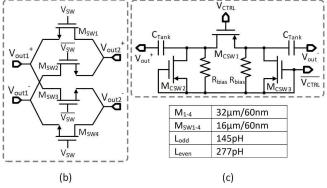


Fig. 9. Schematic of the proposed DCO (a) and phase control switch array (b). The proposed dual-path inductor is used to achieve dual-band operation. A MOSFET switched capacitor array (c) is used to provide continuous frequency tuning.

operating between  $V_{\rm DD}$  and ground, allowing low supply voltage operation. It should be noted that voltage-mode operation does cause significant dependence of oscillator performance on supply voltage. However, the low supply voltage facilitated by this topology reduces the power overhead required to satisfy startup conditions and allows design flexibility for low-power applications. Furthermore, the reduced power consumption mitigates some of the additional power consumption required by the use of two oscillator cores. A higher  $V_{\rm DD}$  can offer improved phase noise performance, but at the cost of significantly higher power consumption. A  $V_{\rm DD}$  of 0.45 V was chosen for this design as an advantageous tradeoff between power consumption and oscillator performance. The frequency of oscillation is found by the application of (3) and (9) to the standard LC oscillator topology. As discussed in Section III, the equivalent inductance corresponding to even- or odd-mode operation can be applied directly to the parallel resonant tank shown in Fig. 9(a). The resulting resonant frequency dictates the frequency of oscillation.

Fine frequency tuning is accomplished using an MOSFET switched capacitor bank similar to that shown in Fig. 1(a). The schematic of one such cell is shown in Fig. 9(c). Two additional MOSFETs are introduced to the schematic shown in Fig. 1(a), namely,  $M_{\rm CSW2}$  and  $M_{\rm CSW3}$ . When the control bit is high, i.e.,  $V_{\rm CTRL}$  is 1 V,  $M_{\rm CSW1}$  is on and the capacitance presented to the tank is approximately  $C_{\rm tank}$ . The introduced switches are both OFF in this state; therefore, they negligibly impact the impedance of the network. The resistors shown in Fig. 9(c) are added to ensure that the source and drain nodes of  $M_{\rm CSW1}$  are pulled to ground. When the control bit is low, the switches are driven "ON" by  $\overline{V_{\rm CTRL}}$ .  $M_{\rm CSW2}$  and  $M_{\rm CSW3}$ 

pull their drain nodes close to the voltage of  $\overline{V_{\text{CTRL}}}$  before switching to the subthreshold region, where resistance is again high. The source and drain nodes of  $M_{\text{CSW1}}$  are pulled higher than the gate, further increasing the OFF-state impedance of the network's primary switch.  $M_{\text{CSW2}}$  and  $M_{\text{CSW3}}$  are sized significantly smaller than  $M_{\text{CSW1}}$ , minimizing the loading while increasing the OFF-state impedance of the switch.

In the proposed oscillator, this switched capacitor bank architecture is repeated for 5 binary-weighted bits of capacitive tuning, allowing fine frequency tuning in addition to the inductive band selection. Analog tuning can be accommodated by the addition of analog varactors capable of spanning the frequency range between the discrete frequency values. Because the varactor required for this purpose is relatively small, this presents minimal loading to the oscillator tank and does not significantly impact oscillator performance.

Control of the relative polarity of the two oscillator cores is achieved through the switch network shown in Fig. 9(b). If  $V_{\rm SW}$  is low,  $M_{\rm SW2}$  and  $M_{\rm SW3}$  are turned ON, while  $M_{\rm SW1}$  and  $M_{\rm SW4}$  present a high impedance.  $M_{\rm SW2}$  and  $M_{\rm SW3}$  conduct pulling the right oscillator formed by  $M_3$  and  $M_4$  into antiphase oscillation pattern relative to the left oscillator formed by  $M_1$  and  $M_2$ . Conversely, when  $V_{\rm SW}$  is high,  $M_{\rm SW1}$  and  $M_{\rm SW4}$  are ON, while  $M_{\rm SW2}$  and  $M_{\rm SW3}$  are OFF, pulling the right oscillator into an in-phase oscillation relative to the left. To ensure low ON-state impedance for the MOSFET switches, a secondary 1-V digital  $V_{\rm DD}$  is used to control the gate voltages of  $M_{\rm SW1-4}$ .

At first glance, these MOSFETs behave similar to signal path switches. In the short transient following a transition of *V*<sub>SW</sub>, the MOSFETs will conduct current between the two oscillator tanks. This creates a temporary loss mechanism due to the resistance of the switches. However, the phase of the two oscillators quickly locks into the relationship dictated by the switch network and the switch control voltage. After this short transient, the voltage across the switches will be approximately zero, and little current will be exchanged between the two oscillator cores [26]. The symmetry of the proposed oscillator ensures that the current required to maintain fixed relative phase is small. Of course, some device mismatch is inevitable, and the loss of the switch network will depend on the matching between the two oscillators [27].

The symmetry of the proposed oscillator topology ensures minimal dependence on ground and power connection parasitic effects. Because the M1 and M2 and M3 and M4 pairs each operate as individual cross-coupled pairs, top-to-bottom symmetry (as drawn in Fig. 9) is guaranteed for both evenand odd-mode operations. Therefore, a virtual ground plane is located horizontally across the vertical midpoint of the layout shown in Fig. 5 in both the operational modes. Odd-mode operation introduces a second virtual ground plane between the left and right halves of the circuit. However, the original symmetry is not compromised, and the oscillator remains insensitive to ground parasitics. Because of this, inadvertent excitation modes are avoided.

It is worth noting that the introduction of a second oscillator core does effectively double the power consumption compared to a traditional single band oscillator. The oscillator behaves effectively like two distinct driving elements with each with a distinct resonant tank. Therefore, startup conditions for each half are similar to those of a standard single-core oscillator, giving doubled aggregate power consumption. However, two benefits result from the presence of two independent cores which largely offset this cost. First, as will be discussed shortly, symmetrically coupled oscillators can offer a reduction in phase noise, effectively counteracting the increased power consumption. Second, because two distinct negative transconductance cores drive each tank, careful system design can leverage both outputs of the oscillator.

# A. Phase Noise of Coupled Oscillators

As discussed above, the switches which control the relative oscillation polarity of the two oscillator cores do not present a significant load on the resonant tanks when the two oscillators are closely matched. However, when mismatch between the tank's resonant frequency or behavior of the active devices is present, current exchanged between the coupled oscillators can present a significant loss term. Mismatched standalone oscillation frequency results in frequency pulling, under which both oscillators operate at some offset from the ideal resonant frequency of the tank. As in the phase noise presented in quadrature VCOs (QVCOs), this frequency pulling presents an effective degraded tank quality factor [28], [29] and corresponding degradations in power consumption, signal output power, and phase noise result.

The presence of two independent oscillators presents an opportunity for significantly improved phase noise. As discussed in [30], N tightly coupled oscillators can reduce expected phase noise by a factor of 1/N. Some efforts [30], [31] to capitalize on this improved phase noise have been conducted with sophisticated coupling networks and multiple coupled oscillators. The proposed topology, however, maintains a simple coupling architecture and compact layout while introducing coupling between the two oscillator halves. The two oscillators in the proposed design afford a corresponding 3-dB reduction in phase noise. Because FoM accounts for both phase noise and power consumption, the 3-dB increase in power consumption is theoretically offset by the improved phase noise of the coupled architecture. Furthermore, the proposed inductor presents minimal area overhead and no degradation in quality factor of the inductor. In this way, the proposed dual-band oscillator introduces no circuit performance degradation while facilitating dual-band operation.

# V. EXPERIMENTAL RESULTS

The proposed signal source circuit was fabricated in a standard 65-nm CMOS process. The nominal  $V_{\rm DD}$  of this process is 1 V, and this supply voltage was used for all digital control circuitries. The oscillator was designed to cover both Ka-band frequencies for 5G applications and a lower K-band frequency band for frequency division to standard ISM and cellular communications bands. To facilitate measurement with laboratory equipment, an open drain buffer is used at one of the outputs of the oscillator. The frequency bands covered by these ranges demonstrate the capabilities of the

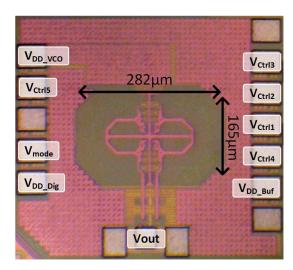


Fig. 10. Chip photograph of the fabricated VCO. The oscillator consumes a silicon area of 0.046 mm<sup>2</sup> (165  $\mu$ m × 282  $\mu$ m).

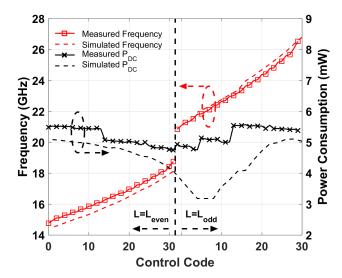
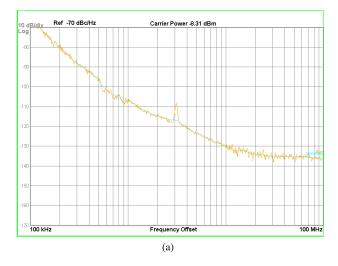


Fig. 11. Measured frequency and power consumption across the tuning range. The lower band ranges from 14.8 to 18.7 GHz, and the upper band ranges from 20.8 to 26.6 GHz.

dual-band oscillator architecture for modern communications applications, but the design is applicable to frequency bands spanning the mmWave spectrum. The chip photograph is shown in Fig. 10. Large bypass capacitors were used for decoupling of the dc supplies and, to a lesser extent, control voltages applied to the pads.

The oscillator occupies a small silicon area of  $0.046 \text{ mm}^2$  ( $165 \mu\text{m} \times 282 \mu\text{m}$ ), demonstrating the benefit of a single multiband oscillator design over implementation of multiple single-band oscillators.

The proposed oscillator was measured using a Keysight PXA 9030A signal source analyzer. The open-drain buffer is biased using an external bias-Tee, the output of which is connected directly to the signal source analyzer. A drain bias voltage of 0.75 V was used. The PXA 9030A was used to measure both frequency and phase noise directly from the output of the oscillator. The frequency of oscillation and power consumption are shown in the left and right axes of Fig. 11, respectively. The low- and high-frequency bands



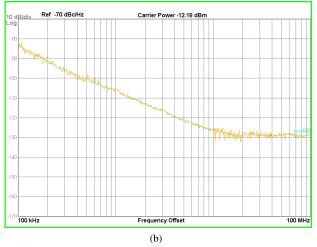


Fig. 12. Measured phase noise versus offset frequency at 16.2 GHz (a) and 23.6 GHz (b). Phase noise was measured directly using a Keysight N9030A. Supply noise at 3 MHz can be seen coupled into the phase noise as a result of supply modulation, but is not inherent to the oscillator performance.

span 14.8–18.7 and 20.8–26.6 GHz, respectively. The power consumption ranges from 4.8 to 5.6 mW and does not change significantly based on the excitation mode for the dual-path inductor. The low power consumption demonstrates the high Q of the proposed inductor under both even- and odd-mode excitations

$$FoM_T = FoM - 20 \cdot \log_{10} \left( \frac{2 \cdot (f_{\text{max}} - f_{\text{min}})}{f_{\text{max}} + f_{\text{min}}} \right). \quad (13)$$

The phase noise of the proposed dual-band oscillator was measured using the Keysight 9030A at 2- and 10-MHz offset. Fig. 12 shows measured phase noise versus offset frequency at 16.2- and 23.6-GHz center frequencies, and Fig. 13 shows the measured phase noise versus center frequency. At 10-MHz offset, the phase noise ranges from -122.5 to -130.4 dBc/Hz. The oscillator demonstrates low phase noise and power consumption, while the proposed inductor structure effectively doubles the achievable tuning range of the oscillator over traditional capacitive tuning techniques. Furthermore, the phase noise is not significantly different in the even-mode

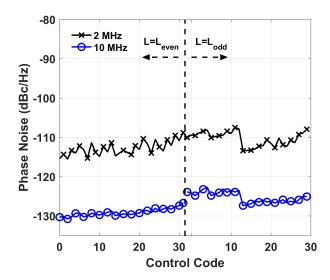


Fig. 13. Measured phase noise at 2 and 10 MHz across the tuning range. Because the inductor maintains a high Q in both states, the phase noise is relatively stable across the frequency range.

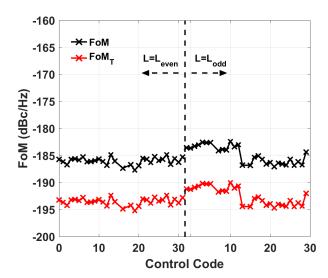


Fig. 14. Measured FoM, calculated according to (1), and tuning-range FoM (FoM $_T$ ), calculated according to (13) using the phase noise at 10-MHz offset.

(low-frequency band) and odd-mode (high-frequency band) excitations.

Fig. 14 shows the FoM and tuning-range FoM (FoM $_T$ ), as calculated by (1) and (13), respectively. In (13),  $f_{\rm max}$  and  $f_{\rm min}$  are the highest and lowest frequencies of each frequency band. The FTR of the low and high bands is calculated using these values. The FoM accounts for tuning range in addition to power consumption, phase noise, and frequency by including an FTR term corresponding to the entire range of the oscillator. The oscillator achieves a 3.9- and 5.8-GHz absolute tuning range of the low and high bands, corresponding to a 23.3% and 24.5% tuning range in the low- and high-frequency bands, respectively.

Table I compares the performance of the proposed dual-band VCO with the state-of-the-art K- and Ka-band oscillators from recent publications. The oscillator demonstrates a comparable

Reference	Technology	f <sub>c</sub> (GHz)	FTR (%)	PN @ 1MHz (dBc/Hz)	$\mathbf{P_{DC}}$ (mW)	FoM (dBc/Hz)	FoMT (dBc/Hz)
[32]	180nm CMOS	16.1/17.0	7.5/4.7	-107/-105*	5.4/7.2	-185/182*	-182/-175*
[33]	180nm CMOS	10.7/22.0	7.6/8.0	-115.9/-106.8**	15.2	-184.6/-181.81**	-182.2/-179.9**
[34]	90nm CMOS	20.8	4.8	-117.2*	3.0	-195.6*	-185.4*
[35]	90nm CMOS	19.19	8.2	-114.1*	3	-194.99*	-193.1*
[36]	$0.13\mu m$ SiGe	19.76	9.8	-112.0 <sup>†</sup>	58	-196.2 <sup>†</sup>	-195.3 <sup>†</sup>
[37]	$0.18\mu m$ SiGe	24.36	15.3	-107.7*	8.2	-186.9*	-190.6*
[38]	$0.13\mu m$ SiGe HBT	22.7	17.0	-114.0	18	-188.57	-193.18
[39]	55nm CMOS	20.7	19.3	-118.6**	55	-187.52**	-193.24**
[40]	$0.13\mu \text{m CMOS}$	17.2	23.3	-111.5	51.4	-179.05	-186.40
[41]	45nm CMOS	24.75	24.8	-101	40	-172.85	-180.74
This Work	65nm CMOS	16.75/23.7	23.3/24.4	-108/-106.6*	4.8	-187.6/-187.2*	-195.1/-194.9*

TABLE I

COMPARISON OF MEASURED RESULTS WITH THE STATE-OF-THE-ART SIGNAL SOURCE CIRCUITS

FoM to other state-of-the-art oscillators and shows improved performance compared to dual-band oscillators in the recent literature. As discussed in Section IV, this is a result of the counteracting cost and benefit of including two distinct oscillator cores. The simple architecture composed of cross-coupled NMOS pairs ensures that power consumption is low, and the two-core structure reduces phase noise. The outstanding FoM<sub>T</sub> of the proposed oscillator demonstrates the possibilities afforded by the proposed dual-path phase-switched inductor.

#### VI. CONCLUSION

A compact, low-loss, dual-path phase-switched inductor suitable for mmWave transceiver subblocks is proposed which leverages the relative phase of excitation signals to determine the inductor's signal path, allowing a wide inductance range in a compact structure. In a 2.5-D electromagnetic simulation of a representative design, the proposed structure demonstrates a 91% FTR and a quality factor above 25 in both states. The proposed dual-path phase-switched inductor facilitates dual-band operation of a wide variety of transceiver subblocks. Because the proposed inductor relies only on the relative phase of input signals, inductors in mmWave amplifiers, mixers, oscillators, and matching networks can be replaced with the proposed inductor to facilitate the dual-band operation.

The proposed inductor was leveraged to design a Ka-band oscillator in a standard 65-nm CMOS technology. The oscillator demonstrates a frequency range from 14.8 to 18.7 GHz and from 20.8 to 26.6 GHz, and the state-of-the-art phase noise, power consumption, and FoM are maintained across the oscillator's tuning range. The two bands demonstrate that measured aggregate FTRs of 23.3% and 24.5% and phase noise of -115.1 dBc/Hz at 2-MHz offset are demonstrated, and the oscillator consumes a minimum of 4.8 mW, resulting in tuning-range FoM of -195.1 and -194.9 dBc/Hz. The proposed inductor and dual-band oscillator demonstrate the potential for high-performance, inductively tuned, dual-mode mmWave circuits for frequency-reconfigurable mmWave transceiver design.

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<sup>\*:</sup> Peak performance; \*\*: Average performace across frequency band; †: Worst performance.

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