BodyWire: A 6.3-pJ/b 30-Mb/s −30-dB SIR-Tolerant Broadband Interference-Robust Human Body Communication Transceiver Using Time Domain Interference Rejection

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***Abstract*— Human body communication (HBC) utilizes the human body as the communication medium between devices in and around the body, providing an energy-efficient, secure alternative to radio wave communication traditionally used in body area networks (BAN). However, the human antenna effect results in the human body picking up environmental interference affecting HBC transmissions. Most state-of-the-art HBC transceivers utilize narrowband modulation techniques to communicate using frequencies, which are not affected by interference. In this article, we use capacitive termination and voltage mode communication techniques to utilize the human body as a broadband (BB) communication channel enabling as a BB HBC. An integrating dual data rate (I-DDR) receiver utilizing time-domain interference rejection (TD-IR) through integration and periodic sampling is used for interference-robust BB HBC operation. The proposed receiver can achieve higher energy efficiency as it utilizes the full bandwidth of the body for data transmission and does not require any modulation/ demodulation. The BB HBC transceiver is fabricated in the TSMC 65-nm technology. Measurement results show 6.3-pJ/bit energy efficiency at a data rate of 30 Mb/s with −30-dB signal-to-interference ratio (SIR) tolerance, making it 18× energy efficient compared with state-of-the-art HBC transceivers.**

***Index Terms*— Body coupled communication (BCC), human body communication (HBC), integrating dual data rate (I-DDR), interference tolerant, time-domain signal interference rejection, transceiver.**

I. Introduction

DECADES of scaling following Moore's law has led to the exponential decrease in the cost and size of unit computing. This has enabled the development of small form factor wearable, implantable devices that reside in and around the body. These devices communicate among each other to form a network of devices around the body commonly referred to as the wireless body area network (WBAN). Radio frequency electromagnetic waves are the communication method of choice for these devices to communicate among themselves. However, the proximity of these devices to the human body along with the body's electrical conductivity properties can be utilized to use the human body as the electrical communication medium between these devices. This has led to the development of human body communication (HBC) also commonly referred to as body coupled communication (BCC). HBC provides potential advantage compared with wireless radio wave communication in terms of energy efficiency and security as shown in Fig. 1. First, The human body provides a lower loss channel compared with the wireless media. Second, the human body can be potentially used as a broadband (BB) channel for communication, alleviating the need for modulation at the transmitter end and demodulation at the receiver end. These provide the energy efficiency advantage of HBC compared with wireless radio wave communication. Moreover, in wireless radio wave communication, the transmitted signal is radiated isotropically and can be snooped by a nearby malicious attacker. However, in HBC, the signals are primarily contained within the human body and can only be snooped by an attacker only if the attacker comes in extremely close proximity with the person or physically touch the person. This enables the enhanced security property of HBC, as compared to radio wave communication. These key potential advantages of HBC make it an attractive alternative

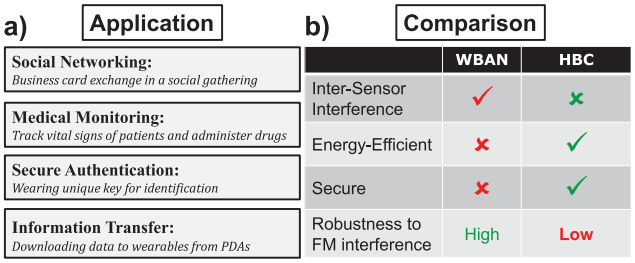

Fig. 1. (a) Possible application scenarios of HBC. (b) Comparison of the advantages and disadvantages of HBC over radio frequency WBAN [17].

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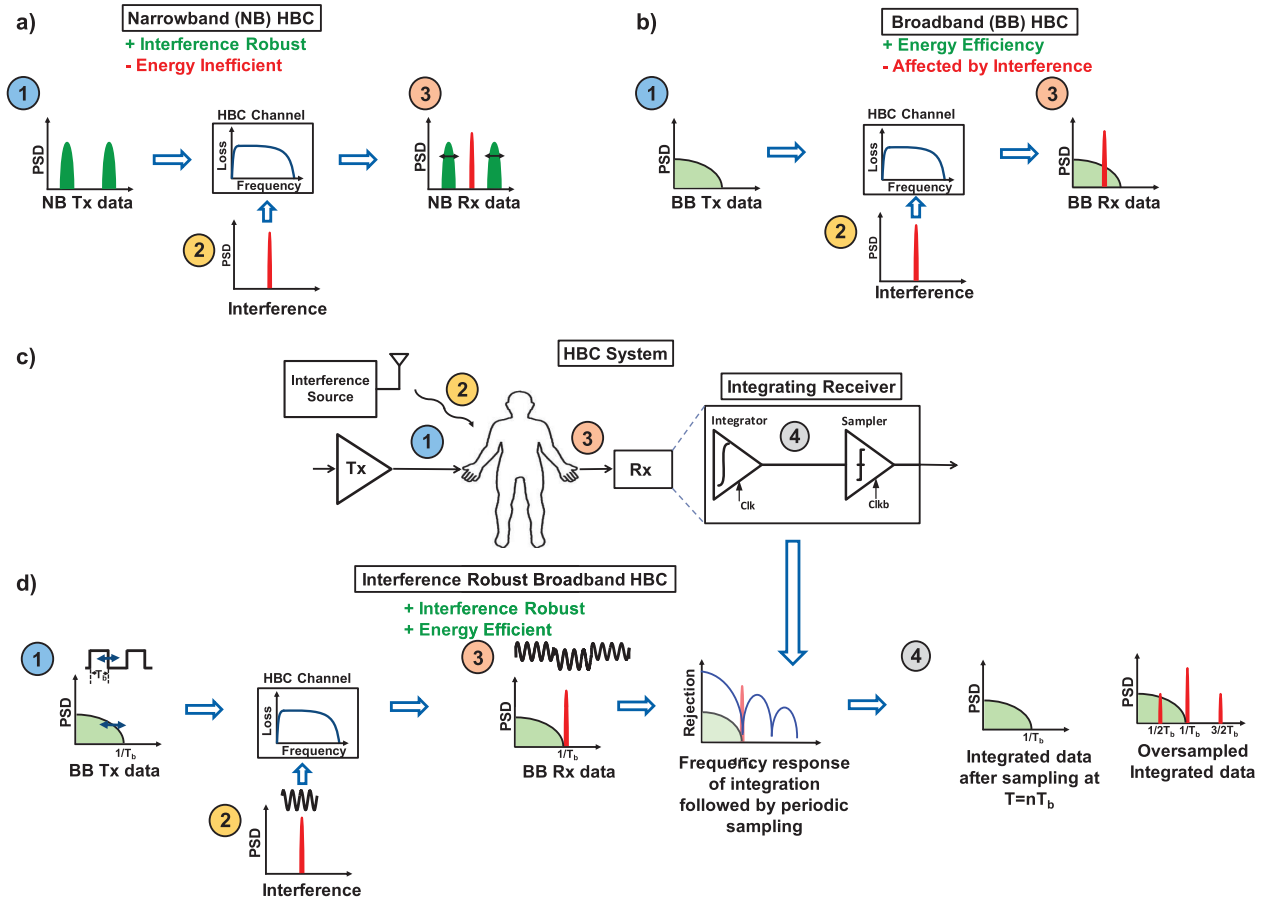


Fig. 2. (a) Frequency spectrum of narrowband data, narrowband interference showing its effect on narrowband HBC. (b) Frequency spectrum of BB data, narrowband interference showing the effect of interference in BB HBC. (c) System-level diagram of HBC showing how interference gets added to transmitted data through the human body. (d) If we adjust the data bit period to match the null of the frequency response of the data with the interference frequency and then pass it through an integrative receiver with a notch around the interference frequency, the complete data can be recovered. This will enable interference-robust BB HBC which is more energy efficient than narrowband HBC.

to radio wave communication as the communication medium of choice in BAN.

There are a few key challenges involved in designing an HBC-based WBAN system. The human body acts as an antenna in a wide frequency range. As a result, any interference present in the environment in this frequency range gets picked up by the human body. This interferes with any data communication going on within the body creating a bottleneck for HBC. Previous studies have tried to alleviate this problem by using narrowband modulation, which transmits and receives HBC data in a frequency band not affected by interferences either adaptively [1] or through pre-characterization [2]. In this article, we propose to use the body as a BB communication channel, like a wire, to enable high energy efficiency HBC. Hence, choosing an interference-free narrowband channel is not a possible solution for BB HBC. Hence, we present the integrating dual data rate (I-DDR) HBC receiver, which uses integration followed by periodic sampling to achieve interference-robust BB HBC operation. The proposed receiver provides $>100\times$ energy efficiency compared to wireless communication protocols and $18\times$ energy efficiency compared with state-of-the-art HBC systems. The enhanced security and energy efficiency property of HBC can be utilized to enable applications such as physiological health monitoring, secure authentication, data exchange between computer and wearable devices, inter-personal information exchange during a social gathering [3], and so on (Fig. 1).

The rest of this article is organized as follows: Section II looks into some of the previous work on HBC transceivers. Section III explains the key techniques that need to be followed to enable BB HBC. Section IV discusses the theory of interference-robust BB HBC, and Section V describes the design of the I-DDR receiver. The measurement results showing interference robustness of the receiver are presented in Section VI. Section VII discusses the safety aspect of HBC, with conclusion and summary of our contributions provided in Section VIII.

II. Related Work

Previous state-of-the-art HBC transceivers primarily employ narrowband techniques for data transmission by utilizing channels free of interference, as shown in Fig. 2(a). Cho *et al.* [2] present a dual-wideband full-duplex HBC transceiver that works on two frequency bands of 40-MHz bandwidth (BW) centered around 40 and 160 MHz. The FM interference problem is solved by choosing the operating frequency band of the transceiver away from the FM frequency band. The proposed transceiver achieves 79-pJ/bit receiver energy efficiency and

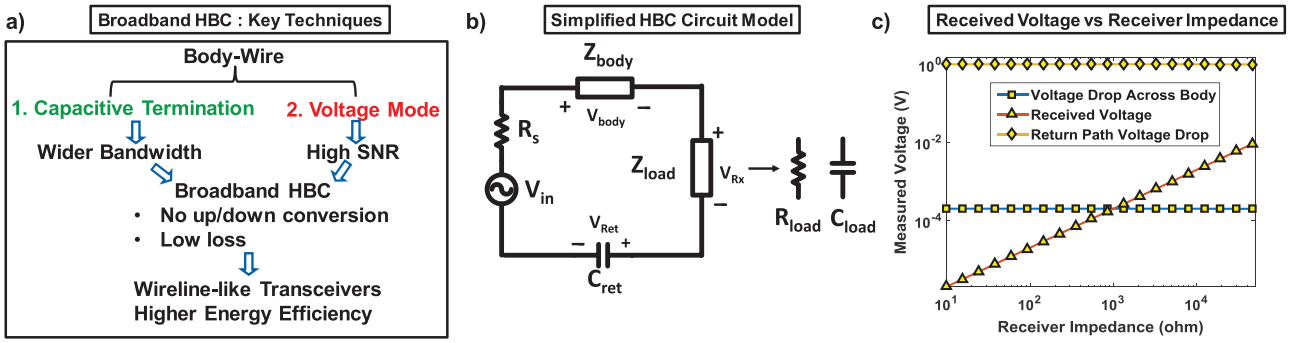


Fig. 3. (a) Key techniques enabling BB HBC leading to higher energy efficiency. (b) Simplified HBC circuit model showing the body impedance, receiver impedance, and return path capacitance. (c) Voltage drop across different components of the model for a 1-V transmitted voltage at the transmitter end.

32.5-pJ/bit transmitter energy efficiency at 80-Mb/s data rate. Lee *et al.* [4] proposed a wideband HBC transceiver that enables a 60-Mb/s data rate using three-level Walsh coding. The proposed receiver uses BB HBC transmission and can achieve interference-robust operation only in robust mode with a separate band-stop filter but not operating at the maximum data rate. Cho *et al.* [1] present a four-channel frequency hopping scheme in the 30–120-MHz frequency band for communication through frequency-shift keying (FSK) with an adaptive data rate from 60 kb/s to 10 Mb/s. The channel conditions are dynamically monitored to send the data through a clean channel, free of interference. The proposed receiver achieves an energy efficiency of 370 pJ/bit. Bae *et al.* [5] propose a double FSK modulation-based transceiver in 180-nm technology utilizing contact impedance sensing (CIS) and resonance matching (RM) to enhance body channel quality and achieve an energy efficiency of 240 pJ/bit. Saadeh *et al.* [6] propose a pseudo-orthogonal frequency division multiplexing (P-OFDM) based transceiver with contact impedance monitoring and compensation at both the receiver and transmitter end. The digital logic blocks for signal processing are also designed to minimize gate count and power consumption, achieving a receiver and transmitter power consumption of 1.1 and 0.87 mW, respectively, for a data rate of 2 Mb/s. In this work, we implement BB HBC by utilizing the human body as a wire-like channel [Fig. 2(b)] using an integrating receiver [Fig. 2(c)] for interference-robust operation [Fig. 2(d)]. It is interesting to note that the oversampling of the integrated waveform does not provide interference rejection. Sampling of the integrated waveform only at a proper rate provides interference rejection.

III. Key Techniques: Broadband Capacitive Voltage Mode HBC

In this article, we utilize the human body as a BB communication channel. To that end, certain system-level design choices have to be followed. The two key techniques for enabling BB HBC [Fig. 3(a)] are: 1) capacitive termination at the receiver end and 2) voltage mode transmitter and receiver operation [9], [10].

A. Capacitive Termination

In capacitive HBC, the return path between the transmitter and the receiver is formed through a capacitance. The channel loss is primarily determined by the impedance at the load end and the return path capacitance. From the simplified HBC circuit diagram in Fig. 3(b), considering a resistive load, with load impedance and return path impedance considerably higher than the forward path components, the channel loss is obtained as follows:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{s}{s + \frac{1}{R_{\text{load}} C_{\text{ret}}}}. \tag{1}$$

Hence, any resistive termination at the receiver end will result in the creation of a pole formed through the load resistance and the return path capacitance ($R_{\text{load}}C_{\text{ret}}$). The "pole" frequency depends on the value of the resistive termination and will result in higher loss at low frequencies. Hence, the human body cannot be used as a BB channel with resistive termination at the receiver end. Several previous studies [11]–[16] have used low resistance termination at the receiver for channel measurements. On the other hand, with a capacitive termination at the receiver end, the channel loss can be expressed as follows:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{\frac{1}{sC_{\text{load}}}}{\frac{1}{sC_{\text{load}}} + \frac{1}{sC_{\text{ret}}}} = \frac{C_{\text{ret}}}{C_{\text{load}} + C_{\text{ret}}}. \tag{2}$$

The channel loss is primarily determined by the ratio of load capacitance and return path capacitance, which is constant over different frequencies. Hence, through capacitive termination at the receiver end, the human body can be used as a BB channel, which passes all frequencies equally. Hence, the receiver needs to be designed such that the input impedance is primarily capacitive.

B. Voltage Mode Operation

In voltage mode operation, the system is designed to optimize voltage transmission from the transmitter to the receiver end. To optimize voltage mode operation the transmitter requires low source impedance and the receiver termination impedance is required to be high. The overall HBC channel loss from the simplified model, considering all the forward path components, is

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{Z_{\text{load}}}{R_{\text{s}} + Z_{\text{body}} + Z_{\text{load}} + \frac{1}{sC_{\text{ret}}}} \tag{3}$$

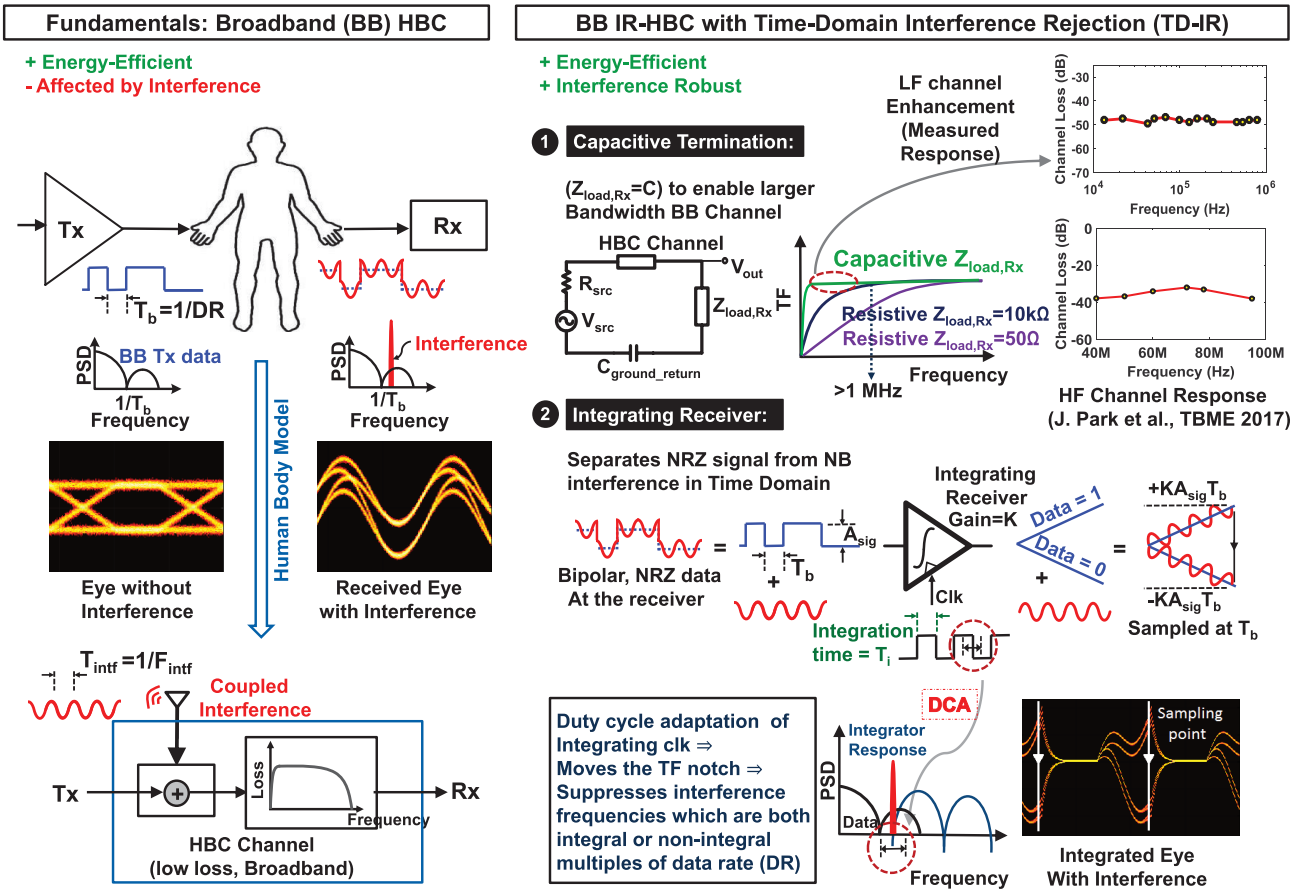


Fig. 4. Conventional BB HBC system versus implemented BB interference-robust (IR) HBC with TD-IR, enabling (1) larger BW using capacitive termination and (2) strong interference rejection using an integrating receiver with DCA.

where $Z_{\text{load}} = R_{\text{load}}$ for resistive termination and $Z_{\text{load}} = (1/sC_{\text{load}})$ for capacitive termination. From (3) it is evident that the overall channel loss will increase if $Z_{\text{body}} > Z_{\text{load}}$. Hence the termination impedance has to be higher than the body impedance, which is in the range of a few kiloohms. Fig. 3(c) also shows that as termination impedance increases, the fraction of voltage drop across it increases and will result in a lower overall loss at the system level. Similarly, a low source impedance at the transmitter end will result in most of the signal being applied at the system and minimize system loss. Hence at the transmitter end, low impedance buffers are used to drive the signal into the human body.

C. Effect: Improved Channel Capacity

The technique of capacitive termination helps us extend the BW of the human body channel. Similarly, voltage mode excitation helps in reducing the overall channel loss and maximizes the received signal amplitude due to the high receiver impedance. Hence, from (3), it is evident that the signal power is proportional to the square of the termination impedance at the receiver $P_{\text{signal}} \alpha R_{\text{load}}^2$.

The noise power for a CMOS receiver with input impedance R is obtained as $P_{\text{noise}} = 4KTR$. Hence, the noise power is proportional to the input impedance ($P_{\text{noise}} \alpha R$). So, the signal-to-noise ratio is proportional to the termination impedance ($(P_{\text{signal}}/P_{\text{noise}}) \alpha R_{\text{load}}$). Hence, having a higher termination impedance at the receiver end increases the overall signal-to-noise ratio (SNR) of the system.

The channel capacity of a system is dependent on the available BW and SNR of the system. According to Shanon's channel capacity theorem the data rate of a channel is related to its BW (B) and SNR as follows:

$$C = B * \log_2(1 + \text{SNR}). \tag{4}$$

Hence, following these two techniques, it is possible to extend the channel capacity of the system by increasing its BW and SNR. The energy efficiency of the system is also significantly increased since the whole channel BW is now utilized for data transmission and there is no overhead of frequency up-conversion and down-conversion in the transceiver.

Termination with a high impedance at the receiver end results in an impedance mismatch, which can potentially result in reflections. However, the wavelength at these frequencies (tens of megahertz) is significantly larger than the circuit dimensions, resulting in no reflections and alleviates the need for matching. Hence, it is possible to have a high impedance voltage-mode receiver in the current scenario. Also, as explained earlier, having a capacitive termination results

in extension of the channel BW. Hence, the high impedance termination at the receiver end is made capacitive. An MOS input stage provides a capacitive impedance, which can be utilized as the termination impedance at the receiver end. The capacitance of the ESD diodes connected to the input of the receiver will also determine the capacitance seen at the receiver end.

However, using the body as a communication medium for BB data transmission introduces the challenge of achieving interference-robust operation without the provision of selectively choosing a narrow band of frequency for transmission/reception, through filtering. The rest of this article discusses the design of an integrating receiver, which utilizes these two techniques along with time-domain interference rejection (TD-IR) (Fig. 4) to achieve the goal of the BB interference-robust operation.

IV. Theory of Interference-Robust Broadband HBC

A. Interference on Human Body

In the presence of electromagnetic fields, the human body acts as an antenna whose wavelength is determined by the height of the person and whether the body is grounded or not [1]. If the human body is not grounded, the wavelength is twice the height of the person, whereas a grounded body has wavelength four times the height of the person. The human body does not act as a perfect conductor and the conductance is dependent on frequency. As a result, the resonance peaking is not sharp, making the human body a BB antenna. Previous studies have mentioned this frequency range to be 40–400 MHz [1]. However, measurements results show that the human body is able to pick up interference for frequencies as lows as 1 MHz. One example of a ubiquitous interference present in this frequency range is the FM radio spectrum (88–108 MHz) and acts as one of the strongest interference source for signal transmission through HBC [1].

B. Theory of Integrating Receiver: Single Tone Interference

The integrating receiver utilizes the constant amplitude of the data signal and the periodic time-varying amplitude of the sinusoidal interference signal to separate them by integrating them over a fixed period of time. The constant amplitude data keeps on adding up as it is integrated over time. However, the periodic sinusoidal interference still remains a sinusoid even after integration. The periodic zero crossing of these sinusoids enables the possibility of sampling at appropriate instants to have zero integrated interference. The I-DDR receiver utilizes the integration, followed by periodic sampling, on periodic interference affected constant amplitude nonreturn to zero (NRZ) data to achieve interference-robust operation through signal interference separation in the time domain. The detailed mathematical analysis of the I-DDR principle on single tone interference is provided in the Appendix.

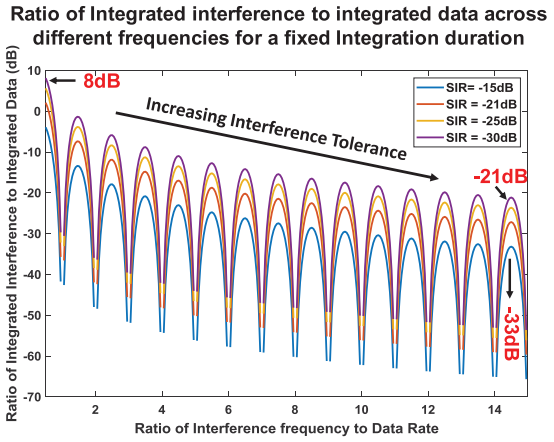


Fig. 5. Variation of residual integrated interference in a multi-tone interference scenario, as the second gone frequency is varied by keeping the first tone constant. The integration period is kept fixed such that it completely nullifies the first tone frequency. The residual interference is calculated with respect to the integrated data. It can be seen that as the second tone interference frequency increases, the residual integrated interference reduces. Also, with the increase in interference amplitude, i.e., reduction in SIR, the residual integrated interference from the second tone increases.

C. Theory of Integrating Receiver: Multitone Interference

This section builds on the theory of single-tone interference rejection principle and provides a theoretical analysis of the performance of the receiver in the presence of a multitone interference. Let us assume there are n interferences of frequencies $\omega_1, \omega_2, \ldots, \omega_n$ present together, where $\omega_n > \ldots > \omega_2 > \omega_1$

$$S_{\text{int}1} = A_1 \sin(\omega_1 t)$$
$$S_{\text{int}2} = A_2 \sin(\omega_2 t)$$
$$S_{\text{int}n} = A_n \sin(\omega_n t).$$

The integrated interference for these interferences are

$$\text{IS}_{\text{int}1} = \frac{A_1(1-\cos(\omega_1 t))}{\omega_1}$$
$$\text{IS}_{\text{int}2} = \frac{A_2(1-\cos(\omega_2 t))}{\omega_2}$$
$$\text{IS}_{\text{int}n} = \frac{A_n(1-\cos(\omega_n t))}{\omega_n}.$$

The time period of integration can be chosen such that it can completely nullify only one of the interference frequencies. Let us assume that the integration period is chosen such that $T_{\text{int}} = (2\pi/\omega_1)$. Then the sampled integrated interference at the end of the integration period is

$$\text{IS}_{\text{int}1}\left(\frac{2\pi}{\omega_1}\right) = \frac{A_1(1-\cos(2\pi))}{\omega_1} = 0$$
$$\text{IS}_{\text{int}2}\left(\frac{2\pi}{\omega_1}\right) = \frac{A_2\left(1-\cos\left(\frac{2\pi\omega_2}{\omega_1}\right)\right)}{\omega_2} \neq 0$$
$$\text{IS}_{\text{int}n}\left(\frac{2\pi}{\omega_1}\right) = \frac{A_n\left(1-\cos\left(\frac{2\pi\omega_n}{\omega_1}\right)\right)}{\omega_n} \neq 0.$$

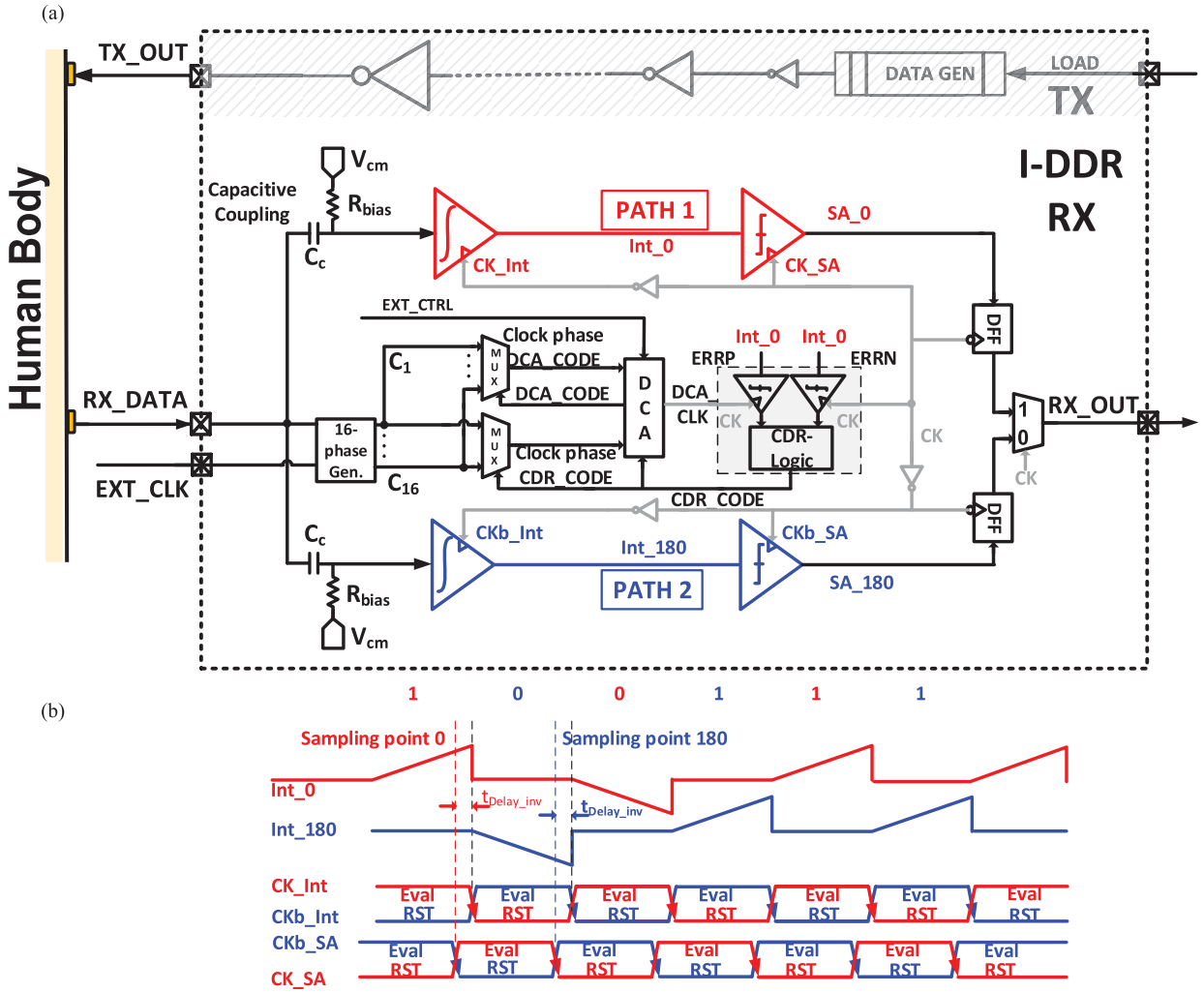
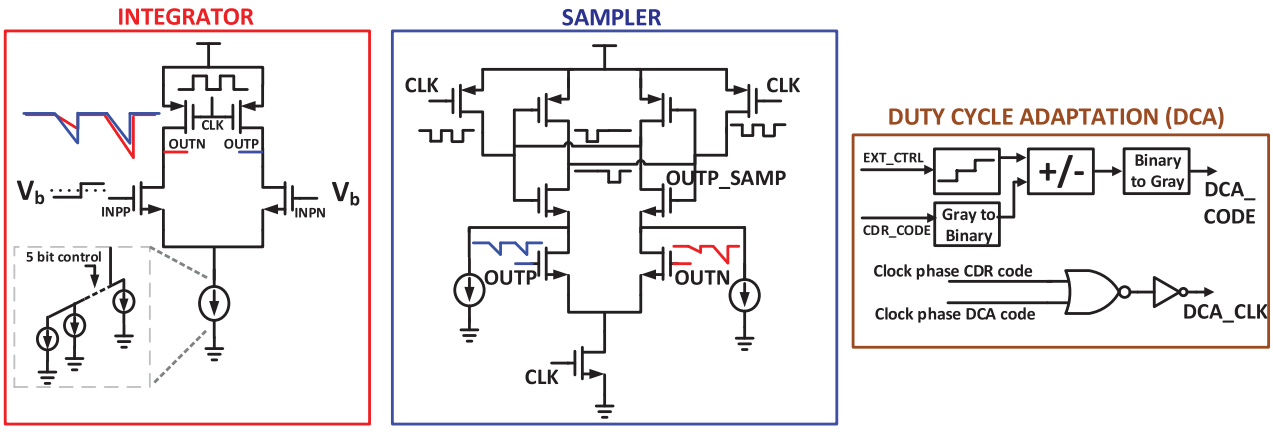


Fig. 6. (a) System-level block diagram of the integrating DDR transceiver. The receiver front end has two paths to process alternate bits, making it a DDR receiver. Each path consists of a mixed-signal integrator and sampler which uses TD-IR technique for interference suppression. The CDR, DCA, and IPD blocks are used to generate clock of appropriate frequency and phase for the receiver front end. The transmitter consists of a data generator followed by a string of buffers to drive the signal into the body. (b) System-level waveforms showing alternate reset and evaluate phases of the two paths.

The amount of residual interference at the end of the integration period is inversely proportional to the frequency of the interference. Fig. 5 shows the plot of the residual integration of the non-nullified interference versus its frequency. As the interference frequency increases, the residual integration reduces. Hence, in the presence of multiple interferences of equal strength, the integration period of the receiver should be chosen to cancel the lowest frequency interference. Even considering the worst-case signal-to-interference ratio (SIR) of -30 dB and maximum residual interference from an interference frequency greater than the locked frequency, the relative rejection of the interference compared to the integrated data is -1.5 dB. The worst-case rejection of interference compared to integrated data is -13.5 dB for an SIR of -15 dB. This shows that choosing the data rate to cancel the lowest frequency provides the best overall interference rejection property of the receiver. Also, it shows that the SIR tolerance of the receiver for a particular bit error rate (BER) performance, is dependent on the relative relation between the frequencies of the multiple interferences present.

V. Bodywire Transceiver Design: I-DDR RX Design

The bodywire transmitter couples the signal into the body through a metal electrode. Multistage buffers are used to drive the BB full-scale voltage signal into the body. The signal is transmitted through the body and picked up at the receiver end through similar metal electrodes. The signal is capacitively coupled to the receiver, which is biased in voltage mode. The interference coupled received data is integrated and sampled according to the theory of I-DDR receiver as discussed in Section IV-B. Both the integrator and sampler are mixed-signal circuits, which require a reset phase in its operation. Hence, two parallel paths enable processing of a data bit per phase of the clock and enable DDR operation. Fig. 6(a) shows the block diagram of the complete bodywire transceiver system. Fig. 6(b) shows the DDR operation with alternate reset and evaluate phase of the integrator and sampler. The two paths work on out-of-phase clocks to ensure only one of them is evaluating at a given instant. The clock to the integrator also needs to be an inverted, delayed version of the sampler clock for the sampler to sample the appropriate integrated voltage.



(a) (b) (c)

Fig. 7. (a) Circuit level implementation of the mixed-signal integrator with NMOS input stage and PMOS pre-charge switches. (b) Regenerative latch-based mixed-signal sampler. (c) DCA block to adjust the duty cycle of the integrating clock to enable variable frequency interference rejection.

Mixed-signal integration followed by sampling at the receiver front end [18] provides the notch filter response necessary for TD-IR and enables interference-robust BB HBC. The incoming BB data and the integrator clock need to be phase aligned to maximize the integrator output. This is achieved through the clock-data recovery (CDR) loop. The CDR loop utilizes multiple clock phases from the 16 phase generator to phase align the integrating clock with data. The duty cycle adaptation (DCA) block uses the CDR phase information to enable duty cycle adjustment of the integrating clock and achieve variable frequency interference rejection. The sampled value from the sampler in each path is stored in a flip-flop and then multiplexed to get the final output. We go into the detailed implementation of each of these blocks in Sections V-A–V-G.

A. Integrator

A mixed-signal clocked integrator is used for the integration operation [Fig. 7(a)]. The integrator consists of a differential NMOS input stage, which drives two PMOS load switches. During the reset phase at the negative half cycle of the clock, both the integrator outputs are precharged to VDD through the PMOS switches. During the positive half cycle of the clock period, the PMOS switches turn off and the parasitic drain capacitances at the output node start to discharge. The branch current, which is determined by the input, controls the discharge rate. The difference in discharge rate translates to a differential output voltage through the discharge of the output parasitic capacitances.

For a small signal input difference of Δv_{in}, the difference in small signal current (Δi_{out}) flowing through the two branches of the integrator is (g_{m} = transconductance of input NMOS)

$$\Delta i_{\text{out}} = g_{\text{m}}(\Delta v_{\text{in}}). \tag{5}$$

Assuming a capacitance of C_{drain} at the output nodes of the integrator, the differential output voltage through the discharge current difference is provided by

$$\Delta v_{\text{out}} = \frac{1}{C_{\text{drain}}} \int_0^{T_{\text{int}}} g_{\text{m}} \Delta v_{\text{in}} dt = \frac{g_{\text{m}}}{C_{\text{drain}}} \Delta v_{\text{in}} T_{\text{int}}. \tag{6}$$

Equation (6) shows that the differential output voltage is proportional to the transconductance of the input stage and inversely proportional to the capacitance at the output node.

B. Sampler

A mixed-signal regenerative feedback-based sampler [Fig. 7(b)] is used for sampling the output of the integrator. The sampler consists of a differential NMOS input stage, which steers current between the two branches of the sampler depending on the applied input values. A back-to-back inverter-based regenerative feedback latch is used to perform the sampling operation. At the negative half of the clock, both outputs of the sampler are precharged to VDD. During the positive half cycle, both the inverter output nodes start to discharge through the input NMOS stage branches, whose discharge rate is controlled by the input. This difference in discharge rate along with the regenerative feedback enables the latching operation to either direction. It is possible to create positive/negative offsets of different value in the sampler by steering current away or into the branches through a parallel path.

C. Clocking Relation Between Integrator and Sampler

To ensure proper operation of the integrating front-end, appropriate clock phase relationship has to be maintained between the integrator and sampler. From the basic operation of the integrator and sampler, it is evident that both of them operate only during the positive half cycle of the clock and are reset during the other half. However, the sampler has to sample the integrator output only after the completion of the integration period. So the integrator and sampler should have alternate EVALUATE phases, which requires them to have out-of-phase clocks. Also, it is necessary that the sampler samples the integrator output just before the completion of the integration period, as shown in Fig. 6(b). To ensure this, the sampler clock needs to be inverted, delayed, and applied to the integrator. The simulated waveforms of one path of the front-end are shown in Fig. 8, showing alternate Reset and Evaluate phases of the integrator, sampler, and also the time delay between the inversion of the sampler and integrating clock to ensure sampling at the end of the integration period.

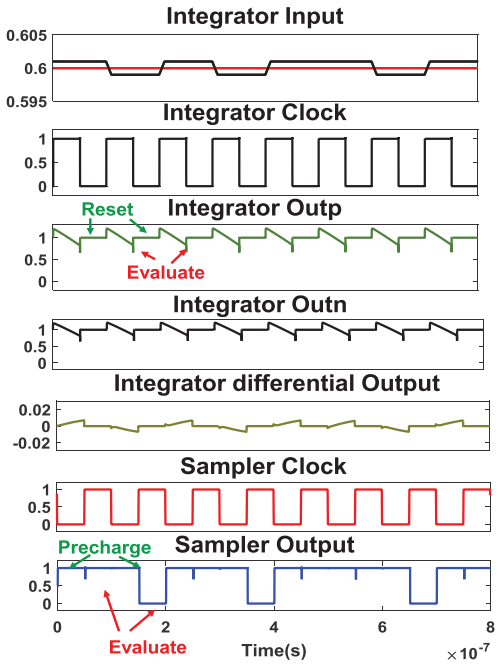


Fig. 8. Simulation waveforms from one path of the integrating front end. The differential output from the integrator is a positive or negative ramp depending on whether the input bit is 1 or 0 during the evaluation period. The integrator and sampler clocks are almost 180° out of phase and have the appropriate delay between them to ensure that the integrator output is sampled at the end of the evaluate period. The sampler output also goes through alternate pre-charge and evaluate phase.

D. Clock-Data Recovery

The integration operation has to start at the beginning of the data bit period to maximize the integrated output voltage and subsequently the eye opening at the receiver end. Therefore, it is necessary to continuously maintain a proper phase relation between the data and the integrating clock. This is similar to a wireline receiver, where the clock phase needs to sample the incoming data bit in the middle to ensure sampling at a point with maximum eye opening. This is typically done through a CDR circuit. A Mueller–Muller (MM) [19] baud rate CDR is used in this particular design to maintain appropriate phase relation between the data and integrating clock. Due to the integrating nature of the front-end, the CDR operation for the I-DDR receiver is different from a traditional wireline receiver. In the integrating scenario, the CDR needs to maintain a 0° phase difference between the clock and the data so that the integration starts at the beginning of the data period. In a wireline receiver, the sampling clock period has to be at the middle of the data bit, resulting in a 180° phase difference. Also, in the I-DDR receiver, any phase mismatch gets directly and proportionally translated into a reduction in voltage margin due to the integration operation, emphasizing the requirement of a CDR circuit.

The MM-CDR requires only one data sample per clock period for CDR operation, hence not requiring an oversampled clock. Two additional error samplers are required to provide necessary error information for the CDR operation. The output of these two error samplers and the data output is used to generate early/late information, which provides phase mismatch

Mueller-Muller CDR : Integrating Front-end

D(n-1)	D(n)	E(n-1)	E(n)	Error Information
0	1	0	1	LATE
1	0	0	1	LATE
0	1	1	0	EARLY
1	0	1	0	EARLY

$$Errp = 1\ if\ v > +V_{ref}, 0\ if\ v < +V_{ref}$$
$$Errn = 1\ if\ v < -V_{ref}, 0\ if\ v > -V_{ref}$$
$$E(n) = Errp(n) \oplus Errn(n)$$
$$D(n) = current\ data\ bit, D(n-1) = previous\ data\ bit$$

Fig. 9. Truth table of MM baud rate CDR for an integrating front end. Errp and Errn are the error information generated from the two error samplers. The final clock-data phase information can be extracted from two consecutive error and data bit information.

information between the data and the clock. The truth table for the MM-CDR is shown in Fig. 9, which is the same as that of a non-integrating receiver. The CDR early/late information is used to either advance or delay the integrating clock to maintain proper phase relation with incoming data.

E. Duty Cycle Adaptation

DCA is required to achieve variable frequency interference rejection by changing the integration duration while keeping the data rate fixed. Through duty cycle adjustment, the goal is to achieve interference rejection of frequencies, which are a non-integral multiple of the data rate. Hence, the integration duration has to be reduced compared with a 50% duty cycle clock in order to achieve variable frequency interference rejection. Logical OR operation between different generated clock phases can be used to create non-50% duty-cycled clock. The generated clock is directly applied to the sampler, which is then inverted and applied to the integrator as has been discussed in Section VI-C. The logical OR operation between multiple clock phases [Fig. 7(c)] will create a resultant clock which has a duty cycle >50%. This clock, when inverted and applied to the integrator, creates the necessary <50% duty-cycled clock. The appropriate clock phases required for the OR operation is determined by the CDR and through external scan control. This can also be achieved through automatic detection of the interference period through an interference period detector (IPD) and subsequently adjusting the duty cycle of the integrating clock to match the time period of the interference. The interference is amplified to generate a square wave of corresponding frequency and the integration duration is adjusted by comparing the ON-time of the clock and interference through time-to-voltage conversion.

F. Receiver Input Bias String

As discussed previously in Section III, one of the key constraints of BB HBC is high impedance capacitive termination at the receiver end. To ensure this constraint is maintained until low frequencies, the impedance of the input bias string at the integrator is required to be very high (> tens of megaohms). To enable that we use a series of pseudo-resistors to implement the input bias string. Under nominal condition the voltage across each pseudoresistor is around

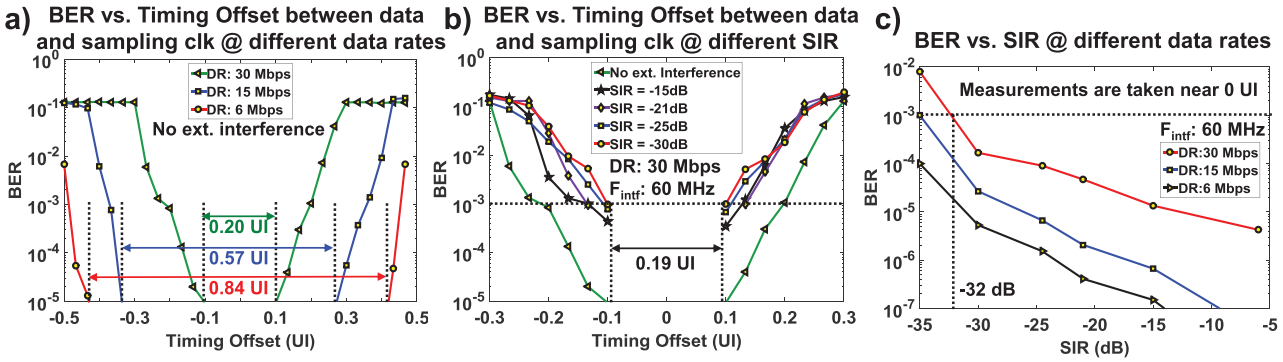


Fig. 10. (a) Plot showing BER versus timing offset between data and clock (bathtub curve) for different data rates without the presence of any interference. Lower data rates show higher timing offset tolerance. (b) Measured bathtub curve in the presence of 60-MHz CW interference for a data rate of 30 Mb/s. The receiver shows −30-dB SIR tolerance with 0.19 UI opening (BER level 10^{-3}). (c) BER versus SIR measurement for different data rates, showing higher interference tolerance (lower BER) for lower data rates.

50 mV for a supply voltage of 1 V. However, taking into care the dynamic conditions with input signal coming in (max amplitude ∼30 mV), a simulation is carried out to measure the resistance provided by the pseudoresistor with the 100-mV voltage across it. The results show that the minimum impedance provided by the bias resistance is ∼158.4 MΩ, which provides significantly higher impedance (1.59 MΩ) compared to the input capacitance (∼1 pF) even for a frequency of 100 kHz, satisfying the capacitive termination constraint.

However, this comes with two key tradeoffs: 1) the settling time of the dc bias string will be high and 2) the low cutoff frequency of the input bias string will result in more effect of flicker noise from the electrode or channel, which can hurt the sensitivity of the receiver.

The slow settling of the dc bias could pose a challenge only when the receiver is turned on and off frequently, for example in a duty-cycled scenario. This can be solved by having a low resistance bias path during reset for fast settling of the bias points. In general, BB receivers (e.g., wireline) tend to have worse sensitivity than narrowband receivers (wireless). However, the capacitive termination reduces the low-frequency loss from ∼90–100 to ∼40–50 dB, which reduces the sensitivity significantly compared to the sensitivity hit due to additional flicker noise from low cutoff frequencies, allowing higher received SNR and wide BW.

G. Transmitter Design

In BB HBC, the signal is transmitted as 1/0 bits and do not require any modulation at the transmitter end. This simplifies the design of the transmitter as there is no requirement for frequency up-conversion. As discussed earlier, since we are doing voltage mode HBC, the output impedance of the transmitter also needs to be minimized to maximize signal transmission. Keeping these design constraints in mind, the transmitter consists of a chain of inverters, driving the data signal into the transmitter electrode, which couples it into the body.

The data can be generated by two methods: 1) externally loading into the registers of the transmitter and 2) programmable PRBS generator which can generate PRBS sequences of different orders (PRBS 5, 7, 11, 15, 31). The maximum supported data rate for this receiver is 30 Mb/s, which is less than the BW of the human body (close to 100 MHz [20], [21]). Hence, there is no band limitation of the transmitted signals and it is not necessary to have any equalization at the transmitter end.

VI. Measurement Results

The proposed BB I-DDR receiver has been fabricated in TSMC 65-nm CMOS technology with an active area of 0.122 mm^2. The die is wire-bonded to a PCB for measurements. The interference robustness of the receiver is determined by measuring the BER under the presence of interference of different types [continuous wave (CW), AM, FM, multitone and different amplitude (varying SIR).

A. BER Performance With CW Interference

Fig. 10(a) shows the BER bathtub curve of the receiver for different data rate of operation, with varying timing offset between the data and the receiver clock in the absence of any external interference. It can be seen that, for the same timing offset, the BER increases as the data rate increases. The horizontal opening of the bathtub curve also decreases for higher data rates. For the highest data rate of 30 Mb/s, a 0.2UI eye opening is achievable for a BER limit of 10^{-5}. To test the interference robustness of the receiver, CW interference of varying amplitude is applied, keeping the data rate fixed at 30 Mb/s. BER measurements show [Fig. 10(b)] a horizontal bathtub curve opening of 0.19UI (BER limit 10^{-3}) in the presence of a CW interference of 60-MHz frequency and an SIR of −30 dB. Fig. 10(c) shows the BER versus SIR performance of the receiver for different data rates. As the SIR reduces (less signal, more interference), BER increases for all data rates. Consistent with the earlier experiments, the BER for higher data rate operation is more under the same interference condition. It can also be seen that until 30-Mb/s data rate the BER is $<10^{-3}$ even in the presence of interference with an SIR of −30 dB. Extrapolating the measurement results linearly shows interference tolerance of −32 dB for a BER of 10^{-3} even at the highest data rate of 30 Mb/s.

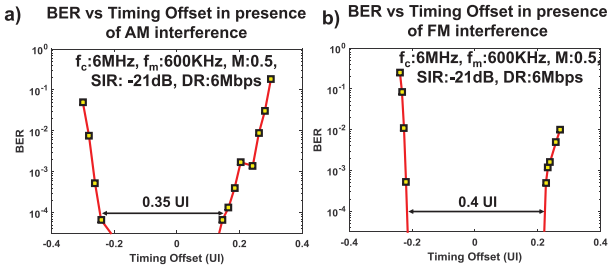


Fig. 11. Bathtub curve in the presence of (a) AM interference and (b) FM interference.

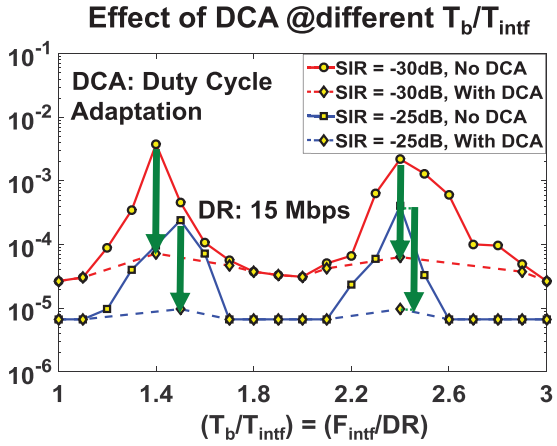


Fig. 12. Interference rejection property of the receiver under varying interference frequency (frequency response), showing lower interference tolerance (higher BER) for interference frequencies which are a non-integral multiple of the data rate. DCA reduces the BER for these scenarios by adjusting the duration of integration.

B. BER Performance With AM and FM Interferences

Fig. 11(a) shows the bathtub curve of the I-DDR receiver in the presence of AM interference of modulation frequency = 600 kHz, carrier frequency = 6 MHz and modulation index = 0.5. The receiver performance under FM interference of 6-MHz carrier frequency, 600-kHz modulation frequency, and 0.5 modulation index is shown in Fig. 11(b). The bathtub curve shows a 0.4 UI horizontal opening for FM interference and 0.35UI opening ($<10^{-4}$ BER) in the presence of AM interference. This shows the tolerance of the I-DDR receiver to AM and FM interferences.

C. BER Performance With DCA

In the presence of interferences that are not an integral multiple of the data rate, the sampled integrated interference is not zero at the end of the integration period. As a result, the BER performance of the receiver degrades in the presence of interferences of such frequencies. Fig. 12 shows the BER at the receiver end, as the ratio between the interference frequency and the data rate is varied from 1–3, keeping the data rate fixed at 15 Mb/s. As can be seen, for non-integral ratios such as 1.5 or 2.5, the BER is almost two orders of magnitude more than the case for integral ratios of interference to the data frequency. However, by adjusting the duty cycle of the integrating clock to an appropriate value through DCA, the BER can be significantly improved even for non-integral relation between interference and data rate. This validates the theory of variable frequency rejection through DCA while keeping the data rate fixed. It is also interesting to note that even without DCA, the BER of the receiver in the presence of −25-dB SIR interference is $<10^{-3}$ for all different non-integral ratios of interference frequency and data rate. This shows the efficacy of integration followed by periodic sampling operation to achieve interference robustness.

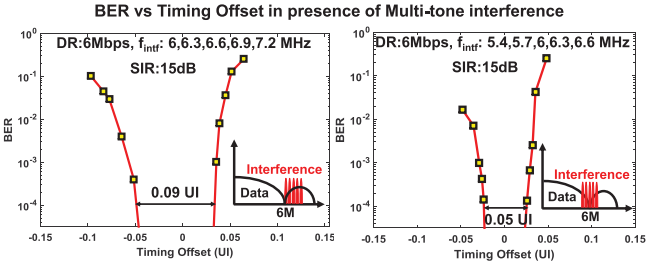


Fig. 13. Bathtub curve in the presence of multitone (five tones) interference. (a) Interference frequencies only higher than the data rate. (b) Interference frequencies both higher and lower than the data rate.

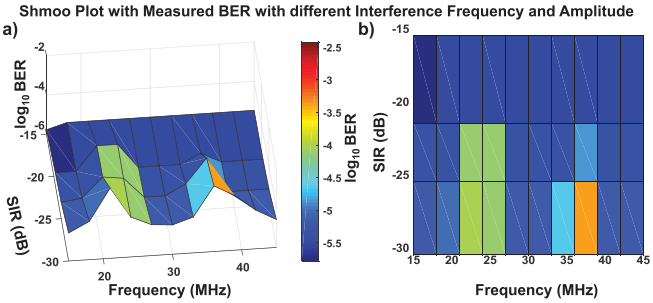


Fig. 14. Shmoo plot showing the variation of measured BER in the presence of interference of varying frequencies and amplitude (different SIR) for a data rate of 15 Mb/s. (a) Surface plot showing the BER variation. (b) 2-D projection of the surface plot.

D. BER Performance for Multitone Interference

In the previous experiments, we have looked into the performance of the I-DDR receiver in the presence of a single frequency. Here we look into the efficacy of the proposed I-DDR receiver in the presence of multiple interferences of different frequencies. The data rate is fixed at 6 Mb/s and interference of five different frequencies [6, 6.3, 6.6, 6.9, 7.2 MHz for Fig. 13(a); 5.4, 5.7, 6, 6.3, 6.6 MHz for Fig. 13(b)] are injected into the data transmission. Each interference corresponds to an SIR of −15 dB. The BER bathtub curve shows a horizontal opening of 0.09UI in Fig. 13(a) and 0.05 UI in Fig. 13(b) for a BER limit of 10^{-3}, showing interference rejection even in the presence of multitone interference.

In the scenario of Fig. 13(a), the data rate is chosen to reject the interference with the lowest frequency of 6 MHz. Whereas, for Fig. 13(b), two of the five interferences have a frequency lower than the frequency (6 MHz), which is set to be completely canceled by the receiver. The results show close correspondence to the theory in Section IV.

E. Frequency Response of I-DDR Receiver

The BER performance of the receiver provides a measure of its interference rejection property. A lower BER signifies high

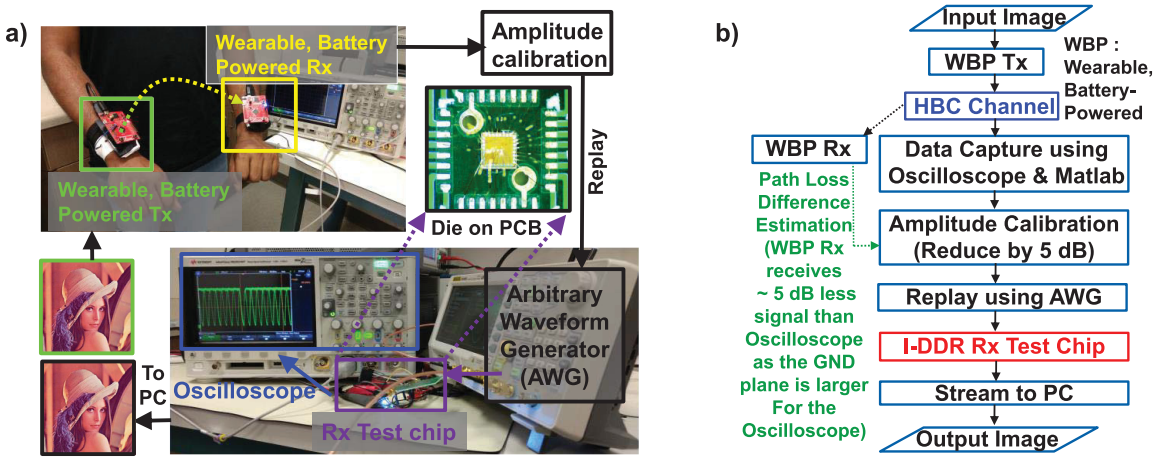


Fig. 15. (a) Experimental setup of image transfer through HBC. (b) Flowchart showing the steps used to convert the image into a stream of bits and re-playing it through an AWG by applying attenuation corresponding to channel loss. The signal amplitude is determined by measuring channel loss and recalibrating it to a wearable transmitter, receiver scenario.

interference rejection and vice versa. Hence, the frequency response of interference rejection for the I-DDR receiver can be measured by varying the interference frequency and measuring the BER in the presence of those different interferences. Fig. 12 shows the frequency response of the I-DDR receiver, showing high interference rejection with BER $<10^{-4}$ for interference frequencies which are integral multiple of data rate. The BER increases to $>10^{-3}$ for interference frequencies, which are non-integral multiple of data rate, showing a lower amount of interference rejection as expected. These results match with the simulated response presented later in the Appendix.

F. BER Variation With Interference Frequency and SIR

Fig. 14 shows the BER variation with changing interference frequency and SIR. The data rate is chosen to be 15 Mb/s and the interference frequency is varied from 15 to 45 MHz. For each frequency, the SIR is also varied to change the strength of interference. The measured BER is high for non-integral relation between the interference and data frequencies. Also as SIR reduces (stronger interference), the BER increases, as seen in other measurements also. The two peaks in Fig. 14 show the range of frequency and SIR for which the BER is high.

G. Image Transmission and Recovery

In this setup [Fig. 15(a)], an image is transmitted from an arbitrary waveform generator (AWG) to the receiver, which is then streamed to a PC for reconstruction using MATLAB. The amplitude of the transmitted signal for image transmission is determined through experimental calibration of the HBC channel. For channel measurements, a wearable battery-powered device is used for transmission and the received signal is measured on an oscilloscope. However, as reported in previous literature, HBC channel measurements show lower loss when measured with ground connected instruments. To compensate for this, the channel loss is recalibrated for the scenario of a wearable transmitter and wearable receiver as reported in [8] and [20]. The signal amplitude of the AWG is determined assuming a transmission voltage of 1 V at the transmitter end, going through a channel loss of a wearable-wearable measurement scenario. The image is digitized and the corresponding bit stream is transmitted from the AWG, with proper channel attenuation, to the receiver. The receiver decodes the incoming signal and the received bit stream is transferred to a computer and the image is reconstructed through MATLAB. The peak signal-to-noise ratio (PSNR) of the received image is found to be >50 dB showing a BER $<10^{-5}$. The steps followed for amplitude recalibration and image transmission is shown in the flowchart of Fig. 15(b).

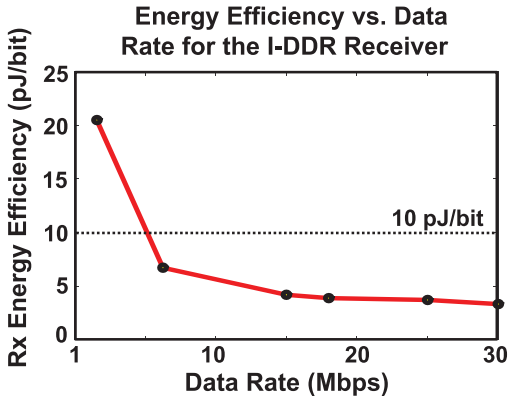


Fig. 16. Plot of receiver energy efficiency over different data rates, showing higher energy efficiency with the increasing data rate.

H. Energy Efficiency

Fig. 16 shows the energy efficiency of the receiver for different data rates. The static dc power consumption of the receiver front-end components (integrator bias current, sampler offset generation current, etc.) does not scale linearly with the data rate. Also, the leakage power is independent of the data rate of operation. As a result, the energy efficiency of the receiver reduces for lower data rates, with the maximum energy efficiency of 3.27 pJ/bit for the maximum data rate of 30 Mb/s.

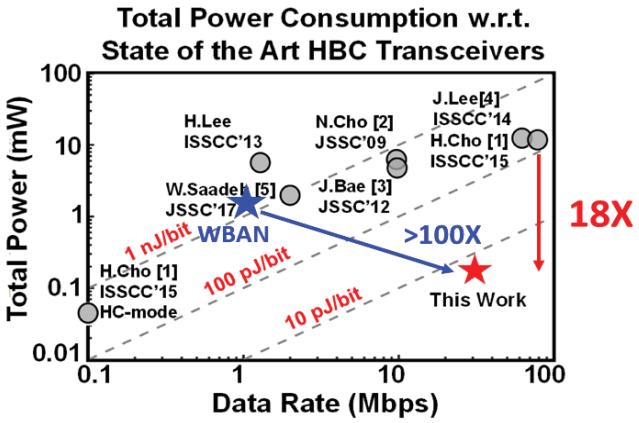


Fig. 17. Comparison of the proposed I-DDR transceiver with other state-of-the-art HBC transceivers in terms of total power and data rate. The proposed transceiver is the only transceiver to show <10-pJ/bit energy efficiency, making it 18× energy efficient than the state-of-the-art HBC transceivers.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH RELATED LITERATURE

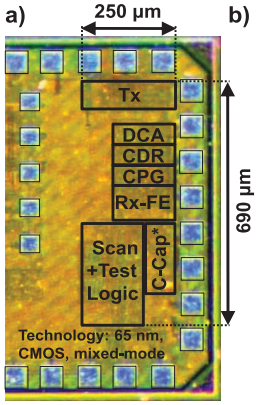
	N.Cho JSCC '09	J.Bae JSSC '12	J. Lee ISSCC '14	H. Cho ISSCC '15	W. Saadeh JSSC '17	This Work
Process	180nm CMOS	180nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Supply Voltage	1	1	1.1	1.2	1.1	1
Modulation	AFH FSK	Double FSK	3-Level Walsh Coding	Coherent BPSK	8 P-OFDM BPSK	NRZ
Maximum Data Rate	10Mb/s	10Mb/s	60Mb/s	80Mb/s	2Mb/s	30Mb/s
Tx Power	2.4mW	2mW	1.85mW	2.6mW	0.87mW	93uW
Rx Power	3.7mW	2.4mW	9.02mW	6.3mW	1.1mW	98uW
Energy/bit (Tx)	240pJ/b	200pJ/b	31pJ/b	32.5pJ/b	435pJ/b	3.1pJ/b
Energy/bit (Rx)	370pJ/b	240pJ/b	150pJ/b	79pJ/b	550pJ/b	3.27pJ/b
SIR (@ 10^{-3} BER)	-28dB	-20dB	-20dB	NA	NA	-30dB
Sensitivity	-65dBm @ 10^{-5} BER	-62dBm @ 10^{-5} BER	-58dBm @ $<10^{-5}$ BER	-58dBm	-83.1dBm @ 10^{-3} BER	-63.3*dBm @ 10^{-3} BER
Input Impedance	<100 Ω	100-600 Ω	10KΩ	–	>> 50Ω	22* KΩ, (Capacitive)
Area (mm^2)	2.3	12.5	1.12	5.93	0.542	0.122
Interference Robust	Yes	Yes	Yes#	No	No	Yes
Broadband	No	No	Yes	No	No	Yes

In robust mode using a separate band-stop filter, not at the highest data rate

* Capacitive input termination, input impedance calculated at the Nyquist frequency of 15MHz corresponding to highest data rate of 30Mbps. Sensitivity corresponding to 6mV input swing for this input impedance

I. Comparison With the State-of-the-Art HBC Transceivers

Table I shows the comparison of the proposed HBC transceiver with other state-of-the-art HBC transceivers. Other than [4], all the previous designs [1], [2], [5], [6] use a narrowband modulation technique for signal transmission. At the peak data rate of 30 Mb/s, the proposed receiver achieves an energy efficiency of 3.2 pJ/bit and the transmitter has an energy efficiency of 3.1 pJ/bit, making the overall transceiver energy efficiency 6.3 pJ/bit. This is an 18× improvement over the previously reported best HBC transceiver energy efficiency of 111.5 pJ/bit [2] and a >100× improvement over state-of-the-art wireless transceivers (Fig. 17), which achieves an energy efficiency of 1 nJ/bit. For a BER of 10^{-3}, the



Block	Sub-block	Power @30Mbps
Rx	Integrator + Sampler (RX-FE)	9µW
	Clock Data Recovery (CDR)	20µW
	Duty Cycle Adaptation (DCA)	5µW
	Clock Phase Generation (CPG)	64µW
Tx		93µW
Total		191µW

Block	Area
(Rx-FE)+CDR+DCA+CPG+(C-Cap)	0.102 mm^2
Tx	0.02 mm^2

*C-Cap: 250 fF AC coupling cap for RX-FE input

Fig. 18. (a) Die micrograph showing the I-DDR transceiver fabricated in 65-nm CMOS technology. (b) Power and area breakdown of different blocks.

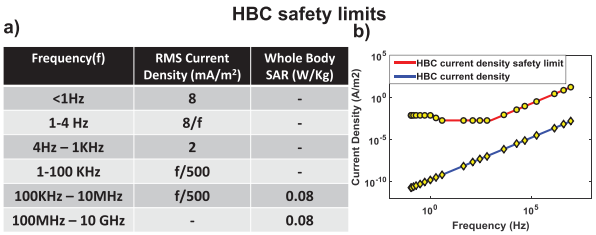


Fig. 19. (a) HBC safety limits according to ICNIRP guidelines. (b) Plot showing the comparison of the current density from simulated HBC circuit model [8] and the actual safety limits, showing >1000× margin in safety limits in terms of current density even at the worst case.

proposed receiver also achieves an interference tolerance of −30 dB, which is higher than other interference-robust HBC transceivers. The input impedance of the receiver is made capacitive to provide wider BW as discussed in Section IV. The input capacitance at the receiver is primarily determined by the ESD diodes connected to the signal input pin. The input impedance of the receiver is 22 kΩ at the Nyquist frequency of 15 MHz, corresponding to the maximum data rate of 30 Mb/s. The sensitivity of the receiver is calculated using this value as the input impedance of the receiver. The proposed transceiver also has an active area of 0.122 mm^2, which is a 4× improvement compared to state-of-the-art HBC transceivers. The die micrograph and the area breakdown of the individual blocks are shown in Fig. 18.

VII. HBC SAFETY

In HBC systems, the impact of signal transmission through the human body and its safety limits must be carefully addressed. The International Commission on Non-Ionizing Radiation Protection (ICNIRP) [7] provides the exposure limit of non-ionizing radiation for humans. Depending on the frequency of the field, different physical quantities are used to set the restriction of exposure. For frequencies in 1 Hz–10-MHz range, current density provides the restriction to prevent effects on the central nervous system. In the 100 MHz–10-GHz range, restrictions are provided on specific energy absorption rate (SAR) to prevent heat stress on the body. Between the

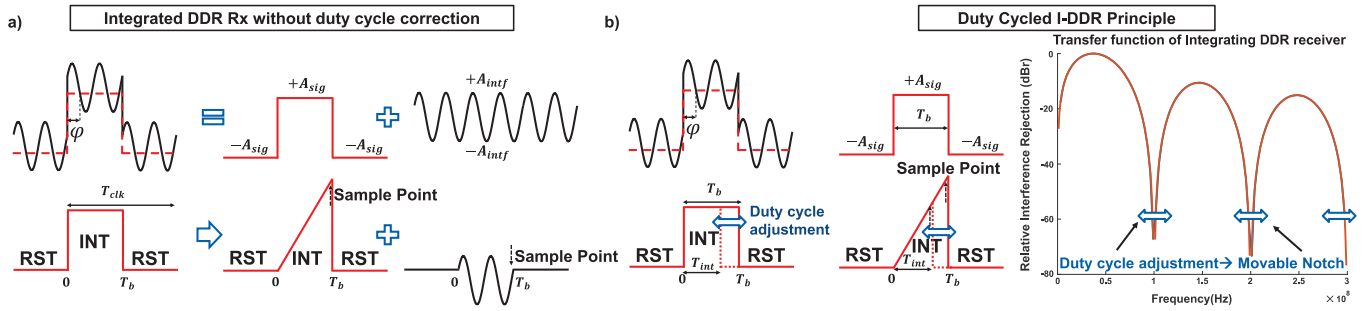


Fig. 20. Working principle of the I-DDR receiver [3]. (a) Data signal affected by sinusoidal interference is divided into a linear superposition of square wave data signal sinusoidal interference. Integration clock waveform showing alternate integration and reset period. The data signal gets integrated into a ramp signal, increasing over time. The sinusoidal interference gets integrated into a sinusoid, which if sampled at $T_b = nT_i$ (shown for $T_b = 2T_i$) will provide an integrated interference of 0. (b) Principle of variable frequency rejection through DCA. The integration duration can be varied by changing the duty cycle of the integrating clock, which translates to movable notches in the frequency response, enabling variable frequency interference rejection.

10 GHz–300-GHz frequency range, power density is restricted to prevent heating in body tissue or near the skin surface. The limits on these restrictions are shown in tabular and graphical form in Fig. 19.

As can be seen from Fig. 19(a), the most stringent requirement on current density is in the 4 Hz–1-kHz frequency range due to the low threshold current required for nerve stimulation at this frequency range. In addition to the whole body SAR requirement provided in Table I, the restriction of localized SAR in head and trunk is 2 W/kg and limbs are 4 W/kg. Apart from these, the reference level for time-varying contact current, when the human body comes in contact with an object of different electrical potential, is provided in order to avoid shock and burn hazards. For frequency of $<$2.5 kHz, the maximum contact current is 0.5 mA, whereas for 2.5–100 kHz, the limit is $0.2f$ (f = frequency in kHz) and for $>$100 kHz, the limit is 20 mA. To find out the safety compliance of capacitive HBC, the current density in an HBC system is simulated from a capacitive HBC circuit model [8]. Fig. 19(b) shows that the current density is orders of magnitude lower ($>1000\times$ in the worst-case frequency) compared to the safety limits.

VIII. Conclusion

This article presents an interference-robust BB HBC transceiver system achieving 6.3-pJ/bit operation, making it $18\times$ more energy efficient than state-of-the-art HBC transceivers. System-level techniques such as capacitive termination and voltage mode operation are used to utilize the body as a wire-like BB channel enabling BB receiver operation. The interference robustness is achieved through an I-DDR receiver employing TD-IR technique for interference rejection. Measurement results from a 65-nm CMOS implementation of the receiver show -30-dB interference tolerance with the maximum achievable data rate of around 30 Mb/s. The receiver is able to reject variable frequency interference by using the variable rejection notches from the integrating front-end using variable duty cycle integration. However, an automatic way to move the notch and adapt in the presence of interference, taking into account its frequency and amplitude, is an area of active research and is part of future work.

Appendix

A. Theory: Time Domain Interference Rejection

An NRZ data transmission in the presence of continuous wave interference is used to explain the theory of interference-robust I-DDR receiver [3]. The received signal is a linear superposition of the NRZ data signal and a CW interference signal [Fig. 20(a)]. In HBC, the interference strength ($A_{\text{int}f}$) is significantly larger than the data signal amplitude (A_{sig}). Due to such high magnitude of interference, the eye diagram of the received signal will show a closed eye. Therefore, it is not possible to do an accurate sampling of the received signal. To solve this problem, the interference affected received signal is first integrated for the symbol-period (T_b) and then sampled. The duty cycle of the clock used for the integration operation is 50%, and a frequency half of the data rate ($T_{\text{clk}} = 2T_b$) [Fig. 20(a)]. The integrator is reset after each integration period. Therefore, two consecutive symbols are integrated using two integrators working on opposite phase clocks, leading to a DDR receiver. The received signal (S_{RX}), is the linear superposition of the desired NRZ signal (S_{sig}) and the undesired interference ($S_{\text{int}f}$)

$$S_{\text{RX}} = S_{\text{sig}} + S_{\text{int}f}. \tag{7}$$

Now S_{sig} and $S_{\text{int}f}$ can be mathematically expressed as follows:

$$S_{\text{sig}}(t) = \pm A_{\text{sig}} 0 \le t \le T_b \tag{8}$$

$$S_{\text{int}f}(t) = A_{\text{int}f} \sin(\omega_i t + \varphi) \forall t \tag{9}$$

$$\omega_i = \frac{2\pi}{T_i} = \text{Interference Frequency}$$

$$\varphi = \text{phase difference between Data and Interference.}$$

Therefore, the integrated component (IS) of the signal and interference is expressed as follows:

$$\text{IS}_{\text{sig}}(t) = \int_0^t S_{\text{sig}} = \begin{cases} \pm K_{\text{int}} A_{\text{sig}} t, & 0 \le t \le T_b \\ 0, & T_b < t \le 2T_b \end{cases}$$

$$K_{\text{int}} = \text{Integrator Gain} \tag{10}$$

$$\text{IS}_{\text{int}f}(t) = \int_0^t S_{\text{int}f} = \begin{cases} -K_{\text{int}} \dfrac{A_{\text{int}f} \cos(\omega_i t + \varphi)}{\omega_i}, & 0 \le t \le T_b \\ 0, & T_b < t \le 2T_b. \end{cases} \tag{11}$$

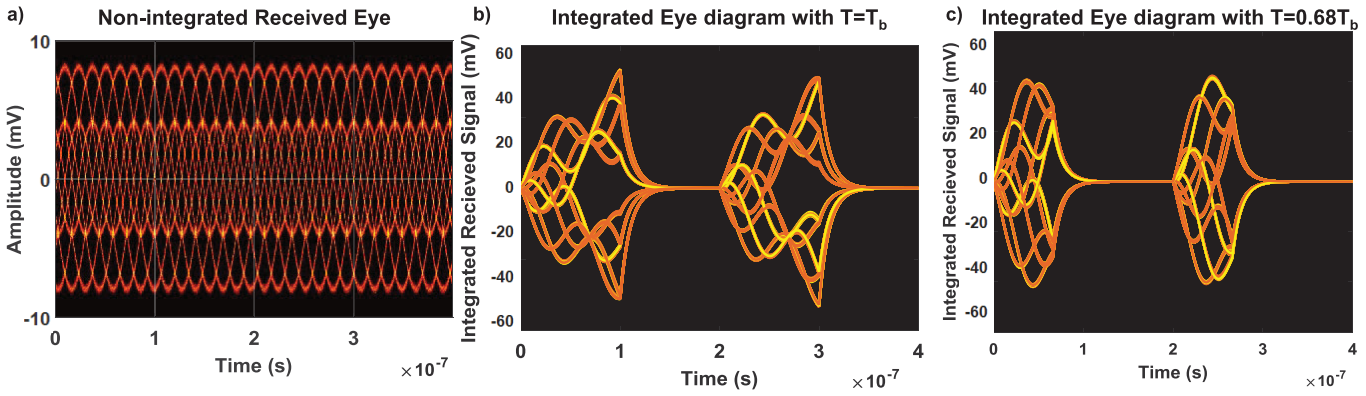


Fig. 21. (a) Simulated receiver eye diagram under a non-integrating scenario. There is no clear eye opening for the receiver to sample in the presence of interference. The interference frequency (14.5 MHz) is a non-integral multiple of the data frequency (10 MHz). (b) Eye diagram for an integrating clock of 50% duty cycle integrating for the complete data period. (c) Eye diagram for a 34% duty cycle clock showing more eye opening compared to scenario (b).

The sampled signal at the sampling instant at the end of the bit period, that is, at $t = T_b$ is obtained as follows:

$$\mathrm{IS_{sig}}|_{t=T_b} = \pm K_{\mathrm{int}} A_{\mathrm{sig}} T_b \tag{12}$$

$$\mathrm{IS_{int}}_f|_{t=T_b} = K_{\mathrm{int}} \frac{A_{\mathrm{int}f}[\cos(\varphi) - \cos(\omega_i T_b + \varphi)]}{\omega_i} \tag{13}$$

$$= K_{\mathrm{int}} \frac{A_{\mathrm{int}f}\left[\cos(\varphi) - \cos\left(2\pi \frac{T_b}{T_i} + \varphi\right)\right]}{\omega_i}$$

$$= 0, \forall T_b = nT_i; n = \text{positive integer.} \tag{14}$$

It is evident from (10) that at $T_b = nT_i$, integrated interference equals 0, for any arbitrary initial phase of interference. In other words, by choosing the bit period to be an integral multiple of the interference period [Fig. 20(a)] and sampling it at that instant, a high interference rejection is achieved. This is the fundamental basis of TD-IR, where time domain integration operation enables rejection of interference. It is important to note that the phase difference between the NRZ signal and interference do not affect the interference rejection property of the proposed I-DDR reciever.

B. Duty Cycle Adaptive Broadband HBC

To achieve maximum interference rejection according to the I-DDR operating principle described in the previous subsection, the interference frequency has to be an integral multiple of the data rate. However, any random frequency interference can be rejected while keeping the data rate the same by changing the integration period to be an integral multiple of the interference period. As a result, the integrated interference during the sampling instant is 0. This can be achieved by adapting the duty cycle of the integrating clock and adjust the ON duration to be an integral multiple of the interference period [Fig. 20(b)] [17]. The integrated signal and interference value over any time duration T_{int} can be mathematically written as follows:

$$\mathrm{IS_{sig}}(T_{\mathrm{int}}) = \int_0^{T_{\mathrm{int}}} S_{\mathrm{sig}} = \pm K_{\mathrm{int}} A_{\mathrm{sig}} T_{\mathrm{int}}$$

$$\mathrm{IS_{int}}_f(T_{\mathrm{int}}) = \int_0^{T_{\mathrm{int}}} S_{\mathrm{int}f}$$

$$= K_{\mathrm{int}} \frac{A_{\mathrm{int}f}\left[\cos(\varphi) - \cos\left(2\pi \frac{T_{\mathrm{int}}}{T_i} + \varphi\right)\right]}{\omega_i}. \tag{15}$$

Now if the time duration T_{int} corresponds to duty cycle $d = (T_{\mathrm{int}}/T_{\mathrm{clk}}) = (T_{\mathrm{int}}/2T_b)$ and $T_b = kT_i$, where k can be a non-integer, then

$$\mathrm{IS_{int}}_f(T_{\mathrm{int}}) = K_{\mathrm{int}} \frac{A_{\mathrm{int}f}\left[\cos(\varphi) - \cos\left(4\pi \frac{dkT_i}{T_i} + \varphi\right)\right]}{\omega_i}$$

$$= K_{\mathrm{int}} \frac{A_{\mathrm{int}f}[\cos(\varphi) - \cos(2\pi(2dk) + \varphi)]}{\omega_i}$$

$$= 0, \quad \forall dk = \frac{n}{2}; n = \text{positive integers.}$$

So, even for interference frequencies which are non-integral multiple of the data rate, it is possible to achieve maximum interference rejection by setting the duty cycle to be

$$d = \frac{1}{2k}, \frac{2}{2k}, \ldots, \frac{N}{2k} \quad \text{s.t. } d \le \frac{1}{2}.$$

Hence, DCA enables interference rejection even when the integral relation between the interference frequency, the data rate is not maintained and the phase difference between the data and interference shows variation across different cycles. This translates into a movable notch in the transfer function of the integrating receiver, adjustable through the duty cycle of the integrating clock, as shown in Fig. 20(b).

The advantage of DCA on receiver performance can be observed from the simulation results of Fig. 21. As a measure of received signal quality, the eye diagram at the receiver end is plotted under a scenario where the interference frequency (f_i) is a non-integral multiple of data rate (f_b) ($f_i = 1.45 f_b$). The transmitted voltage is 1 V and the channel loss is taken to be 40 dB with an integrator gain of 10. Integration over the duration of the bit period T_b results in an eye opening of ~30 mV [Fig. 21(b)], whereas integration with a duty cycle of 0.34 results in an increased eye opening of ~50 mV [Fig. 21(c)].

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