An Improved Update Rate CDR for Interference Robust Broadband Human Body Communication Receiver

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***Abstract*—Broadband Human Body Communication (HBC) enables energy efficient communication between body area network devices by utilizing the electrical conductivity property of the human body. However, environmental interference remains a primary bottleneck in its implementation. An integrating front-end receiver with resettable integration followed by periodic sampling can be utilized to enable interference robust broadband HBC. However, as required in all broadband communication systems, a Clock Data Recovery (CDR) loop is necessary to correctly sample the received data at the appropriate instant. The CDR is required to be sensitive to the clock-data phase mismatch at the receiver end and take corrective action for reducing it, similar to the CDR of a traditional receiver. In addition to that, the CDR for a broadband HBC receiver also requires to be tolerant to environmental interference. This paper analyzes the traditional Baud Rate CDR for an integrating front-end receiver and proposes a modified integrating CDR architecture with a higher update rate. Simulation results show 2.5X higher clock data frequency offset tolerance of the proposed CDR compared to the traditional Baud Rate CDR, >1.25X higher clock data frequency offset tolerance in presence of interference and >10% interference frequency offset tolerance with respect to the integration clock. The proposed CDR is also implemented in a Xilinx Spartan-3E FPGA board to validate its closed loop functionality in real time.**

***Index Terms*—Baud rate CDR, body coupled communication (BCC), broadband HBC receiver, clock data recovery (CDR), human body communication (HBC), Mueller-Muller CDR.**

I. Introduction

BODY Area Networks (BAN) in the form of wearable and implantable devices are gaining wide popularity due to their capability of performing tasks such as sensing, actuation, computation and communication with a very small form factor [1], [2]. Due to the small form factor, BANs are generally battery constrained and a large portion of the system energy is consumed in communication, thus there is a need for energy efficient systems to enhance the lifetime of these BAN devices. State of the art BANs communicate between devices on the network through radio waves. However, wireless radio communication requires signal modulation to a higher frequency at the transmitter and demodulation at the receiver which proves to be quite energy intensive. Furthermore, health care monitoring applications such as multichannel electroencephalogram (EEG), neural signal recording and implantable monitoring devices have large bandwidth requirements (for supporting 1–24 Mbps data rates) [3]–[5], favoring the use of broadband techniques. Alternatively, human body communication (HBC) may be utilized [6], where the electrical conductivity of the human body is used to communicate between BAN devices as they reside in close proximity to the body [7]. This is possible as the human body acts as a broadband channel and can be used for broadband communication, enabling higher communication security [8] and energy efficiency [9].

The primary bottleneck for broadband HBC is the interference picked up by the human body antenna effect [10]. To achieve interference robust broadband communication, an integrating Dual Data Rate (I-DDR) receiver [11]–[13] is used, which performs time domain integration to nullify the effect of interference. Since data are transmitted in a broadband manner, to recover the transmitted data at the receiver, it is necessary to sample data at proper instants, i.e., the receiver clock must maintain a certain phase relationship with the incoming data. This is achieved using clock data recovery (CDR) loop widely used for wireline receivers. However, due to the integrating front-end, the CDR operation varies from a traditional CDR.

In our previous works [11], we have performed feasibility studies of using human body as a wire-like broadband communication channel and presented the RF front-end parameters and circuit implementations. In vivo experiments validating the concept of broadband HBC in presence of interference are covered in [14]. The HBC electro-quasistatic channel model is presented in [15] in terms of resistances and capacitances along with their origins. In this paper, our primary focus is to analyze the applicability of the traditional Mueller Muller (MM) CDR [16] for an integrating front-end, as well as focus on the detailed design of an Integrating Mueller-Muller (I-MM) CDR suitable for broadband HBC. Although, the proposed I-MM CDR is applicable to general broadband systems (such as wireline receivers) affected by interference, however, we focus on broadband HBC as our current scope.

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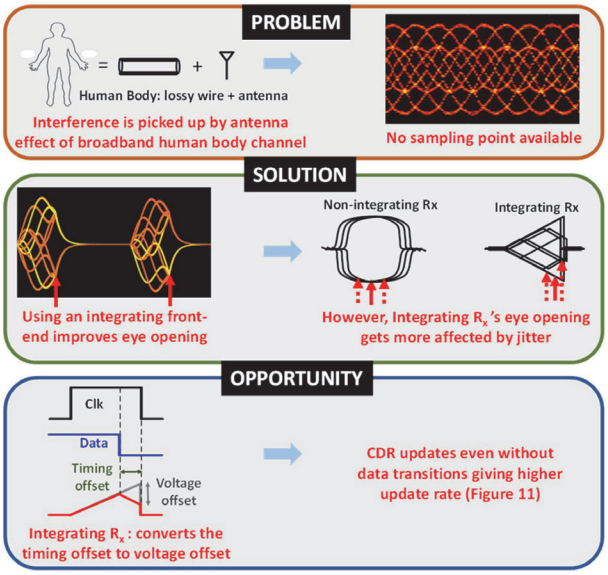

Fig. 1. Summary of the problem addressed, proposed solution and opportunity recognized in this paper.

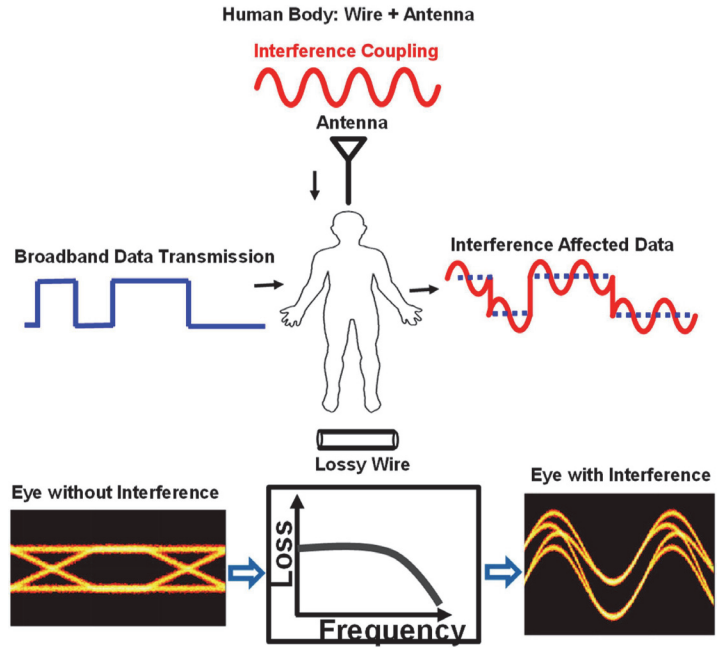

Fig. 2. Human body as a combination of a broadband wire and antenna. The body acts like a broadband channel with high impedance capacitive termination. The conductance of the human body also makes it a radiating antenna operating at a frequency determined by the height of the person. The antenna effect results in the broadband data transmission getting affected with environmental interference and resulting in a closed eye.

Fig. 1 summarizes the problem, solution and opportunity captured by this paper. The problem of interference being picked up by the human body antenna effect (when using it as a broadband channel) can be solved by using an integrating front-end receiver which provides a bigger eye opening for sampling. However, a flipside of using an integrating front-end over a non-integrating front-end receiver is the reduction in eye opening with increase in timing jitter as the sampling point in the non-integrating case lies in the middle and allows for more jitter tolerance. A consequence of using an integrating front-end receiver, is the conversion of timing offset (between the integrator clock and incoming data) to voltage offset at the integrator output, leading to CDR updates even without data transitions. The proposed I-MM CDR utilizes this higher update rate opportunity provided by the integrating front-end to improve the CDR performance.

This paper is divided into the following sections: Section I builds insight into using broadband HBC as an alternative to narrowband communication to achieve better energy efficiency, in Section II we discuss the human body as a communication channel, Section III discusses the undesirable effect of interference while employing HBC as a communication channel and provides a possible solution to achieve interference robustness in Section IV. To recover the broadband data correctly by maintaining a proper phase relation with the receiver clock, we analyze the traditional MM CDR architecture for an integrating front-end and propose a modified I-MM CDR with higher update rate in Section V. Section VI highlights the important considerations while designing an I-MM CDR followed by the simulation results in Section VII comparing the traditional and proposed CDR's performance. Hardware validation using an FPGA is done in Section VIII and the paper is concluded in Section IX.

II. Human Body: Combination of Wire and an Antenna

HBC utilizes the body as a communication medium between channel [17]–[22] with high loss at frequencies below the MHz range. However, recently it has been shown that with voltage mode signaling [11], and high impedance capacitive termination at the receiver end, it is possible to reduce the channel loss at low frequencies [14], [15], [23], [24]. As a result, the human body channel response becomes flat-band across frequencies. Hence, the human body can be utilized as a wire-like broadband channel as shown in Fig. 2, where the complete bandwidth can be utilized for data transmission. However, the channel loss provided by the body is in the range of 45–55 dB, which is significantly higher than in the case of a wire. Hence, traditional broadband wireline circuit design techniques utilized for HBC should be adapted to consider the additional loss introduced by the HBC channel. The other artifact introduced by the electrical conductivity property of the human body is the human body antenna effect. Any conductor on top of a ground plane acts as an antenna at a frequency dependent on the length and grounding of the conductor. For a grounded conductor the resonance frequency is four times its length, whereas for a non-grounded conductor the frequency is twice the length of the conductor. The human body has some electrical conductivity property and the surrounding environment acts as a big ground plane around us. Hence, the human body acts as an antenna on a frequency range dependent on the height of the person [10], [25], [26]. For example, a 2 m tall person will have resonance peak at 37.5 MHz during a grounded condition and 75 MHz for a non-grounded condition. However, the human body is a lossy conductor and is a combination of multiple layers with different conductance values. Hence, the body does not show resonance peaking

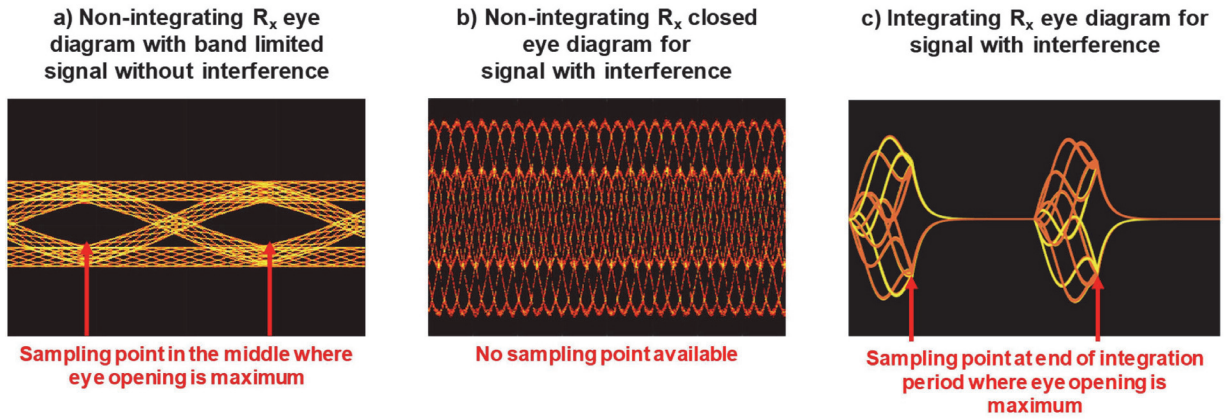

Fig. 3. Comparison of sampling points in non-integrating and integrating receivers. (a) In case of a band limited signal without interference, the eye opening is maximum in the middle of data period and is the most suitable location for sampling. (b) Presence of interference on the signal closes the eye opening. (c) By making use of an integrating front-end receiver, the eye opening is improved, and sampling is performed at the end of integration duration where the eye opening is maximum.

studies [10]. Any environmental interference present in these frequencies will get picked up by the body due to the antenna effect. This interference will affect any data transmission going on within the body [27]. Hence, along with the lossy wire-like property the human body also exhibits an antenna property. The measured in-band interferences over the range 30–150 MHz with various radio signals being injected into the human body due to the body antenna effect are provided in [10]. This necessitates the traditional wireline techniques to be further adapted for application in the interference prone lossy human body channel.

For narrowband communication, the interference problem can be alleviated by utilizing an interference free frequency band for data transmission and filtering out all the interferences present in the other frequency bands. However, for broadband signaling no such filtering techniques can be employed as it will affect the transmitted signal also. Hence, it is necessary to adjust the data rate to align its nulls with the interference frequency and then employ a filtering technique which acts as a notch filter at that frequency. This can be achieved through resettable integration followed by periodic sampling. The details of the interference robust broadband HBC circuits are provided in the next section. We especially look in depth into the effect of interference on the design of clock data recovery circuits, which is one of the key building blocks of broadband wireline systems.

III. Effect of Interference on Broadband HBC

An important criterion while designing BAN devices is energy efficiency to extend their lifetimes. Since most of the system energy is consumed in communicating between these devices, it is essential to use energy efficient communication techniques. Using broadband HBC for communication is an attractive solution due to its superior energy efficiency compared to narrowband techniques as it obviates the need for energy intensive up/down frequency conversion blocks. However, as discussed in the previous section, the human body picks up challenge in the implementation of broadband HBC receivers in BAN devices.

Thus, state of the art BAN devices resort to narrowband implementations which utilize either static frequency bands with tolerable interference [28], or measure channel quality and adaptively hop between frequency bands [10]. However, if interference robustness can be realized in broadband HBC receivers, we can achieve both a higher energy efficiency by utilizing the complete bandwidth for data transmission as well as maintain sufficient reception quality. To achieve interference robustness in broadband HBC receivers, we employ an integrating front-end [11], which provides interference robustness if a properly adjusted integration duration which is an integral multiple of the interference duration is ensured. A detailed theoretical analysis of an integrating receiver in presence of different kinds of interference (continuous wave AM and FM) has been presented in [29].

We now validate why we choose an integrating receiver over a non-integrating one, under the effect of interference. In case of a non-integrating receiver, with a band limited signal without interference, sampling is performed where the eye opening is maximum (Fig. 3(a)), i.e., in the middle of the data period. However, when the transmitted broadband HBC data is affected by interference from the human body antenna effect, the eye opening closes (Fig. 3(b)) and may result in improper sampling. Fig. 4(a) shows a non-integrating receiver scenario, where depending on the phase alignment of the interference with respect to the data (considering the interference duration to be an integral multiple of the integration period), the data may or may not be sampled correctly. In case of an integrating receiver, data is sampled at the end of integration period where eye opening is maximum (Fig. 3(c)). The receiver achieves interference rejection by integrating over a complete cycle of interference followed by reset. The integration duration is determined by the receiver's clock period and it is adjusted to be an integral multiple of the interference duration by adjusting the data rate and duty cycle of the clock. As a result, the integrated interference over a

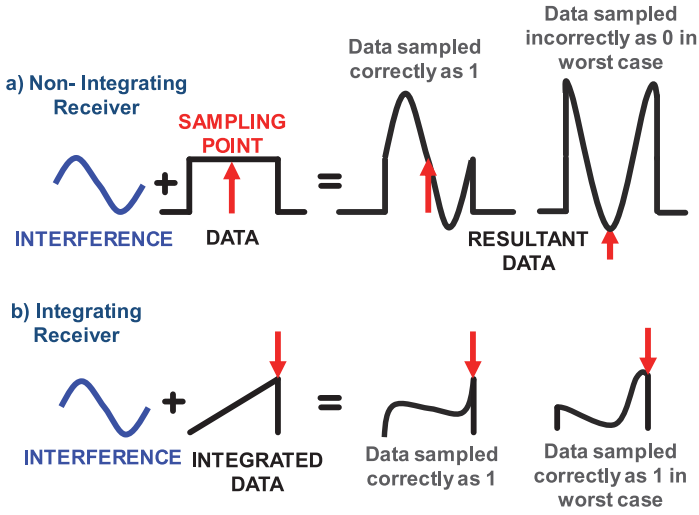

Fig. 4. Comparison of integrating and non-integrating receivers with respect to interference robustness. (a) In a non-integrating receiver scenario, it may or may not be possible to sample the data correctly with 2x interference amplitude. (b) In case of an integrating receiver scenario, data is always sampled correctly.

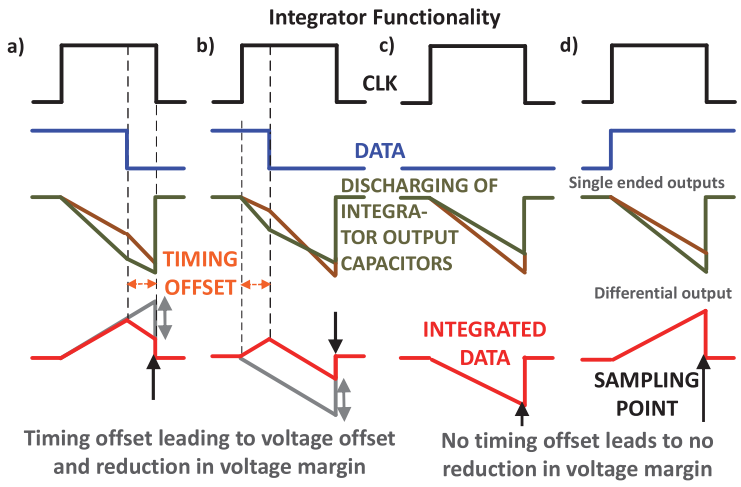

Fig. 5. Integrator functionality showing the following waveforms: integrator clock, differential input data to the integrator, parasitic capacitor voltage waveform at the output nodes and differential output from the integrator. (a) Shows reduction in voltage margin when clock is late. (b) Shows reduction in voltage margin when clock is early. (c) Integrator output reaches maximum value when data is 0 throughout. (d) Integrator output reaches maximum value when data is 1 throughout.

concept is illustrated in Fig. 4(b) which shows an integrating receiver scenario where the interference duration is an integral multiple of the integration period. Thus, the interference integrates to zero over that period. Since at the sampling point (at the end of data period), the effect of interference has been nullified, the sampler is able to sample correctly, irrespective of the phase alignment of the interference with respect to the data.

IV. Interference Robust Broadband HBC Receiver: Architecture

As discussed in the previous section, interference robust broadband operation is achieved through resettable integration followed by periodic sampling. The integrator [11] has two phases of operation, namely, reset and evaluate. Differential input is provided to the integrator which results in a linear discharge of the parasitic capacitors at the output node as shown in Fig. 5 and the differential output shows the integration functionality. It is important to note that the integrated output reaches its maximum value when the data hold their values during the integration period (Fig. 5(c,d)) whereas any phase offset between the data and integration clock is directly translated to a reduction in voltage margin (Fig. 5(a,b)). The voltage level obtained after integration is later utilized by the CDR to obtain phase mismatch information.

The integrator is followed by regenerative latch based samplers to obtain the received data information and the phase mismatch information from the integrated output. Like the integrator, sampler too has a reset phase. Thus, two parallel chains of integrators and samplers are required to process data at both phases of clock achieving dual data rate operation. The goal of the CDR is to minimize the phase mismatch between the incoming data and the receiver clock. The threshold value of the data sampler is kept at 0 threshold, while the error sampler thresholds are kept at a voltage offset of +Vref and −Vref.

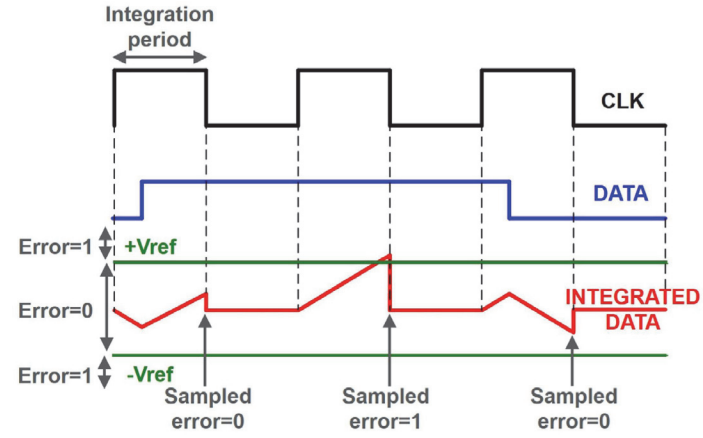

Fig. 6. Generation of phase mismatch error samples from the integrated data output.

the error samplers (+Vref, −Vref), the phase mismatch error signal in the CDR is generated as shown in Fig. 6, which in turn is used by the CDR to take corrective action on the clock ensuring alignment with the data. *It is noteworthy to mention that the CDR is able to distinguish between the low voltage level due to timing offset between the integrator clock and input data from the low voltage level due to insufficient gain of the integrator. This is achieved by setting the error sampler thresholds in accordance with the gain of the integrator such that the error value equals zero only as a result of timing offset and not due to insufficient gain of the integrator. Once the error sampler thresholds are set depending on the gain of the integrator, any timing offset between the integrator clock and incoming data gets translated to voltage offset at the integrator output leading to an error value of zero, while error value of one occurs as a result of clock aligned data or when data remains fixed (i.e., no transition) during the integration period.* Fig. 7 shows the internal details

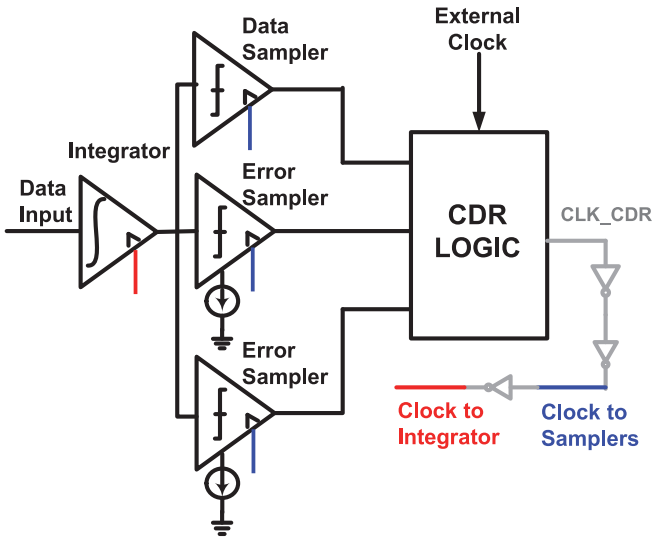

Fig. 7. System level block diagram of the I-DDR receiver. The CDR takes input from the data and error samplers to generate the phase locked clock.

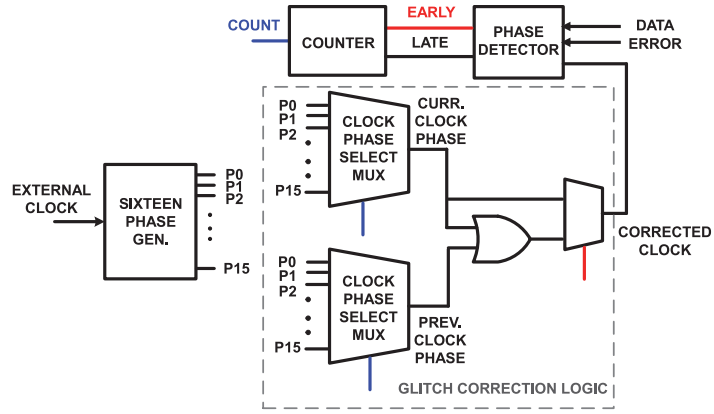

Fig. 8. Internal logic diagram of the CDR. The phase detector creates early/late updates, which chooses the correct phase of the phase generator, and passed through a glitch correction logic to generate the system clock.

the integrator gain, input data amplitude and acceptable eye opening for tolerable bit error rate (BER) as explained later in Section VI-A. A consequence of very small values of Vref is a small eye opening and very few corrective triggers to the CDR, i.e., only a large data clock phase mismatch will lead to an error transition, generating early/late updates and make the CDR to change its clock phase less frequently. On the other hand, a very high value of Vref, though has a good eye opening, has a possibility of generating too many corrective triggers, i.e., CDR's clock gets corrected very frequently as even a small clock data phase mismatch leads to an error transition, which may hamper the CDR loop stability.

A baud rate CDR is preferred over Alexander and Hogge CDR phase detectors [30], as it requires only one sample per clock period as opposed to others which require two samples per clock period. Thus, using a baud rate CDR minimizes the power overhead by 2X as the circuit now works only on one clock edge instead of both. Instead, the additional timing mismatch information is derived from the voltage domain through two extra error samplers (Fig. 5). The data and error signals obtained after the sampling stage are fed to the CDR's phase detector and decide whether the clock is early or late with respect to the data, which either increments or decrements a counter as shown in Fig. 8. A phase generator circuit generates multiple phases of the clock and feeds them to a multiplexer. The counter value is used to select a clock phase from the sixteen phases of the clock (fed to the multiplexer by the phase interpolator) which reduces clock data phase mismatch. For instance, when the clock is early with respect to the data, the counter is incremented to select the next later phase such that the clock alignment with the data improves. The sampler clock is inverted and delayed before being applied to the integrator to ensure sampling just before the end of the integration period. This sampling clock is directly provided by the corrected clock. This clocking relation is shown in Fig. 7. The phase tracking loop is implemented as a single loop CDR important step as glitches add false clock edges in the corrected clock leading to false updates (explained in Section VI-B).

V. Clock Data Recovery Architectures

In this section, we analyze the performance of the traditional MM CDR under non-integrating and integrating front-end scenarios. We identify the additional possibilities of extracting timing information due to the integration functionality, i.e., incorporation of adjacent bit information in the current integration period, and we propose an Integrating Mueller Muller (I-MM) CDR with a 2x higher update rate.

A. Mueller Muller Baud Rate CDR: Non-Integrating Receiver

MM CDR is advantageous in terms of requiring just one data sample per clock period to extract clock data phase mismatch information, as opposed to other CDR topologies such as Alexander and Hogge. Instead, it extracts timing mismatch information from the voltage domain through error samplers. The baud rate CDR takes the data and error samples as shown in Fig. 7 and generates early/late updates. Depending on the whether the clock is early or late, the counter is incremented or decremented and selects a later or earlier clock phase from the multiplexer. A gray counter is implemented for this purpose to ensure the output of the counter is glitch free. Otherwise, propagation delays in the outputs of the counter will result in spurious clock phase selection, which can result in the creation of undesired clock edges. After the phase adjustment from the CDR, the clock gets better aligned to the data. The truth table for the generation of early/late clock phase information from data and error signals for MM CDR is provided in Fig. 9. D(n) and E(n) are the current data and error bits respectively, and the current transition corresponds to the (n − 1)th and nth bits. As can be seen from the table, early/late updates are only available on data and error transitions. In turn, error transitions are only caused when there is a clock data phase mismatch and the data transitions (without data transitions, the error value remains fixed until the next data transition occurs). However, due to band

Mueller-Muller CDR : Both for Non-integrating and Integrating Front-End

D(n-2)	D(n-1)	D(n)	D(n+1)	E(n-1)	E(n)	Error Information
X	0	1	0	0	0	No Info
X	0	1	1	0	1	LATE
X	1	0	0	0	1	LATE
X	1	0	1	0	0	No Info
0	0	1	X	1	0	EARLY
1	0	1	X	0	0	No Info
0	1	0	X	0	0	No Info
1	1	0	X	1	0	EARLY

$$Errp = 1\ if\ v > +V_{ref}, 0\ if\ v < +V_{ref}$$
$$Errn = 1\ if\ v < -V_{ref}, 0\ if\ v > -V_{ref}$$
$$E(n) = Errp(n) \oplus Errn(n)$$
$$D(n) = current\ data\ bit, D(n-1) = previous\ data\ bit$$

Fig. 9. MM-CDR truth table. A 0–1 or 1–0 data transition does not necessarily contain phase error information and is dependent on the adjacent bits. This reduces the update rate of the CDR.

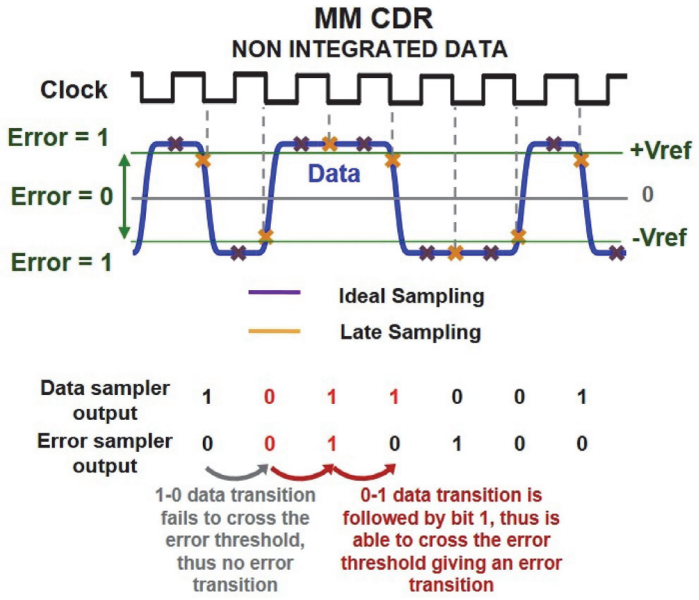

Fig. 10. MM CDR update generation in a non-integrating reciver scenario with a late clock and data sequence 1011001, creating updates at 11/00 data trasitions.

reach the error = 1 region. More precisely, error transitions are created only when data transitions are preceded by the same bit e.g., **0**01 when clock is early (where **0**, 0, 1 are D(n-2), D(n-1) and D(n) respectively) or followed by the same data bit e.g., 01**1** when clock is late (where 0, 1, **1** are D(n-1), D(n) and D(n+1) respectively), as shown in Fig. 10. For the data sequence 10**1** where the subsequent bit (D(n+1) = 1) is different from D(n)th bit (=0), due to the effect of band limitation, the D(n)th bit falls within the error = 0 region at the sampling points and fails to create an error transition. Whereas, 01**1** data pattern produces an error transition, as effect of band limitation is negligible on D(n)th bit (=1) and is able to fall in the error = 1 region. In summary, the baud rate CDR provides clock-data phase

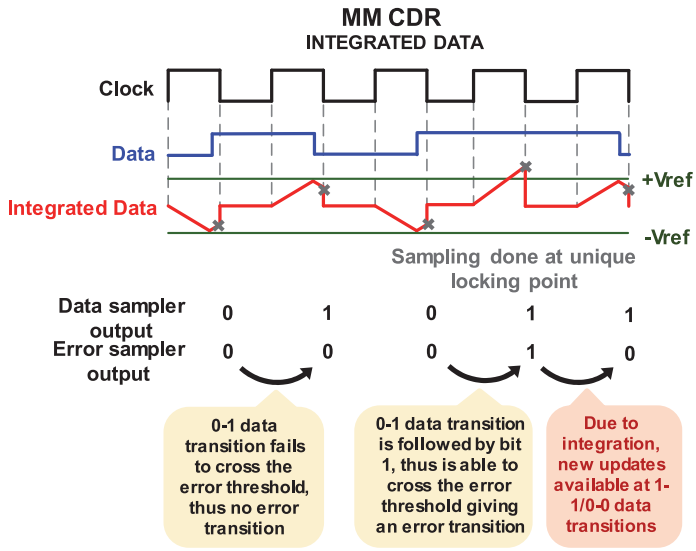

Fig. 11. MM CDR update generation in an integrating receiver scenario with a late clock and data sequence 01011, creating updates at 11/00 data trasitions. It also highlights the opportunity of updating even without data transitions.

generate a phase error update information in case of MM CDR in non-integrating scenario. Another disadvantage is having multiple locking phases depending on the band-limitation of the received data. For instance, a less band limited received signal will be a flatter square wave pulse, with no unique maximum eye opening position, thus, no unique locking point.

B. Mueller Muller Baud Rate CDR: Integrating Receiver

As discussed earlier, the effect of interference on receiver data can lead to faulty sampling. To circumvent the interference problem, we make use of the integrating receiver, which adapts the clock duty cycle such that the interference is an integral multiple of the integration period and its affect is cancelled out. As seen in Fig. 5, the integrated output is a function of input data, integration duration and clock data phase mismatch, translating any timing offset between clock and data to voltage information. As a result, the error information for a data transition becomes sensitized to the adjacent bit sequence.

1) Need for New CDR: The truth table of the baud rate CDR with integrating receiver remains same as in the non-integrating scenario. We can observe from Fig. 9 that only half of the 0–1 and 1–0 transitions result in an update information, depending on the adjacent data bits (i.e., updates for only 1–1/0–0 transitions). So the traditional MM CDR for an integrating front-end does not utilize the extra information provided by the integration operation and the update rate still remains as 25%. From Fig. 11 we can observe that at 011 data transition the corresponding error sequence is 010, however, MM CDR produces only a single update at 0–1 error transition and there is an opportunity to update at 1–0 error transition as well (which interestingly, does not correspond to a data transition). It is important to note that due to the integration functionality the maximum eye opening

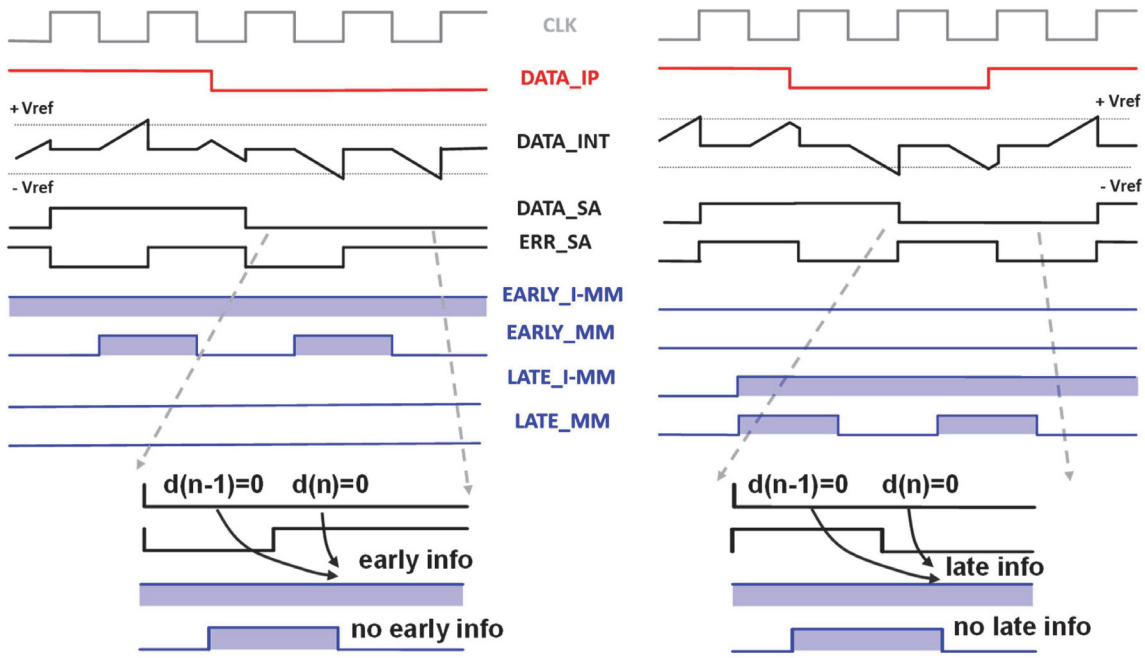

Fig. 12. Comparison between traditional MM CDR and I-MM CDR under integrating conditions. It can be seen from the data sequence that the I-MM CDR provides update for certain bit sequences, which is not provided by the traditional MM CDR, resulting in a higher update rate.

Integrating Mueller-Muller CDR : Integrating Front-End

D(n-2)	D(n-1)	D(n)	D(n+1)	E(n-1)	E(n)	Error Information
X	0	0	0	1	1	No Info
X	0	0	1	1	0	LATE
X	0	1	0	0	0	No Info
X	0	1	1	0	1	LATE
X	1	0	0	0	1	LATE
X	1	0	1	0	0	No Info
X	1	1	0	1	0	LATE
X	1	1	1	1	1	No Info
0	0	0	X	1	1	No Info
1	0	0	X	0	1	EARLY
0	0	1	X	1	0	EARLY
1	0	1	X	1	0	No Info
0	1	0	X	0	0	No Info
1	1	0	X	1	0	EARLY
0	1	1	X	0	1	EARLY
1	1	1	X	1	1	No Info

Fig. 13. I-MM CDR truth table for integrating receiver. The early-late information is obtained by looking at two data bits (D(n-1), D(n)) and two error bits (E(n-1), E(n)). The update rate is higher compared to a traditional Mueller-Muller CDR working on integrated data.

C. Proposed Baud Rate CDR: Integrating Receiver

For an integrating front-end, integration operation enables transfer of information from adjacent bits into the current bit period if there is a phase mismatch between the data and clock and converts this phase mismatch into voltage domain mismatch. Hence it is possible to extract phase error information even from a scenario when there is no data transition as can be seen Hence, by taking advantage of the phase-voltage mismatch transfer it is possible to increase the update rate of an integrating MM-CDR compared to a traditional MM CDR. The phase error information is derived from the current data bit (D(n)), previous data bit (D(n-1)), current error (E(n)) and previous error (E(n-1)) information. Although there is possibility of extracting Early/Late update information for all possible combinations of current and previous data bits, it occurs 50% of the time and is dependent on the adjacent data bits. Hence, the overall update rate of the CDR increases to 50% in this scenario, which can also be seen from the truth table in Fig. 13. In summary, the benefit of an integrating front-end is converting the timing mismatch to voltage domain mismatch making it possible to achieve a higher update rate. While the adjacent bit information remains unused in the traditional CDR with an integrating front-end, the proposed I-MM CDR utilizes it and increases its update rate.

VI. CDR Closed Loop Design Considerations

One of the key design constraints for a CDR is the offset value of the error samplers. This offset value determines the threshold beyond which the CDR starts corrective action. Another crucial component is the glitch correction circuitry, which is essential for proper CDR loop operation, especially at relatively low frequencies using technology nodes with very small delays. Glitches can falsely trigger edge sensitive sequential circuits, leading to faulty clock phase selection. To ensure no such false triggers occur, a glitch correction logic is added to the phase selection logic in the CDR loop. These two considerations are discussed in more detail in this section.

A. Choice of Error Sampler Threshold

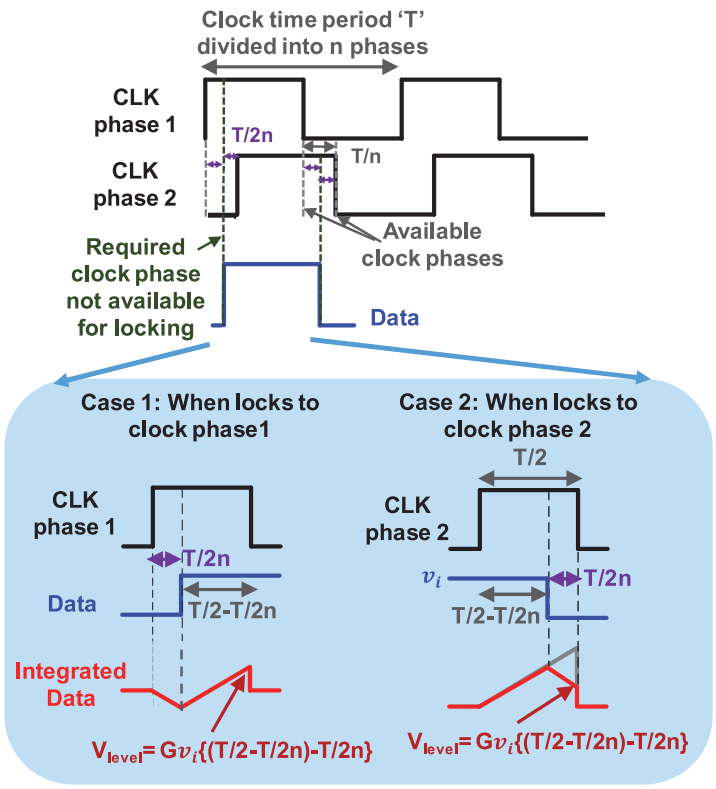

Fig. 14. Relationship between clock phases and sampler volatge offset.

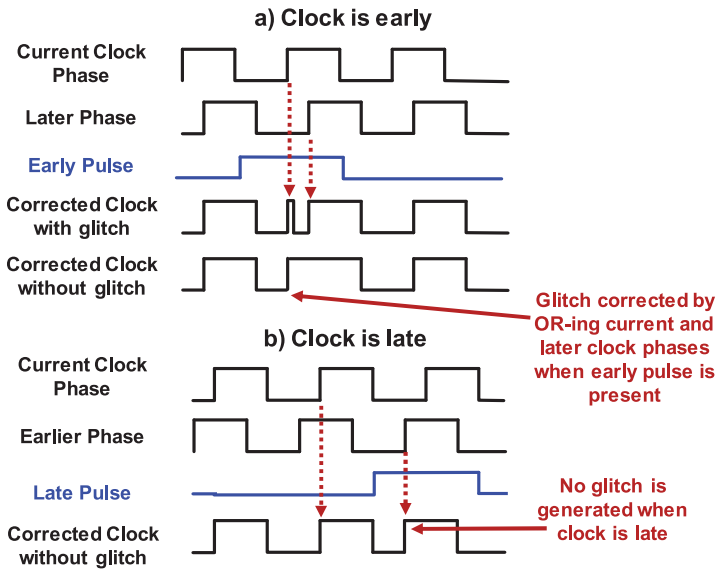

Fig. 15. Two cases of clock being early and late are illustrated. (a) When the clock is early, the corrected clock is a later phase clock leading to generation of glitch. (b) When the clock is late, an earlier clock phase is selected for correction but does not produce a glitch.

'n', then the difference between consecutive phases is T/n. In the worst case, the data lies in the middle of the two consequent phases and the clock data phase mismatch between them is $T/2n$ as shown in Fig. 14. In this scenario, the clock may choose to lock to either phase 1 or 2. The voltage level obtained after integration is $G * v_i * (T/2 - 2T/2n)$. On setting threshold of error samplers above this V_{level} will generate updates that will make the CDR toggle between clock phases 1 and 2. To avoid this situation, we choose the sampler threshold to be less than V_{level}, which will allow the CDR in this worst case situation to lock to either clock phase 1 or 2 and avoid unnecessary triggering. This introduces a dead-zone in the closed loop operation ensuring the CDR logic does not continuously generate phase mismatch information.

These threshold values, namely $+$Vref and $-$Vref are set by providing current offset to the error samplers. As discussed earlier, higher threshold values though provide better noise immunity, trigger updates more frequently reducing the loop stability.

B. Glitch Correction

Using human body as a broadband channel for communication between devices puts a constraint on the data rate and is limited by the body channel bandwidth of around 100 MHz [31]. In most HBC applications, required data rate is in few Mbps range. However, at scaled technology nodes (65 nm) the intrinsic delays of the gates are much faster than MHz frequencies. Thus, when the operating clock is in MHz range, the clock glitches in the clock waveform while switching between different clock phases. This is a unique scenario for broadband HBC, which is not present in traditional high speed wireline receivers employing phase interpolators. In those cases, the data rates are generally faster and the delays involved are close to the limit of the technology. This can be overcome either by having delay between different phases of the same order as its slew rate or by implementing a glitch correction logic. As shown in Fig. 15, generation of early/late updates changes the counter value at the positive edge of the current clock (in the duration when an update is high) and selects an updated phase of the clock from the multiplexer. Ideally, the counter must get updated and select the new clock phase exactly at the positive edge of the current clock phase when an early/late update signal is high. However, due to the combinational logic delay, the counter takes finite time to select the new clock phase from the multiplexer, during which the current clock stays selected and gets corrected to the new clock phase only after the combinational delay duration. When clock is early with respect to the data, a later phase of the clock must be selected for correction. When early update is high, at the positive edge of the current clock, it stays selected to the current clock (which goes high) and after some time when the new phase gets selected, the corrected clock starts following the new later clock phase (which is low), giving rise to a glitch as shown in Fig. 15. Thus, due to the delay taken by the combinational circuit to select the new clock phase a glitch is created. Interestingly, this happens only in the early clock scenario. When clock is late, and late update is high, at the positive edge of the current clock it remains selected at the current clock (which goes high) and after the combinational delay when the new earlier clock phase is selected, the corrected clock starts following it (which is also high). Thus, in this case there is no glitch generation. The glitch problem can be easily solved by logically OR-ing the current

it enables glitch correction by doing a logical operation between the appropriate phases.

VII. CDR Closed Loop Simulation

The I-MM CDR logic is written in Verilog and imported via Cadence AMS environment to verify the functionality and system performance. The closed loop I-MM CDR functionality is cross validated with a MATLAB based simulation model and is used to obtain BER results for data offset tolerance and interference robustness. BER performance for a large number of input bits under different data, clock frequency offset scenarios in presence of different signal to interference ratios (SIR) is evaluated. The proposed I-MM CDR loop is also synthesized, laid out and extracted in TSMC 65 nm technology for data rate and power consumption measurements.

A. Update Rate

The update rates of MM CDR and I-MM CDR are evaluated by applying a random bit stream of 4×10^6 data bits and measuring the early/ late updates in an open loop setting, i.e., without correcting the clock phases. The goal of this simulation is to validate the update rate values obtained from the truth table. The results show that the traditional MM CDR shows an update rate of 0.25 for early and 0.25 for late updates. On the other hand, I-MM CDR shows an update rate of 0.501 for early and 0.5 for late updates which correspond to the values obtained from the truth table.

B. Frequency Offset Tolerance

The offset tracking tolerance of the CDR is tested by providing a frequency offset between data and clock frequency and observing the BER at different offset scenarios. It can be seen from Fig. 16 that the I-MM CDR, with higher update rate has better tolerance for data frequency offset compared to traditional MM CDR. The update rate of the CDRs can be controlled by averaging, where the decision of the clock being either early or late is taken after a pre-determined number of early/late updates have occurred. Averaging is useful in cases where early and late updates are being generated alternately, some of which might be generated spuriously due to noise triggers. Through averaging it is ensured that in the case when CDR is actually early or late, i.e., when an early/late update is followed by a series of early/late updates, only then the clock gets corrected. Fig. 16 also shows that an update rate averaging of four (four consecutive early/late signal generates an actual early/late update) shows the best BER performance.

C. Interference Tolerance

As discussed in Section III, the human body antenna effect results in environmental interference affecting broadband signal transmission. Hence, along with clock data frequency offset, the CDR for a broadband HBC receiver must also be tolerant to interference. Interference tolerance of the I-MM CDR is

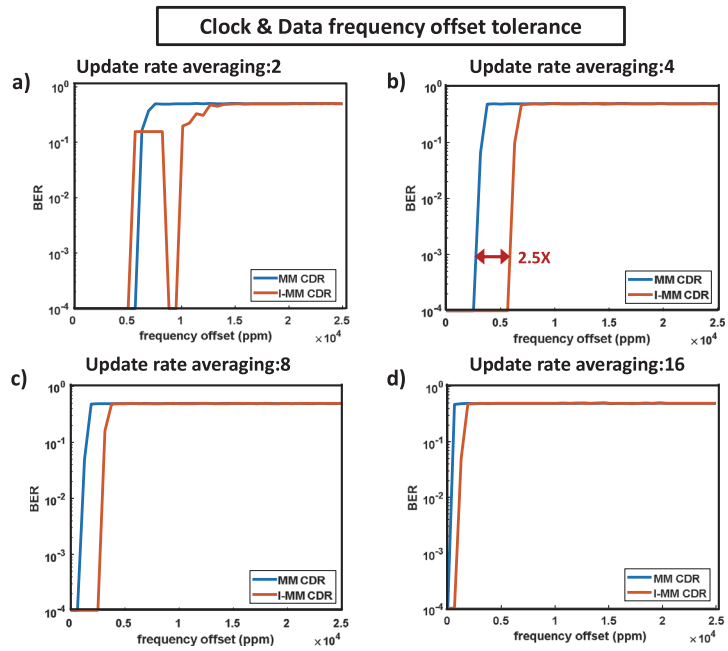

Fig. 16. Simulation results showing the data and clock frequency offset tolerance of the MM CDR and I-MM CDR for different averaging of early/late update rates. The I-MM CDR shows higher offset tolerance due to its higher update rate compared to the traditional MM CDR in an integrating scenario.

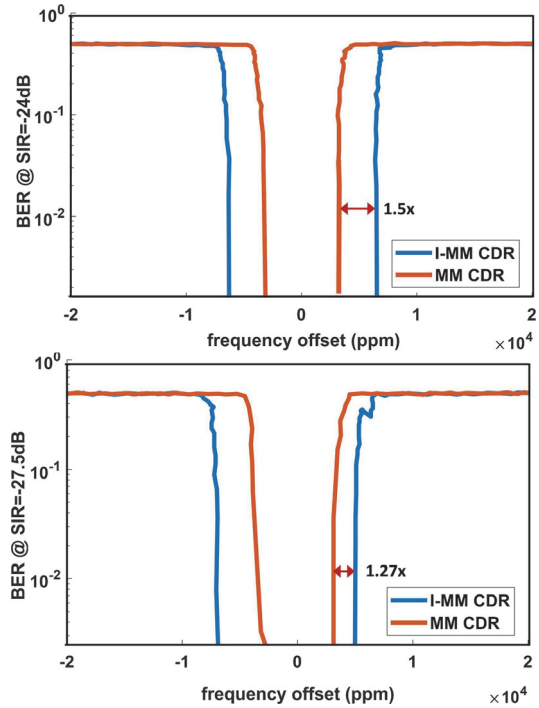

Fig. 17. Simulation results showing the data and clock frequency offset tolerance of the MM CDR and I-MM CDR for different SIRs. The I-MM CDR shows higher offset tolerance due to its higher update rate compared to the traditional MM CDR in an integrating scenario.

the BER when the interference frequency is kept constant, and the frequency offset between data and clock is varied. It can be observed that I-MM CDR shows >1.25X more tolerance to clock data frequency offset compared to the traditional MM

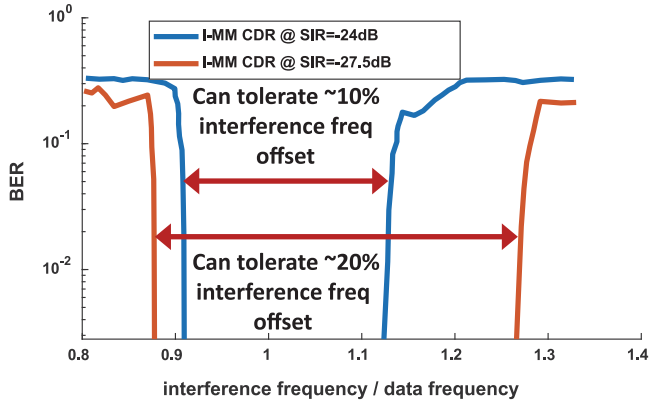

Fig. 18. Simulation results showing the interference frequency offset tolerance of modified I-MM CDR for different SIRs.

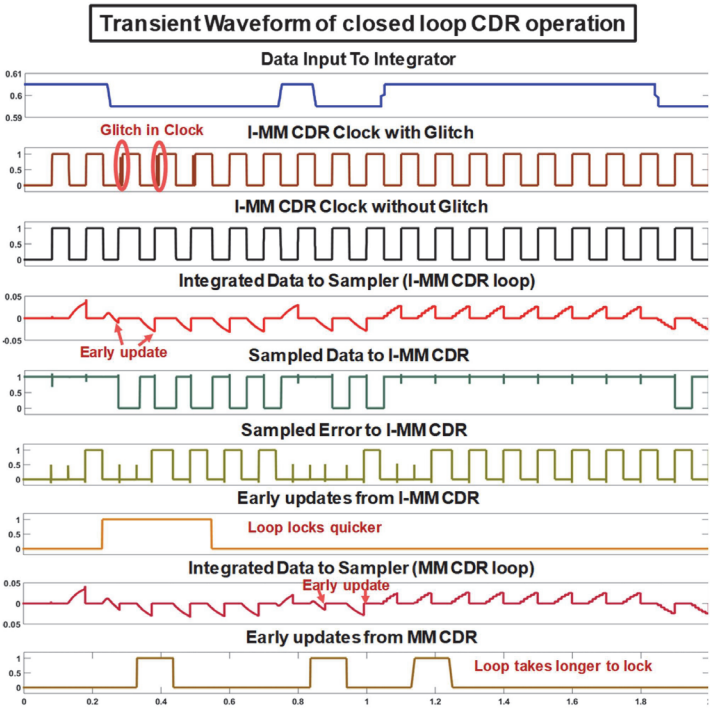

Fig. 19. System level transient waveforms of the closed loop CDR operation. The I-MM CDR generates early updates back to back which helps in locking the loop quicker compared to the traditional MM CDR.

tolerance when subjected to an SIR condition of −24 dB and −27.5 dB respectively.

As a separate experiment, the robustness of the I-MM CDR to interference is evaluated by changing the interference frequency while keeping the clock and data frequencies constant. Simulation results in Fig. 18 show that the CDR can tolerate up to −24 dB and −27.5 dB SIR with interference frequency offset of 20% and 10% respectively, compared to the data frequency.

D. Closed Loop System Level Functionality

Fig. 19 shows the transient waveforms of the traditional MM and modified I-MM closed loop CDRs. Due to data and clock phase mismatch the modified CDR generates early updates quite

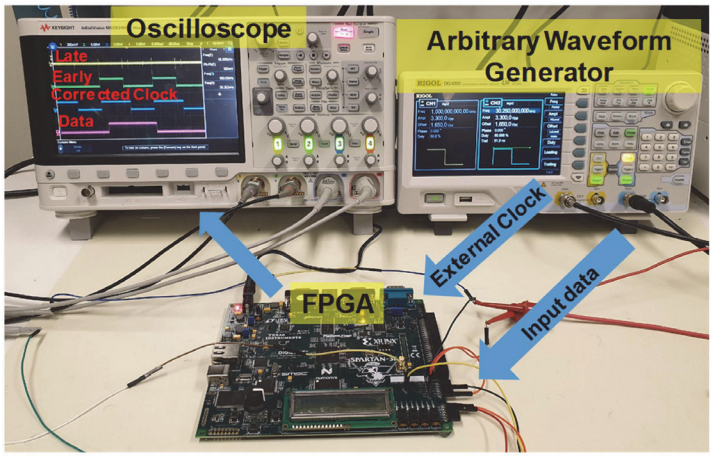

Fig. 20. Hardware implemetation setup of the I-MM CDR using Xilinx Spartan-3E FPGA, AWG and Oscilloscope.

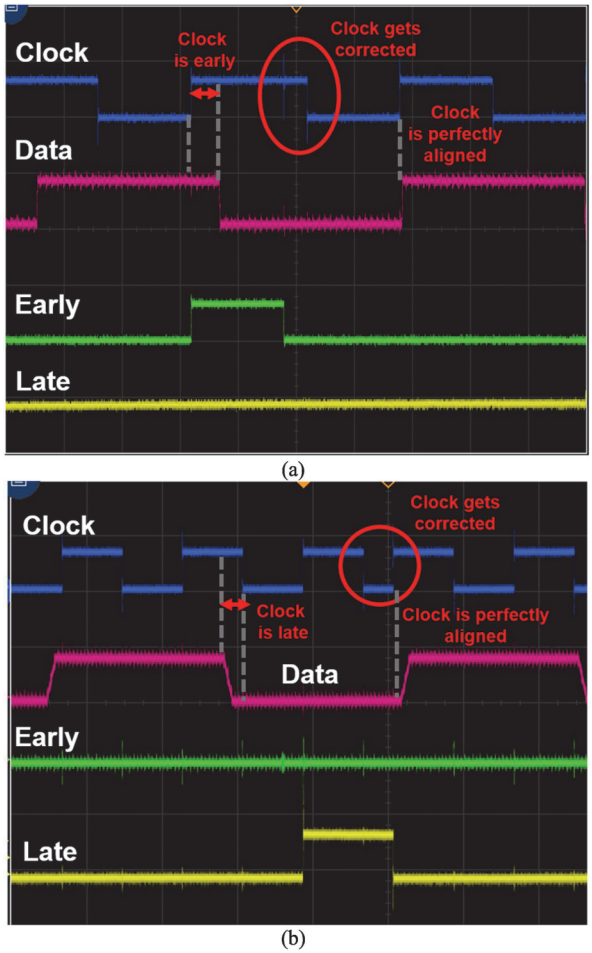

Fig. 21. I-MM CDR implemented on Xilinx Spartan-3E FPGA and the closed loop performance is viewed from oscilloscope. (a) Clock is early with respect to the data, which can be viewed visually. It results in a early update and gets aligned with the data at the subsequent positive clock edge. (b) Clock is late with respect to the data resulting in a late update. It gets corrected such that the next positive edge is aligned with the data.

data. The glitch correction logic ensures removal of any glitch with changing clock phase. The error sampler offsets are chosen to introduce a dead zone in the control loop and hence the loop gets locked to a steady state phase as seen from the waveforms.

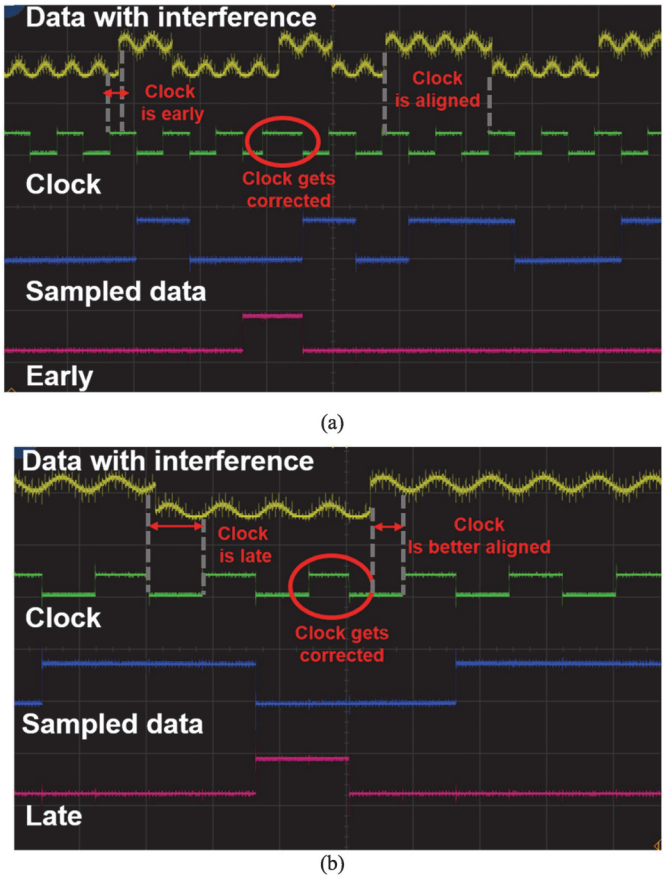

Fig. 22. I-MM CDR implemented on Xilinx Spartan-3E FPGA and the closed loop performance with −9 dB single tone SIR at 1 Mbps data rate is viewed from oscilloscope. (a) Clock is early with respect to the data with interference, which can be viewed visually. It results in a early update and gets aligned with the data at the subsequent positive clock edge. (b) Clock is late with respect to the data with interference resulting in a late update. It gets corrected such that the next positive edge is aligned with the data.

Closed loop I-MM CDR circuit is synthesized, laid out and extracted in Cadence to obtain achievable data rate and power consumption results. The post layout circuit simulation results support data rates up to 300 Mbps, using phase locked loop as our phase generator and utilizes a maximum power of 0.5 pJ/bit.

VIII. Hardware Implementation

We implemented the modified I-MM closed loop CDR on Xilinx Spartan-3E FPGA kit and observed the CDR functionality. The CDR functionality is experimentally validated by providing it with a nominal clock of 16 MHz and a data rate of 1 Mbps using PRBS data sequence. The higher frequency external clock is internally divided to generate 16 phases of a 1 MHz clock. Arbitrary waveform generator (AWG) is used to provide external data as well as the clock. The phase alignment as well as the frequency mismatch between the data and the clock can be controlled through AWG. The input data is integrated using a digital integrator and sampled through a digital comparator which compares the integrated digital equivalent to the pre-determined threshold values to obtain data and error samples. Digital integrator and comparator are used to emulate of the front-end to a first order. In this section, we focus on evaluating the performance and functionality of the closed loop integrating CDR through actual hardware. Using the data and error samples, the CDR logic generates early/late updates which increments/decrements an up/down counter. A digital phase generator is implemented to generate sixteen clock phases and the counter value is used to select the appropriate clock phase with reduced clock and data phase mismatch. The hardware implementation setup is as shown in Fig. 20 and the corrected clock and early/late updates were observed on an oscilloscope as shown in Fig. 21. A single tone interference of −9 dB SIR is added on top of PRBS data and the closed loop performance of I-MM CDR is observed on the oscilloscope as shown in Fig. 22. By virtue of the integrating front-end, data and error samples generated at the output of the integrator are same both with and without the interference subjected on the input PRBS data. It can be observed that in presence of interference, which is an integral multiple of the integration period has its effect cancelled out irrespective of its amplitude/SIR, thus the I-MM CDR sees the same data and error samples as it would without interference. This allows the data and error samples to correctly generate early/late updates as expected, in turn correctly adjusting the clock phase to be in better alignment with the incoming input data with interference. Thus, as explained, data subjected to higher SIRs exhibit same performance under the constraint of the integration duration being an integral multiple of the interference duration.

IX. Conclusion

This paper analyses the benefits of using an integrating front-end receiver for realization of interference robust and energy efficient broadband HBC. Clock data recovery is an integral part in such broadband communication systems to recover the data properly by reducing the clock and data's phase mismatch. The paper analyses the operation of MM CDR for an integrating front-end and proposes an I-MM CDR with a higher update rate by utilizing the adjacent bit information reflected in the current bits in presence of the integrating front-end. The I-MM CDR shows >5000 ppm clock-data frequency offset tolerance (2.25X higher than MM CDR), 1.27X better data-clock frequency offset tolerance in presence of −27.5 dB SIR and can tolerate >10% interference frequency offset, i.e., when the interference is not an exact integral multiple of the integration clock. Finally, the I-MM CDR functionality is validated through hardware implementation using a Xilinx Spartan-3E FPGA using 1 Mbps PRBS data with −9 dB SIR.

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