

Reliable Power Grid Network Design Framework Considering EM Immortalities for Multi-Segment Wires

Han Zhou, Shuyuan Yu, Zeyu Sun, and Sheldon X.-D. Tan
Department of Electrical and Computer Engineering, University of California, Riverside, CA 92521

Abstract—This paper presents a new power grid network design and optimization technique that considers the new EM immortality constraint due to EM void saturation volume for multi-segment interconnects. Void may grow to its saturation volume without changing the wire resistance significantly. However, this phenomenon was ignored in existing EM-aware optimization methods. By considering this new effect, we can remove more conservativeness in the EM-aware on-chip power grid design. Along with recently proposed nucleation phase immortality constraint for multi-segment wires, we show that both EM immortality constraints can be naturally integrated into the existing programming based power grid optimization framework. To further mitigate the overly conservative problem of existing immortality-constrained optimization methods, we further explore two strategies: first we size up failed wires to meet one of immortality conditions subject to design rules; second, we consider the EM-induced aging effects on power supply networks for a targeted lifetime, which allows some short-lifetime wires to fail and optimizes the rest of the wires. Numerical results on a number of IBM and self-generated power supply networks demonstrate that the new method can reduce more power grid area compared to the existing EM-immortality constrained optimizations. Furthermore, the new method can optimize power grids with nucleated wires, which would not be possible with the existing methods.

I. INTRODUCTION

Electromigration (EM) remains the top killer for the copper based interconnects in current and near-future advanced VLSI technologies. The International Roadmap for Devices and Systems (IRDS) [1] and the International Technology Roadmap for Semiconductors (ITRS) [2] predict that the allowable current density continues to decrease due to EM while the required current density to drive the gates continues to increase. As a result, the EM-related aging and reliability will become worse for current 7nm and below technologies.

For practical VLSI chip, the on-chip power supply or power-ground (P/G) networks are most susceptible to EM failures due to large and unidirectional current densities [3]–[6]. The interconnect usually contains multiple segments, which is a multi-segment wire. As a result, designing robust power supply networks to satisfy the demanding design requirements remains a challenging task.

During the power grid synthesis in a typical design flow, an important step is to size the wire width of the power grid stripes after the topology of the power supply networks has been determined, power grid areas are optimized while electromigration and excessive IR drop constraints are met. There is a rich body of work previously proposed for the power supply network optimization, based on nonlinear or sequence of linear programming (SLP) methods [7]–[14]. To satisfy the EM reliability, most methods used the current density of individual wires as the constraint, which is mainly based on the highly conservative Black’s EM model [3]. Furthermore, most of them failed to consider the multi-segment interconnects, which consists of continuously connected high-conductivity metal within one layer of metallization. Recent studies show that the hydrostatic stress in multi-segment interconnect wires (as shown in Fig. 1) are coupled and the EM failure conditions must be considered for the whole interconnect wire [15]–[21]. For instance, the parameter change of one wire segment may affect the EM stress condition of another wire segment in the same interconnect tree, which provides more powerful potential to optimize a power grid subject to EM constraints for a multi-segment wire compared with the traditional current density based methods.

This work is supported in part by NSF grant under No. CCF-1527324, and in part by NSF grant under No. CCF-1816361 and in part by NSF grant under OISE-1854276.

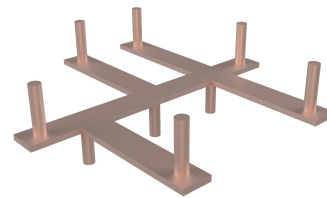


Fig. 1: Example of a multi-segment wire.

In [14], [22], a power grid network sizing method considering the multi-segment interconnects has been proposed based on the multi-segment EM immortality check criteria [23]. It can automatically consider all the wire segments and their interactions in a wire interconnect tree. However, the proposed EM immortality constrained optimization can still be too conservative as it still requires all the wire segments in each tree to be immortal, i.e., void nucleation are not allowed.

For a multi-segment interconnect, if a void is formed in a segment, the void will start to grow. However, the void growth will stop when compressive stress in the remaining wires reach steady state status (back force from the compressive stress is equivalent to the force for void growth). The void volume at this time is called *saturation volume*. If the saturation volume of a void is smaller than the so-called *critical volume* or *critical area* as shown in Fig. 2, then the wire will still be considered immortal even if a void is formed. The *critical volume/area* is defined as the volume (or area in the two-dimensional case) that the void must meet or exceed to completely block the current flow in the copper interconnect and shunt it to the metal liner. Therefore, the conservative nature of the power grid optimization process can be relaxed if this saturation volume effect is considered. This will be the major focus of this work.

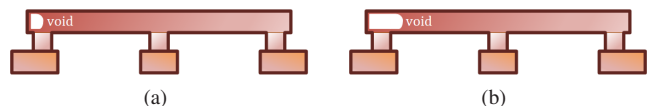


Fig. 2: (a) Void is smaller than the critical area. (b) Void is larger than the critical area.

In this article, we propose a new power grid network sizing technique based on the recently proposed EM saturation volume estimation method for general multi-segment interconnect wires [24], [25]. With the new EM saturation volume model, the EM immortality can be redefined as we can treat some nucleated wires as immortal as well. We demonstrate how the immortality constrained EM wire sizing can be reformulated considering the new EM saturation volume for general multi-segment interconnects. Then we show how the new constraints can be used in the existing sequence of linear programming based power grid optimization framework. We illustrate that many of the power grids which cannot be optimized using existing EM immortality constraints can be further optimized using the new EM immortality criteria while the resulting power grid networks with some failed interconnects can still be considered immortal. Furthermore, we define two EM immortality constraints: *EM nucleation phase immortality* and *EM incubation phase immortality*, which is a new concept, to distinguish two different immortality conditions. On top of this, we show that both EM immortality conditions and check

criteria can be naturally integrated into the existing programming based power grid optimization framework, which still remains the most effective power grid optimization method. To mitigate the overly conservative nature of the optimization formulation, we further considered the EM-induced aging effects on power supply networks for a target lifetime, which allows some short-lifetime wires to fail and optimizes the rest of the wires. Numerical results on a number of IBM and self-generated power supply networks demonstrate that the new method outperforms the existing immortality constrained optimizations. Furthermore, the new method can optimize the on-chip power grids with nucleated wires, which was considered EM mortal and can't be optimized by the existing immortality constrained optimization methods or leading to more area reduction than previous methods.

II. REVIEW OF EM PHYSICS AND STRESS MODELING

EM is the physical phenomenon of the migration of metal atoms along the direction of the applied electrical field. Atoms (either lattice atoms or defects/impurities) migrate along the trajectory of conducting electrons. Due to momentum exchange between lattice atoms, hydrostatic stress is generated inside the embedded metal wire during migration process. Before the hydrostatic stress reaches the critical level, the atomic flux flowing caused by electron flow from cathode to anode can still balance with the atomic flux caused by inhomogeneous distribution of hydrostatic stress. When the stress reaches the critical level, a void and a hillock caused by conducting electrons will be formed at the cathode end and anode end respectively. However, if the hydrostatic stress cannot reach the critical level, the void will not be formed. In the case where a void cannot be formed it is called EM nucleation phase immortal.

After a void is formed, it will keep growing until saturated. Void saturation happens when two kinds of flux balance with each other. One is the flux of atoms previously located in metal which is consumed by the growing void and the other is the back flux of atoms generated by a gradient of growing stress. If void volume is smaller than the volume of the intersection which is recognized as critical volume \mathcal{V}_{crit} , current can still flow through the copper wire as the wire cross-section is not blocked by the void. Once the void size is large enough and occupies the wire cross-section, current has to go through the liner whose resistivity is much higher than copper and the resistance of the wire will increase. As can be seen, if the saturation volume is smaller than critical volume, the wire is still immortal although a void is formed. This case is called EM incubation phase immortal.

In order to determine if a wire is immortal, a model predicting the saturation volume \mathcal{V}_{sat} was proposed in [24] shown as following

$$\begin{aligned} \mathcal{V}_{sat} &= \sum_i \mathcal{V}_{sat,i} = h \times \sum_i \mathcal{A}_{sat,i} \\ &= h \times \sum_i \left[(-2\sigma_{c,i} + \frac{j_i l_i \rho e Z}{\Omega}) \times \frac{l_i w_i}{2B} \right] \\ &= h \times \sum_i \left[(-2\sigma_{c,i} + \frac{V_i e Z}{\Omega}) \times \frac{l_i w_i}{2B} \right] \end{aligned} \quad (1)$$

where h is thickness of the wire and $\mathcal{V}_{sat,i}$, $\mathcal{A}_{sat,i}$, $\sigma_{c,i}$, j_i , l_i and w_i represent the contribution to void volume, contribution to void area, stress at the cathode, current density, and length and width of the i th segment respectively. For the segment in which a void has nucleated, $\sigma_{c,i}$ is 0 on the cathode where the void is nucleated. Except for the segment with the void, steady-state stress on cathode of other segments are the same as the anode of the segment connected to them.

As shown in the Eq. (1), voltage and width on each branch i can contribute to the void volume. So saturation void volume can be adjusted in order to reach incubation immortal by modifying the voltage and width of the branches. Besides, \mathcal{V}_{crit} can be expressed as

$$\mathcal{V}_{crit} = h \times w \times d \quad (2)$$

where h is thickness of the wire, w is the wire width and d is the via diameter. For wide wires, multiple vias may be applied, then d is

equivalent to w . In this case, we can assume that \mathcal{V}_{crit} is proportional to w^2 .

In order to know if the wire is EM incubation phase immortal or not, the saturation volume is compared with the critical volume, specifically, the wire is incubation phase immortal if

$$\mathcal{V}_{sat} < \mathcal{V}_{crit} \quad (3)$$

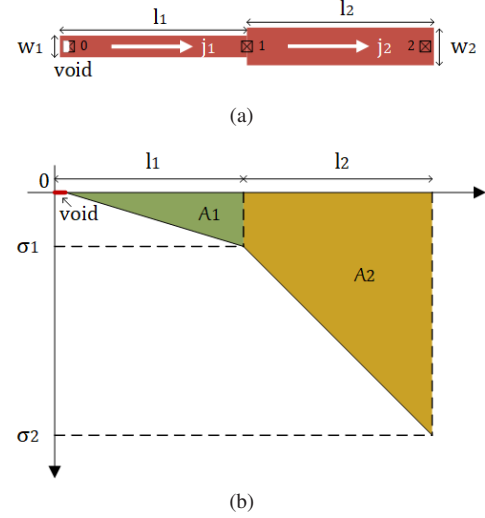


Fig. 3: (a) A two-segment wire and the direction indicate electron flow. (b) Stress integration area of a two-segment wire.

Fig. 3 uses a two-segment wire to illustrate this method. Here, stress at node 1 and node 2 can be expressed

$$\begin{aligned} \sigma_1 &= 0 - \frac{(\mathcal{V}_1 - 0)eZ}{\Omega} = -\frac{j_1 l_1 \rho e Z}{\Omega} \\ \sigma_2 &= -\sigma_1 - \frac{(\mathcal{V}_2 - \mathcal{V}_1)eZ}{\Omega} = -\frac{(j_1 l_1 + j_2 l_2)\rho e Z}{\Omega} \end{aligned} \quad (4)$$

Fig. 3(b) shows stress at steady state during growth phase with calculated stress at node 1 and node 2. As can be seen, stress on both branches has contribution to the void formation. \mathcal{A}_1 and \mathcal{A}_2 in the figure are the contribution to void area of two branches. Then can compute void saturation volume using Eq. (1), compare \mathcal{V}_{sat} with \mathcal{V}_{crit} to see if the wire is EM incubation phase immortal.

III. NEW EM IMMORTALITY CONSTRAINED OPTIMIZATION FOR MULTI-SEGMENT INTERCONNECTS

In this section, we propose a new EM immortality constrained power grid wire sizing optimization method for multi-segment interconnect wires. Compared to recent work [14], the new EM constraint is less conservative and can optimize more hard-to-optimize problems while ensuring all the wires EM immortal. We first introduce the power grid models in our work, then we propose a few new EM immortality definitions. Then we present the new EM immortality constrained optimization method.

A. Power grid models

In this optimization, the P/G network is composed of an orthogonal mesh of multi-segment wires. Only DC issues are considered, i.e., we focus on the resistance of the network. Furthermore, we do not size vias and thus ignore via resistance. To get the initial nodal voltages and branch currents of the P/G network, an equation must be solved first $G \times V = I$.

B. New EM immortality criteria

In general, the EM failure process is divided into nucleation phase, incubation phase and growth phase. In the nucleation phase, the stress at the cathode increases. When it reaches a critical level, a void will be nucleated. After the nucleation phase, the void starts to grow and eventually leads to wire failure after a period of time.

1) *EM immortality for multi-segment wires*: Fig. 4 shows the void formation in a power grid network. We consider the following three cases.

a) *Case 1*: In the left vertical wire, no void is formed, which means the stress at the cathode does not exceed the critical stress in the nucleation phase. Thus the wire is EM immortal. We call it *EM nucleation phase immortal*.

b) *Case 2*: In the middle vertical wire, a void is nucleated, but it does not fully cover the via, EM failure process ends at the incubation phase in which no meaningful wire resistance is observed. Note that the via resistance may change due to void formation, but we do not take via resistance into consideration here. In conclusion, the void is saturated before reaching the critical volume and the wire is still considered EM immortal. We call it *EM incubation phase immortal*.

c) *Case 3*: In the right vertical wire, a void is nucleated at the cathode, after the incubation phase, it fully covers the via, initiating the true growth phase. In this phase, the resistance starts increasing as current starts to flow through the more resistive barriers of the copper wire. When it increases to the critical level (such as 10% or other defined thresholds) the wire can be considered to be failed. We deem this kind of wire *EM mortal*.

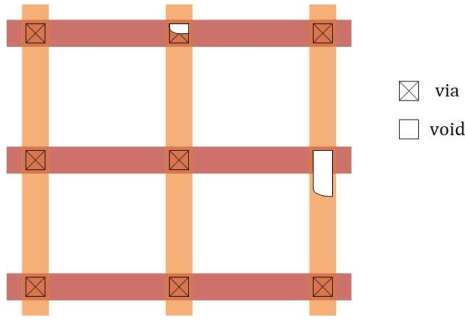


Fig. 4: Void formation of a power supply network.

2) *New EM immortality check*: In [23], [26], a new EM immortality check criteria has been proposed for general multi-segment interconnects. This method, called voltage-based EM or *VBEM* method, formulated the new criteria in terms of nodal voltages (which is in contrast to traditional current density based method). Specifically, the EM immortality condition of a multi-segment interconnect is described as

$$V_E < V_{crit,EM} \quad (5)$$

where *critical EM voltage* $V_{crit,EM}$ is defined by

$$V_{crit,EM} = \frac{1}{\beta}(\sigma_{crit} - \sigma_{init}) \quad (6)$$

where σ_{init} is the initial stress. $V_{E,m}$ is the *EM voltage* for that tree, it is proportional to stress at the ground node (σ_g) and can be calculated as

$$V_E = \frac{1}{2A} \sum_{k \neq g} a_k V_k \quad (7)$$

where V_k is the normal nodal voltage (with respect to cathode node *cat*) at node k of the wire and a_k is the total area of branches connected to node k . With voltage of node i (V_i), steady-state stress at that node (σ_i) can be calculated as $\sigma_i = \beta(V_E - V_i)$, where $\beta = \frac{eZ}{\Omega}$, e is elementary charge, Z is effective charge number and Ω is the atomic lattice volume.

However, this condition only checks void nucleation (Case 1). It does not consider the case where a void is nucleated in a wire, but the saturation void volume is less than the critical volume (Case 2).

Given a multi-segment wire m , the new EM immortality criteria first checks *VBEM* for the cathode node. If it passes, then the wire is considered to be immortal. Otherwise, we compute the saturation void volume V_{sat} from Eq. (1) and perform saturation volume check using Eq. (3). If Eq. (3) satisfies, the wire is still immortal. Otherwise, it is mortal, more complicated analysis of transient hydrostatic stress evolution is needed to evaluate the time to failure.

Note that EM nucleation phase immortal indicates that no void will be formed, in other words, the stress will not reach the critical level. It does not mean that the saturation volume is 0, however, saturation volume makes sense only after a void is nucleated.

We remark that the EM models applied in our work are for general cases, we will consider process variation with Monte Carlo method in the future.

C. Problem formulation

Let $G = \{N, B\}$ be a P/G network with n nodes $N = \{1, \dots, n\}$ and b branches $B = \{1, \dots, b\}$. Each branch i in B connects two nodes i_1 and i_2 with current flowing from i_1 to i_2 . l_i and w_i are the length and width of branch i , respectively. ρ is the sheet resistivity. The resistance r_i of branch i is

$$r_i = \frac{V_{i1} - V_{i2}}{I_i} = \rho \frac{l_i}{w_i} \quad (8)$$

1) *Objective function*: We can express the total routing area of a power grid network in terms of nodal voltages, branch currents and branch lengths as follows

$$f(V, I) = \sum_{i \in B} l_i w_i = \sum_{i \in B} \frac{\rho I_i l_i^2}{V_{i1} - V_{i2}} \quad (9)$$

2) *Constraints*: The constraints that need to be satisfied for a reliable, working P/G network are shown as follows.

1. Tree-related constraints

a) *Equal width constraints*: For typical chip layout designs, branches within an interconnect tree should have the same width, i.e. $w_i = w_k$.

$$\frac{V_{i1} - V_{i2}}{l_i I_i} = \frac{V_{k1} - V_{k2}}{l_k I_k} \quad (10)$$

b) *New EM immortality constraints for multi-segment interconnects*: As described before, for a multi-segment interconnect m , we consider two EM immortality constraints: the *EM nucleation immortal constraint* (5) and *EM incubation phase immortal constraint* (3). We will select one of them depending the m stress conditions.

We remark that for constraints (5) and (3), both the *EM voltage*, $V_{E,m}$ and the saturation volume V_{sat} are linear functions of the nodal voltages of the interconnect wires, supposing that the length and width of each branch is fixed. As a result, the constraints are still linear in terms of nodal voltages, which is a requirement for the sequence of linear programming method.

2. Other constraints

c) *Voltage IR drop constraints*: A threshold voltage is required to guarantee proper logic operation

$$V_j > V_{min} \text{ for power network} \quad (11)$$

d) *Minimum width constraints*: Usually different layers have different requirements for the width of the wire segments

$$w_i = \rho \frac{l_i I_i}{V_{i1} - V_{i2}} \geq w_{i,min} \quad (12)$$

e) *Kirchoff's current law (KCL)*: For each node j , we have

$$\sum_{k \in B(j)} I_k = 0 \quad (13)$$

where $B(j)$ is the set of branches incident on node j .

D. Relaxed two-step sequence of linear programming solution

The power grids optimization aims to minimize objective function (9) subject to constraints (5), (3), (11)-(13). It will be referred as problem P . Problem P is a constrained nonlinear optimization problem.

Note that $V_{E,m}$, which is defined in Eq. (7), is a function of both nodal voltage and area of a wire. According to the objective function

(9), the area of a wire segment is a function of nodal voltage and branch current, therefore, $V_{E,m}$ is a nonlinear function. Take a three-segment wire which is similar to Fig. 3(a) as an example,

$$\begin{aligned} V_{E,m} &= \frac{a_1 (V_0 - V_{cat,m}) + (a_1 + a_2) (V_1 - V_{cat,m})}{2(a_1 + a_2 + a_3)} \\ &\quad + \frac{(a_2 + a_3) (V_2 - V_{cat,m}) + a_3 (V_3 - V_{cat,m})}{2(a_1 + a_2 + a_3)} \\ &= \frac{l_1 w_1 V_0 + (l_1 w_1 + l_2 w_2) V_1 + (l_2 w_2 + l_3 w_3) V_2 + l_3 w_3 V_3}{2(l_1 w_1 + l_2 w_2 + l_3 w_3)} \\ &\quad - V_{cat,m} \end{aligned} \quad (14)$$

where $V_{cat,m}$ is the cathode node voltage of the wire. If we have the equal width constraints (10), which indicates $w_1 = w_2 = w_3$, then the EM nucleation phase immortal constraint (5) actually becomes a linear function of nodal voltage again. This is because current density is independent of wire width and is related to wire length.

$$V_{E,m} = \frac{l_1 V_0 + (l_1 + l_2) V_1 + (l_2 + l_3) V_2 + l_3 V_3}{2(l_1 + l_2 + l_3)} - V_{cat,m} \quad (15)$$

For $\mathcal{V}_{sat,m}$, it is also nonlinear in terms of nodal voltages, assume V_0 is the cathode node voltage,

$$\begin{aligned} \mathcal{V}_{sat,m} &= h \times \left[\left(-2\sigma_0 + \frac{(V_1 - V_0) eZ}{\Omega} \right) \frac{l_1 w_1}{2B} + \left(-2\sigma_1 \right. \right. \\ &\quad \left. \left. + \frac{(V_2 - V_1) eZ}{\Omega} \right) \frac{l_2 w_2}{2B} + \left(-2\sigma_2 + \frac{(V_3 - V_2) eZ}{\Omega} \right) \frac{l_3 w_3}{2B} \right] \\ &= h \times \frac{eZ}{2B\Omega} [(V_1 - V_0) l_1 w_1 + (V_1 + V_2 - 2V_0) l_2 w_2 \\ &\quad + (V_2 + V_3 - 2V_0) l_3 w_3] \end{aligned} \quad (16)$$

However, considering $\mathcal{V}_{crit,m}$ is proportional to w^2 , EM incubation phase immortality condition can be simplified as

$$\frac{eZ}{2B\Omega} [(V_1 - V_0) l_1 + (V_1 + V_2 - 2V_0) l_2] < w \quad (17)$$

With all these linear constraints, we can follow the relaxed two-phase iterative optimization process [9], [11] and apply the sequence of linear programming technique [14] to solve the relaxed problem in each phase.

Specifically, we have a voltage solving phase when all branch currents are assumed to be fixed and a current solving phase when all nodal voltages are fixed. Because the objective function in the voltage solving phase is nonlinear, we take the first-order Taylor's expansion around the initial solution V^0 to get the linearized objective function

$$g(V) = \sum_{i \in B} \frac{2\rho I_i l_i^2}{V_{i1}^0 - V_{i2}^0} - \sum_{i \in B} \frac{\rho I_i l_i^2}{(V_{i1}^0 - V_{i2}^0)^2} (V_{i1} - V_{i2}) \quad (18)$$

Since I_i is a constant, an additional constraint is added [11]

$$\xi \text{sign}(I_i) (V_{i1}^0 - V_{i2}^0) \leq \text{sign}((I_i) (V_{i1} - V_{i2})) \quad (19)$$

where $\xi \in (0, 1)$ is a restriction factor, which will be selected by some trials and experiences and $\text{sign}(x)$ is the sign function.

IV. COMPREHENSIVE POWER GRID OPTIMIZATION STRATEGIES

In this section, we propose several EM constrained power grid optimization strategies for multi-segment interconnect wires.

A. New EM immortality constrained P/G optimization

In the aforementioned optimization problem, the new EM immortality constrained P/G optimization starts with an initial feasible solution which is obtained from Eq. (III-A). Then we iteratively solve the voltage solving phase and current solving phase. The entire EM immortality constrained power grid network optimization procedure is summarized as follows.

New EM immortality constrained P/G wire sizing algorithm

1. Obtain the initial V^k , I^k for $k = 0$ from network G_I .
2. Perform new saturation volume based EM immortality check flow (The flow will be discussed later). Construct equal width

constraints (10), EM nucleation phase immortal constraints (5) or EM nucleation phase immortal constraints (3), minimum width constraints (12), and linear companion constraints (19) with I^k .

3. Minimize $g(V^k)$ subject to constraints (11), (12), (5), (3), (10), and (19) by sequence of linear programmings, record the result as V_m^k , m begins from 1. If $f(V_m^k) > f(V_{m-1}^k)$, perform line search along the direction $d = V_m^k - V_{m-1}^k$ until $f(V_m^k) \leq f(V_{m-1}^k)$. Record the result from last iteration m as V^{k+1} .
4. Construct equal width constraints (10) and minimum width constraints (12) with V^{k+1} .
5. Minimize $f(I^k)$ subject to constraints (12), (10), and (13) by sequence of linear programmings, record the result as I^{k+1} .
6. If $|f(V^{k+1}, I^{k+1}) - f(V^k, I^k)| < \varepsilon$, ε is the stopping criterion, then stop. Otherwise, set $k = k + 1$ and goto step 2.

At the beginning of each voltage solving phase (step 2-3), we check the EM immortality for all the interconnect trees. If there exists a wire, which is neither EM nucleation phase immortal nor EM incubation phase immortal, we consider the power grid can not be optimized. Otherwise, EM constraint is built for each wire for later optimization. Note that the length and width of a certain branch used in each iteration may differ, thus the constant part of the EM constraints will change. Sometimes the initial P/G network does not meet the EM requirement, in order to enable the optimization, we keep the original topology but adjust the resistance/width of power grid stripes. The new saturation volume based EM immortality check flow is shown in Fig. 5.

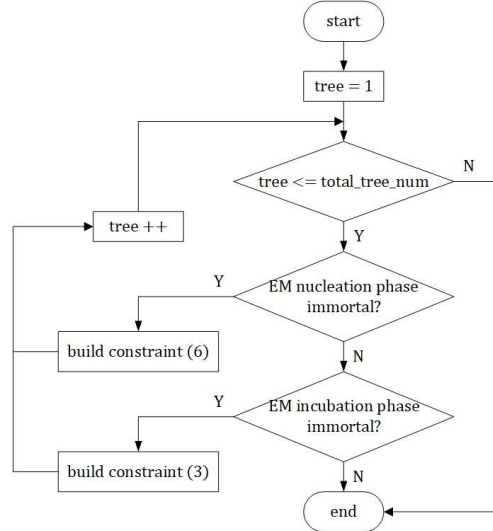


Fig. 5: Saturation volume based EM immortality check for P/G network.

B. New EM immortality constrained P/G optimization with pre-wire-sizing

EM immortality requirement for all the interconnects at the initial stage sometimes can be too strict. This happens when the initial P/G grids are designed so that we may not be able to find a solution from the previous optimization process. To mitigate this problem, we propose a pre-wire-sizing strategy, which can also be seen as a preprocessing stage before the P/G optimization.

As discussed earlier, we check the EM immortality conditions at the beginning of the voltage solving phase and consider the power grid network cannot be optimized if neither immortality condition is satisfied, which will greatly reduce the optimization space.

When a wire fail the immortality condition, one idea is to size the width up to make the wire immortal subject to the design rules. When we increase the width of the wire segment or interconnect trees (for all of its segments), we will increase the critical void volume, which is

increased quadratically with the width w as defined in (2). As a result, the wire may become incubation immortal based on (3). Also, width increase will also reduce the current density and branch voltages, as a result, it can also make the wire nucleation phase immortal based on (5) and (7). In our approach, we size up the failed wires so that one of the immortal conditions are met. We can size the wire by recomputing the branch voltages assuming that it will not affect other connected interconnect trees as a first order approximation until one of immortality conditions are met.

C. EM lifetime constrained P/G optimization

Previous methods use EM immortal constraints to ensure that none of the interconnect trees fail. However, such constraint may be conservative because some wires can have EM failures as long as the power grid networks can work in the target lifetime and it fails to contain aging effect. Therefore, a EM aging-aware P/G wire sizing optimization method is applied in which some segments of interconnects will be allowed to fail or to increase resistance.

After performing EM immortality check, if neither of the EM constraints are met for a certain interconnect tree, then the lifetime of the wire will be computed based on the fast EM lifetime estimation method [27]. If the calculated lifetime is smaller than the target lifetime, the interconnect will be marked as failed and its EM constraint will not be considered any more. Furthermore, if void is formed in via-above interconnect, the via will be treated as disconnected (open circuit), otherwise (via-below case), segment resistance increase will be computed [22].

On the other hand, if the calculated lifetime meet or exceed the target lifetime, the saturation volume obtained from the previous optimization $V_{sat,m,prev}$ for m th segment will become the new critical void saturation volume for next optimization iteration, i.e. (3) becomes

$$V_{sat,m,prev} > V_{sat,m} \quad (20)$$

The rationale behind this is that we relax the incubation phase immortality constraint as it still leads to satisfactory lifetime for this wire in previous optimization. But adding this constraint, we expect that its lifetime will not change too much and still meet the given lifetime after the follow-up optimizations. After either *resistance change*, or *wire disconnection*, or *constraint relaxation*, a new round of SLP programming optimization is carried out until the chip meet the EM lifetime target after the optimization. Compared with [22], there will be more sizing space with the saturation volume based constraint and it will provide better optimization results.

V. EXPERIMENTAL RESULTS AND DISCUSSION

A. Experiment setup

The proposed EM-aware constrained power grid optimization is implemented in C/C++. Several IBM power grid benchmarks [28] are used to test our work. We also have a few synthesized power grid networks so that different kinds of EM immortality constraints can be tested and verified. Node location and layer information are provided, therefore, the geometric structure of a certain benchmark is known. Current source, voltage source and resistance values can also be obtained easily. Since there is no wire length and width information, we made some assumptions including wire length and layer height for the experiments. The maximum allowable IR drop is assumed to be 10% V_{dd} and the minimum allowable width is $0.1\mu\text{m}$. Some important parameters used in our experiments are listed in Table I.

TABLE I: Parameters used in the optimization process

Parameters	Value	Parameters	Value
σ_{crit}	500MPa	Ω	$1.182 \times 10^{-29}\text{m}^3$
V_{crit}	$3.69 \times 10^{-3}\text{V}$	E_a	0.8eV
T	323K	D_0	$5.55 \times 10^{-8}\text{m}^2/\text{s}$
B	140GPa	ρ_{Cu}	$1.9 \times 10^{-8}\Omega \cdot \text{m}$
Z	10	ρ_{Ta}	$1.35 \times 10^{-7}\Omega \cdot \text{m}$

B. EM immortality constrained power supply optimization results

Table II compares the results of the new optimization method considering saturation volume with the results of the existing P/G optimization method checking EM nucleation phase immortal only [14].

In the optimization process, we assume that all the branches have the same width on one tree but different trees can have different widths. For fair comparison, we only allow the difference in the EM constraints. In Table II, column 1 to 5 list the P/G network benchmarks (*circuit*), the number of interconnect trees (*# tree*), the number of nucleated wires at the beginning (*# nuc-wires (b)*), the number of nucleated wires at the end (*# nuc-wires (e)*), and the original area (*area (mm²)*). Column 6 and 7 report the reduced chip area ratio (*area reduced (%)*) with respect to the original area for the two methods with EM nucleation phase immortal only constraint (*w/o saturation volume*) and the new EM immortality criteria (*with saturation volume*) respectively. Note that for the two methods, all the wires are EM immortal after optimization.

As we can see, for *ibmpg2* example, which has 462 immortal trees at the beginning, the original area is 60.38mm^2 . After 2 iterations, the area can have 77.55% reduction without any EM violation. For *pg2*, all the wires are EM nucleation phase immortal at first, after 2 iterations, although it has 9 nucleated wires, all of them are EM incubation phase immortal. Compared with the previous work [14] which has about 28.78% reduction, the new method has better performance in terms of area reduction, while still ensuring EM immortality. Previous work can not size *pg3* because it has nucleated wires in the beginning. Since the nucleated wires can still pass the saturation volume check (it is incubation immortal (II)), the P/G network can be sized properly with the new method. Note that the area improvement strongly depends on the original layouts, thus the absolute values of reduced area are not that important.

We further observe that the new method typically leads to more area reduction compared to the previous method. The reason is that the new EM immortality criteria is less conservative and thus it effectively allows the *EM voltage* to exceed the *critical EM voltage* by using the *EM incubation phase immortal* constraint. In other words, larger current density which can nucleate a void is allowed in the new method while ensuring wire resistance is not affected. As a result, we can conclude that the new method successfully enables the optimization of power grids, which would have been impossible in the previous method due to the conservative immortality constraint, in addition to leading to further area reduction in power grids compared to the previous method.

C. EM immortality constrained power supply optimization results with pre-wire-sizing

The result of the EM immortality constrained power supply optimization with sizing up are also shown in Table II. There exist some benchmarks which do not satisfy the EM requirement in the initial situation, in this way, we check if the interconnects can be sized up to become incubation phase immortal. In *pg4* example, we find that there are one nucleated wires (fail both immortality constraints) in the beginning. As discussed in subsection IV-B, after width adjustment (increase), it becomes incubation phase immortal. For *pg5*, half of the interconnects are mortal at first, all become nucleation phase immortal after pre-wire-sizing. As a result, the optimization process can finish successfully.

D. EM lifetime constrained power supply optimization results

pg6 and *pg7* in Table II demonstrated the lifetime constrained optimization case. In *pg6* example, the lifetime of the nucleated wires are longer than 100 years, thus the difference between the previous method and the new method is the relaxed constraint. In *pg7* example, before optimization, the shortest lifetime among the 11 nucleated wires is 5.53 years, which violates the lifetime constraint. After the optimization, the lifetime was improved to 17.02 years. As we can see from this example, lifetime can be extended while area can still be saved. The reason is that the open circuit or resistance change of the short-lifetime wires will be compensated by properly sizing of other wires to meet the lifetime requirement due to redundant

TABLE II: Results of EM immortality and lifetime constrained P/G optimization considering void saturation volume

circuit	# tree	# nuc-wires (b)	# nuc-wires (e)	area (mm ²)	w/o saturation volume [14]	with saturation volume
					area reduced (%)	area reduced (%)
ibmpg2	462	0	0	60.38	77.55	77.55
pg1	128	0	0	40.21	34.34	34.34
pg2	38	0	9	0.50	28.78	38.33
pg3	9	1	3	0.031	can't finish (with mortal wires (II))	53.26
pg4	12	1	1	0.030	can't finish (with mortal wires)	25.21
pg5	20	10	10	0.017	can't finish (with mortal wires)	14.84
pg6	20	2	2	0.23	27.39	28.41
pg7	80	11	11	1.28	26.68	29.76

structure design of P/G networks. It may lead to wider width, but the overall area of all the wires can be reduced. This further demonstrates the superior advantage of the lifetime constrained method over the immortality constrained method. For the cases with very long lifetime wires, even though they may have a few nucleated wires, after optimization, this is still the case. Besides, compared with previous method, the void saturation volume based method can lead to more area reduction.

VI. CONCLUSION

In this paper, we have proposed a new on-chip power grid network optimization technique to consider the EM void saturation volume for multi-segment interconnects, which has never been exploited in existing methods. We showed that the new saturation volume immortality constraints can be integrated into the existing programming based power grid optimization framework. To further mitigate the overly-conservative problem of the existing immortality-constrained methods, we explored two strategies: first we size up wires to be failed to meet one of immortality conditions subject to design rules; second, the EM-induced aging effects on power supply networks was further considered, which allows some short-lifetime wires to fail and optimizes the rest of the wires. Numerical results on a number of IBM and self-generated power supply networks demonstrate that the new method outperforms the existing immortality constrained optimizations in terms of area reduction. Furthermore, the proposed method can optimize power grids with EM nucleated wires, which would not be possible with the existing immortality constrained methods.

REFERENCES

- [1] "IEEE International Roadmap for Devices and Systems (IRDS)," 2018. <http://irds.ieee.org/>.
- [2] "International Technology Roadmap for Semiconductors 2.0 (ITRS 2.0)," 2015. <http://www.itrs2.net/itrs-reports.html>.
- [3] J. R. Black, "Electromigration-A Brief Survey and Some Recent Results," *IEEE Trans. on Electron Devices*, vol. 16, no. 4, pp. 338–347, 1969.
- [4] H. B. Bakoglu, *Circuits, Interconnections, and Packaging for VLSI*. Addison-Wesley Pub. Co., 1990.
- [5] Q. K. Zhu, *Power distribution network design for VLSI*. John Wiley & Sons, Inc., 2004.
- [6] F. Chen, O. Bravo, K. Chanda, P. McLaughlin, T. Sullivan, J. Gill, J. Lloyd, R. Kontra, and J. Aitken, "A Comprehensive Study of Low-k SiCOH TDDDB Phenomena and Its Reliability Lifetime Model Development," in *IEEE Int. Reliability Physics Symposium (IRPS)*, pp. 46–53, Mar. 2006.
- [7] S. Chowdhury and M. Breuer, "Minimal Area Design of Power/Ground Nets Having Graph Topologies," *IEEE Trans. on Circuits and Systems*, vol. 34, no. 12, pp. 1441–1451, 1987.
- [8] S. Chowdhury and M. A. Breuer, "Optimum Design of IC Power/Ground Nets Subject to Reliability Constraints," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 7, no. 7, pp. 787–796, 1988.
- [9] S. Chowdhury, "Optimum Design of Reliable IC Power Networks Having General Graph Topologies," in *Proc. Design Automation Conf. (DAC)*, pp. 787–790, Jun. 1989.
- [10] R. Dutta and M. Marek-Sadowska, "Automatic Sizing of Power/Ground (P/G) Networks in VLSI," in *Proc. Design Automation Conf. (DAC)*, pp. 783–786, Jun. 1989.
- [11] X.-D. Tan, C.-J. Shi, and J.-C. Lee, "Reliability-Constrained Area Optimization of VLSI Power/Ground Networks Via Sequence of Linear Programmings," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 12, pp. 1678–1684, 2003.
- [12] S. X.-D. Tan and C.-J. R. Shi, "Efficient Very Large Scale Integration Power/Ground Network Sizing Based on Equivalent Circuit Modeling," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 3, pp. 277–284, 2003.
- [13] K. Wang and M. Marek-Sadowska, "On-Chip Power-Supply Network Optimization Using Multigrid-Based Technique," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 3, pp. 407–417, 2005.
- [14] H. Zhou, Y. Sun, Z. Sun, H. Zhao, and S. X.-D. Tan, "Electromigration-Lifetime Constrained Power Grid Optimization Considering Multi-Segment Interconnect Wires," in *Proc. Asia South Pacific Design Automation Conf. (ASPDAC)*, pp. 399–404, Jan. 2018.
- [15] C. V. Thompson, S. P. Hau-Riege, and V. K. Andleigh, "Modeling and experimental characterization of electromigration in interconnect trees," in *Proc. AIP Conference*, vol. 491, pp. 62–73, 1999.
- [16] S. P. Hau-Riege and C. V. Thompson, "Experimental characterization and modeling of the reliability of interconnect trees," *Journal of Applied Physics*, vol. 89, no. 1, pp. 601–609, 2001.
- [17] V. Sukharev, A. Kteyan, E. Zschech, and W. D. Nix, "Microstructure Effect on EM-Induced Degradations in Dual Inlaid Copper Interconnects," *IEEE Trans. on Device and Materials Reliability*, vol. 9, no. 1, pp. 87–97, 2009.
- [18] X. Huang, A. Kteyan, S. X.-D. Tan, and V. Sukharev, "Physics-Based Electromigration Models and Full-Chip Assessment for Power Grid Networks," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, no. 11, pp. 1848–1861, 2016.
- [19] S. Chatterjee, V. Sukharev, and F. N. Najm, "Power Grid Electromigration Checking using Physics-Based Models," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, no. 7, pp. 1317–1330, 2018.
- [20] V. Mishra and S. S. Sapatnekar, "Predicting Electromigration Mortality Under Temperature and Product Lifetime Specifications," in *Proc. Design Automation Conf. (DAC)*, pp. 1–6, Jun. 2016.
- [21] S. X.-D. Tan, H. Amrouch, T. Kim, Z. Sun, C. Cook, and J. Henkel, "Recent advances in EM and BTI induced reliability modeling, analysis and optimization," *Integration, the VLSI Journal*, vol. 60, pp. 132–152, Jan. 2018.
- [22] H. Zhou, Z. Sun, S. Sadiqbacha, N. Chang, and S. X.-D. Tan, "EM-Aware and Lifetime-Constrained Optimization for Multisegment Power Grid Networks," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 4, pp. 940–953, 2019.
- [23] Z. Sun, E. Demircan, M. D. Shroff, C. Cook, and S. X.-D. Tan, "Fast Electromigration Immortality Analysis for Multisegment Copper Interconnect Wires," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, no. 12, pp. 3137–3150, 2018.
- [24] Z. Sun, S. Sadiqbacha, H. Zhao, and S. X.-D. Tan, "Accelerating Electromigration Aging for Fast Failure Detection for Nanometer ICs," in *Proc. Asia South Pacific Design Automation Conf. (ASPDAC)*, pp. 623–630, Jan. 2018.
- [25] Z. Sun, S. Sadiqbacha, H. Zhao, and S. X.-D. Tan, "Saturation-Volume Estimation for Multisegment Copper Interconnect Wires," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 7, pp. 1666–1674, 2019.
- [26] Z. Sun, E. Demircan, M. D. Shroff, T. Kim, X. Huang, and S. X.-D. Tan, "Voltage-Based Electromigration Immortality Check for General Multi-Branch Interconnects," in *Proc. Int. Conf. on Computer Aided Design (ICCAD)*, pp. 1–7, Nov. 2016.
- [27] X. Wang, H. Wang, J. He, S. X.-D. Tan, Y. Cai, and S. Yang, "Physics-based Electromigration Modeling and Assessment for Multi-Segment Interconnects in Power Grid Networks," in *Proc. Design, Automation and Test In Europe Conf. (DATE)*, pp. 1727–1732, Mar. 2017.
- [28] S. R. Nassif, "Power Grid Analysis Benchmarks," in *Proc. Asia South Pacific Design Automation Conf. (ASPDAC)*, pp. 376–381, Mar. 2008.