Scaling of Power Generation With Dopant Density in Integrated Circuit Silicon Thermoelectric Generators

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***Abstract*—Integrated circuit (IC) thermoelectric generators (TEGs) fabricated by standard "65 nm" Si processing have been shown to be potentially competitive with (Bi, Sb)$_2$Te$_3$ TEGs in terms of maximum power generated, P_{max}, per conduction cross-sectional area at a given temperature difference. Optimization of P_{max} in these Si IC TEGs with respect to design and processing parameters remains an open issue. Here the dependence of P_{max} on dopant density in Si thermopiles is examined both experimentally and by developing a simple physics-based model using empirical material parameters. Experimentally, P_{max} improved by ~1.8× with increasing dopant density from 3 × 10^{17} to 4 × 10^{18} cm^{-3}. Modeling shows that $P_{max} \propto$ thermopile figure-of-merit ZT, which scales with dopant density approximately as (density)$^{0.24}$ from 10^{17} to 10^{19} cm^{-3}. A model extrapolation to 10^{20} cm^{-3} predicts that parasitic resistance and thermal conductance will cause Z and P_{max} to have a maximum at densities above 10^{19} cm^{-3} and then decline at higher densities. Without parasitics Z and P_{max} would continue to increase roughly as (density)$^{0.4}$. The results emphasize the importance of minimizing parasitics.**

***Index Terms*—Thermoelectric, thermoelectric generators, energy harvesting.**

I. Introduction

THERMOELECTRIC generators (TEGs) are attractive as an environmentally clean technology for converting waste heat into electrical power. Integrated circuit (IC) TEGs have recently become of interest. These TEGs are aimed at microelectronic circuit/sensor applications, such as on-chip thermal management [1], bio-thermal power [2], low temperature heat harvesting [3], and energizing or actuating microelectronic sensors [4], [5].

Most TEG research has focused on high TE figure-of-merit, $zT = (S^2/\rho\kappa)T$, materials, where S is the Seebeck coefficient, ρ the electrical resistivity, κ the thermal conductivity, and T the mean operating temperature (in K). [We use $z = (S^2/\rho\kappa)$ for a single material, and Z is the equivalent for a two-material thermopile.] Materials such as (Bi, Sb)$_2$Te$_3$ or PbTe have $zT \approx 1$ near 300 K, while bulk Si has $zT \sim 10^{-3}$ to 10^{-2} [6]. Thus, Si is usually not considered a viable material for TE applications.

In 2008 two groups reported [7], [8] that Si nanowires can have zT up to 0.6, competitive with more exotic TE materials. While this prompted efforts [4], [9]–[12] to make Si TEGs with nanostructured Si thermopiles, these works did not find efficiencies or power generation capabilities competitive with high zT material technologies.

We recently reported [13] on Si IC TEGs fabricated using an industrial "65 nm node" process line. The best device generated maximum power, P_{max}, of 204 nW over an area of 48 μm × 36 μm operating between 295 K and 315 K. Such performance is comparable to most (Bi, Sb)$_2$Te$_3$ TEGs, even though Si TEGs have much smaller ZT. In this paper we examine the dependence of P_{max} on dopant density in these Si IC TEGs. We find empirically and with a physics-based model that P_{max} and ZT scale with average dopant density, $\eta = 1/2\ (n + p)$, where n and p are the dopant densities of the n- and p-doped sides of the thermopile, approximately as $\eta^{0.24}$ for η from 10^{17} to 10^{19} cm^{-3}, including realistic parasitic resistance and thermal conductance. From modeling, as $\eta \rightarrow 10^{20}$ cm^{-3} these parasitics cause ZT and P_{max} to have a maximum above 10^{19} cm^{-3} and subsequently decline, whereas without parasitics ZT and P_{max} would continue to increase approximately as $\eta^{0.4}$.

II. Thermoelectric Generator Devices

The structure of the Si IC TEGs is described in detail elsewhere [13] and is summarized here. Fig. 1(a) is a sketch of the side view of a thermocouple comprising the thermopile. The basic TE elements were n- and p-doped Si "blades" of nominal dimensions 80 nm width × 750 nm length × 350 nm height. These blades were, etched from n$^+$- or p$^+$-doped wells. Fig. 1(b) is a scanning electron microscope image of a 4-blade group. A thermopile consisted of 100 to 150 groups with a total conduction cross-sectional area $A = 48\ \mu$m × 36 μm.

A resistive heater with known temperature coefficient was integrated on-chip to set temperature T_H. An embedded thermometer in the probe station chuck read $T_C \approx 295$ K.

A TEG circuit consisted of a thermopile and metallization to electrically connect and conduct heat to the blades. Circuit layout variations differed in number of blades per group, number of groups per thermopile, and metallization. Layouts were

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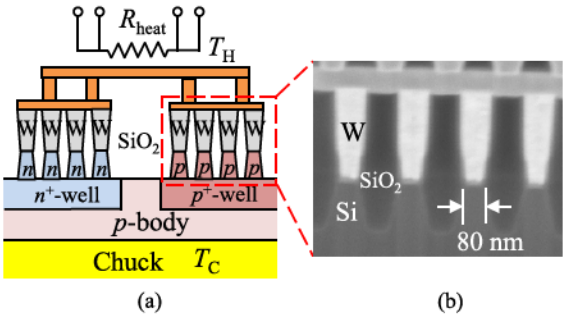

Fig. 1. (a) Illustration (not to scale) of the cross-section of an n-p thermocouple. The n- and p-blades are grouped in sets of four, each blade contacted on top by a tungsten (W) plug. SiO_2 is used as a spacing filler. (b) SEM cross-section image of a 4-blade group.

TABLE I
WAFER QUADRANT VARIATIONS

Quad	n (cm^{-3})	p (cm^{-3})	Θ_{tot} (K/W) of Layout: 1	2	3	4	5
I	4.3E+17	2.2E+17	594	448	613	1230	532
II	8.9E+17	7.6E+17	623	429	643	1204	550
III	1.9E+18	1.9E+18	613	430	625	1163	528
IV	3.9E+18	4.3E+18	604	452	620	1187	552

repeated over a wafer divided into quadrants with different n^+- and p^+-well densities. Table I lists densities n and p determined by technical computer-aided design (TCAD).

III. Data and Model

Fig. 2(a) shows current-voltage-power (I-V-P) data at various $\Delta T = T_H - T_C$ on one device under test (DUT) from quadrant III. A linear V-I offsets away from the origin with increasing ΔT. The slope $|\Delta V/\Delta I|$ is the source resistance, R_S. The open-circuit voltage, V_{OC}, and short-circuit current, I_{SC}, are the intercepts of V-I with the V and I axes. The power, $P = VI$, has maximum $P_{max} = 1/4 V_{OC} I_{SC}$ = power generated to a load resistance $R_L = R_S$ (matched load). Fig. 2(b) shows that P_{max} is a linear function of $(\Delta T)^2$. The slope of the fitted line is $2.8 \times 10^{-4} \mu W \cdot K^{-2}$. Normalizing to A gives a specific power density of $16\ \mu W \cdot cm^{-2} K^{-2}$. Fig. 2(c) shows ΔT vs. heater power Q. The slope of the fitted line gives the total thermal impedance, $\Theta_{tot} = 613$ K/W, which includes all parasitic impedances.

Measurements of the kind shown in Fig. 2 were conducted on a series of DUTs. DUTs of the same layout in the same quadrant reproduced I-V-P and Θ_{tot} to within ±5% of the mean. To test dopant density dependence, DUTs of identical layout were taken from each quadrant. Five TEG layouts were used. Table I gives Θ_{tot} for these layouts from each quadrant.

Fig. 3 shows the normalized P_{max} at $\Delta T = 20$ K, interpolated from fits like in Fig. 2(b), vs. average density η in each quadrant. P_{max} is arbitrarily normalized to quadrant I DUT values which are, in order for Layouts 1 to 5 (in nW): 71, 58, 51, 20, and 55. For any given layout, P_{max} in quadrant IV is ~1.8× higher than in quadrant I. The inset is the same data on a log-log plot. The slope of the dashed reference line shows that P_{max} scales approximately as $\eta^{0.24}$ for all layouts.

Using $R_L = R_S$ in the general expression for thermopile efficiency in Ref. 14 and applying it to Si TEGs

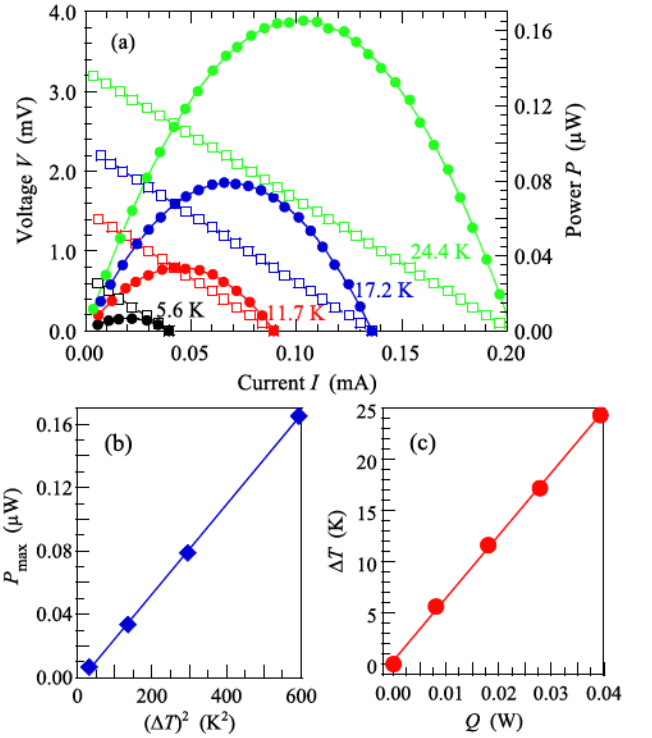

Fig. 2. (a) Voltage (open squares) and Power (solid circles) vs. current at $\Delta T = 5.6$ K (black), 11.7 K (red), 17.2 K (blue) and 24.4 K (green) for a representative TEG. The lines are linear (for V-I) and quadratic (for P-I) fits. (b) Maximum power $P_{max} = 1/4 V_{OC} I_{SC}$ vs. $(\Delta T)^2$ from the data in (a). The solid line is a linear fit. (c) ΔT vs. heater power Q for the DUT in (a). The solid line is a linear fit.

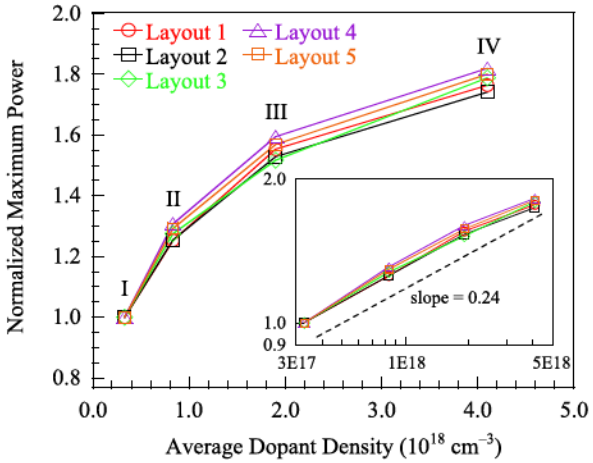

Fig. 3. Normalized P_{max} (at $\Delta T = 20$ K) for five different layouts vs. average dopant density in the quadrant each DUT was from. Values are normalized to DUTs from quadrant I. Inset: Same data on a log-log plot. The dashed black line is a reference showing a slope of 0.24.

where $ZT \ll 1$ [4], [9]–[13], we obtain to leading order in Z:

$$P_{max} \propto \frac{1}{\Theta_{tot}} (T_H - T_C)^2 Z \quad (1)$$

where we used $Q = \Delta T/\Theta_{tot}$ as the heat flow in. From Table I, Θ_{tot} depends on circuit layout, but for any given layout Θ_{tot} varies by $< \pm 3\%$ about the mean across a decade of η. Previous thermal impedance modeling [13] indicated that Θ_{tot} is dominated by circuit-dependent series thermal impedances from heater to thermopile and from thermopile to chuck which

are independent of n and p. Thus the density scaling of P_{max} should be determined almost entirely by Z.

For a thermopile composed of p- and n-type elements [15]

$$Z = (S_p - S_n)^2/RK \tag{2}$$

where S_p and S_n are the Seebeck coefficients, R is the electrical resistance and K the thermal conductance of the thermopile. In our TEGs each Si blade has conduction area a and length λ. The n- and p-sides are connected electrically in series and thermally in parallel, so

$$R = [\rho_n/N_n + \rho_p/N_p](\lambda/a) + R_0 \tag{3a}$$

$$K = [N_n\kappa_n + N_p\kappa_p](a/\lambda) + K_0 \tag{3b}$$

where N_n, N_p are the number of n- and p-blades, R_0 is a parasitic series resistance, and K_0 is a parasitic thermal conductance for heat flow that bypasses the TE elements. Note that if $R_0 = K_0 = 0$, the product RK is independent of a and λ.

A parabolic band model [16] gives $S \propto (\text{density})^{-2/3}$. However, Ohishi, *et al.* [6] reviewed how S_p and S_n in Si depend on n and p from 10^{17} to 10^{20} cm^{-3} and found a logarithmic dependence. We find the following describe their data well:

$$S_p = [3743.5 - 177.43\log(p/\text{cm}^{-3})]\mu\text{V}\cdot\text{K}^{-1} \tag{4a}$$

$$S_n = [-3817.3 + 179.56\log(n/\text{cm}^{-3})]\mu\text{V}\cdot\text{K}^{-1} \tag{4b}$$

For n, $p < 10^{18}$ cm^{-3}, Refs. 17 and 18 showed that $\kappa_p \approx \kappa_n \approx 1.27 \pm 0.03$ Wcm^{-1}K^{-1} near 300 K, reflecting the dominant role of phonons in thermal conduction near room temperature. For n, $p \geq 10^{18}$ cm^{-3}, Ref. 6 compiled data from many sources. We fit the data in Ref. 6 from 10^{18} to 10^{20} cm^{-3} and found that $\kappa_{p,n} = [1.27 - 0.0986(\log n - 18)^2 - 0.00205(\log n - 18)^4]$ Wcm^{-1}K^{-1}, where n stands for either n- or p-density in units of cm^{-3}, describes the data well for both n- and p-type Si.

The monotonic decrease of ρ_n and ρ_p with increasing n, p has been thoroughly studied and modeled [19]. On-line calculators [20] give ρ_n and ρ_p for specified dopant species and density.

Ref. 13 gives a quantitative model of electrical and thermal impedances in our IC TEGs. From this model, contact metallization and spreading resistance give R_0 between 2.0 to 2.5 Ω. K_0 is due to leakage heat flow through the SiO_2 filler in Fig. 1 and is between 0.010 to 0.015 WK^{-1}. For model calculations we use $R_0 = 2.2$ Ω and $K_0 = 0.125$ WK^{-1}. This $K_0 \approx$ that of the Si blades, which have a much higher κ but occupy a much smaller area compared to SiO_2. Consequently, if K_0 could be eliminated, Z would roughly double.

Fig. 4 shows Z calculated using the above expressions and P_{max} data for Layout 5, both vs. η on a log-log plot. Both y-axes span two decades. For η from 10^{17} to 10^{19} cm^{-3}, $(S_p–S_n)^2$ from Eq. 4 decreases but the product RK using Eq. 3 decreases faster, causing Z from Eq. 2 to increase as a power law. Over the η covering wafer quadrants I to IV, the calculated Z with parasitics correctly accounts for the empirical scaling of Fig. 3 and Eq. 1, *i.e.*, $P_{max} \propto Z \sim \eta^{0.24}$, as indicated by the dashed black reference line with slope of 0.24. At higher η $(S_p–S_n)^2$ continues to decrease but RK cannot decrease below the parasitic lower bound R_0K_0 from

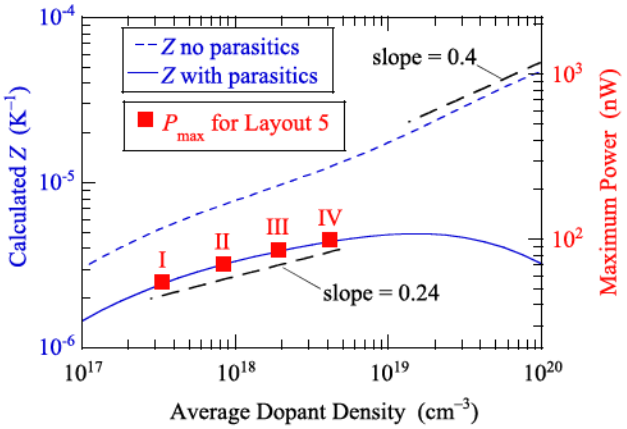

Fig. 4. Calculated Z, with and without parasitics, and measured P_{max} for Layout 5 vs. average density η on a log-log plot. Both y-axes span two decades. Black dashed lines are references with slopes as indicated.

Eq. 3, causing Z to go through a maximum for η above 10^{19} cm^{-3} and then decline as $\eta \to 10^{20}$ cm^{-3}.

With no parasitics ($R_0 = K_0 = 0$) Eq. 3 shows the product RK is always smaller than with parasitics, giving a larger scaling exponent of 0.4, as indicated in Fig. 4 by the dashed black reference line with slope = 0.4. Also, R and K will decrease faster than $(S_p–S_n)^2$ as $\eta \to 10^{20}$ cm^{-3} but without lower bound, so Z continues to increase as $\eta^{0.4}$. No physical theory currently explains why the density dependencies of S, ρ, and κ should conspire to give a power law with scaling exponent of 0.4.

Power scaling with dopant density in our TEGs is accurately modeled using properties of bulk doped Si. This may appear surprising since Si nanomaterials are thought to have much higher z compared to bulk [7], [8], [21]–[23]. However, no Si nano-structure TEGs we know of have reported Z distinguishably greater than that expected of bulk doped Si [4], [9]–[13]. It is unclear why higher nanomaterial z has not translated to higher thermopile Z. Our previous work [13] found that achieving a generated power density that rivals that of $(Bi, Sb)_2Te_3$ TEGs resulted not from improving Z, but from the ability of Si processing to fabricate a very high number of thermocouples per cm^2 with precise enough control to minimize parasitic resistances and optimize thermal impedance matching.

IV. Summary

In a set of Si IC TEGs fabricated using 65 nm technology, P_{max} depended on TEG circuit layout, but the relative increase of P_{max} with thermopile dopant density η was independent of layout. A physics-based model shows that $P_{max} \propto$ thermopile Z. An expression for Z was evaluated as a function of η using literature values of the TE properties of Si. This model indicates that P_{max} will increase at higher η than used in our TEGs, but parasitics will ultimately cap Z and P_{max}. Significant improvement in P_{max} can be expected upon reducing parasitics.

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REFERENCES

[1] I. Chowdhury, R. Prasher, K. Lofgreen, G. Chrysler, S. Narasimhan, R. Mahajan, D. Koester, R. Alley, and R. Venkatasubramanian, "On-chip cooling by superlattice-based thin-film thermoelectrics," *Nature Nanotechnol.*, vol. 4, no. 4, pp. 235–238, Jan. 2009. doi: 10.1038/nnano.2008.417.

[2] A. R. M. Siddique, S. Mahmud, and B. Van Heyst, "A review of the state of the science on wearable thermoelectric power generators (TEGs) and their existing challenges," *Renew. Sustain. Energy Rev.*, vol. 73, pp. 730–744, Jun. 2017. doi: 10.1016/j.rser.2017.01.177.

[3] C.-T. Hsu, G.-Y. Huang, H.-S. Chu, B. Yu, and D.-Y. Yao, "Experiments and simulations on low-temperature waste heat harvesting system by thermoelectric power generators," *Appl. Energy*, vol. 88, no. 4, pp. 1291–1297, Apr. 2011. doi: 10.1016/j.apenergy.2010.10.005.

[4] M. Tomita, S. Oba, Y. Himeda, R. Yamato, K. Shima, T. Kumada, M. Xu, H. Takezawa, K. Mesaki, K. Tsuda, S. Hashimoto, T. Zhan, H. Zhang, Y. Kamakura, Y. Suzuki, H. Inokawa, H. Ikeda, T. Matsukawa, T. Matsuki, and T. Watanabe, "Modeling, simulation, fabrication, and characterization of a 10-μW/cm$_2$ class Si-nanowire thermoelectric generator for IoT applications," *IEEE Trans. Electron Devices*, vol. 65, no. 11, pp. 5180–5188, Nov. 2018. doi: 10.1109/TED.2018.2867845.

[5] A. Tarancón, "Powering the IoT revolution with heat," *Nature Electron.*, vol. 2, pp. 270–271, Jul. 2019. doi: 10.1038/s41928-019-0276-4.

[6] Y. Ohishi, J. Xie, Y. Miyazaki, Y. Aikebaier, H. Muta, K. Kuorsaki, S. Yamanaka, N. Uchida, and T. Tada, "Thermoelectric properties of heavily boron- and phosphorus-doped silicon," *Jpn. J. Appl. Phys.*, vol. 54, no. 7, Jun. 2015, Art. no. 071301. doi: 10.7567/JJAP.54.071301.

[7] A. I. Hochbaum, R. Chen, R. D. Delgado, W. Liang, E. C. Garnett, M. Najarian, A. Majumdar, and P. Yang, "Enhanced thermoelectric performance of rough silicon nanowires," *Nature*, vol. 451, pp. 163–167, Jan. 2008. doi: 10.1038/nature06381.

[8] A. I. Boukai, Y. Bunimovich, J. Tahir-Kheli, J.-K. Yu, W. A. Goddard, III, and J. R. Heath, Jr., "Silicon nanowires as efficient thermoelectric materials," *Nature*, vol. 451, pp. 168–171, Jan. 2008. doi: 10.1038/nature06458.

[9] Y. Li, K. Buddharaju, N. Singh, G. Q. Lo, and S. J. Lee, "Chip-level thermoelectric power generators based on high-density silicon nanowire array prepared with top-down CMOS technology," *IEEE Electron Device Lett.*, vol. 32, no. 5, pp. 674–676, May 2011. doi: 10.1109/LED.2011.2114634.

[10] D. Dávila, A. Tarancón, C. Calaza, M. Salleras, M. Fernández-Regúlez, A. S. Paulo, and L. Fonseca, "Monolithically integrated thermoelectric energy harvester based on silicon nanowire arrays for powering micro/nanodevices," *Nano Energy*, vol. 1, pp. 812–819, Nov. 2012. doi: 10.1016/j.nanoen.2012.06.006.

[11] J. Xie, C. Lee, and H. Feng, "Design, fabrication, and characterization of CMOS MEMS-based thermoelectric power generators," *J. Micromech. Syst.*, vol. 19, no. 2, pp. 317–324, Apr. 2010. doi: 10.1109/JMEMS.2010.2041035.

[12] G. Gadea, M. Pacios, A. Morata, and A. Tarancón, "Silicon-based nanostructures for integrated thermoelectric generators," *J. Phys. D, Appl. Phys.*, vol. 51, Aug. 2018, Art. no. 423001. doi: 10.1088/1361-6463/aad683.

[13] G. Hu, H. Edwards, and M. Lee, "Silicon integrated circuit thermoelectric generators with a high specific power generation capacity," *Nature Electron.*, vol. 2, pp. 300–306, Jul. 2019. doi: 10.1038/s41928-019-0271-9.

[14] Z. Tian, S. Lee, and G. Chen, "Comprehensive review of heat transfer in thermoelectric materials and devices," *Ann. Rev. Heat Transf.*, vol. 17, pp. 425–483, 2014. doi: 10.1615/AnnualRevHeatTransfer.2014006932.

[15] G. S. Nolas, J. Sharp, and J. Goldsmid, *Thermoelectrics: Basic Principles and New Materials Developments*. New York, NY, USA: Springer, 2001, pp. 8–10.

[16] M. Cutler, J. F. Leavy, and R. L. Fitzpatrick, "Electronic transport in semimetallic cerium sulfide," *Phys. Rev. J. Arch.*, vol. 133, pp. A1143–A1152, Feb. 1964. doi: 10.1103/PhysRev.133.A1143.

[17] M. Asheghi, K. Kurabayashi, R. Kasnavi, and K. E. Goodson, "Thermal conduction in doped single-crystal silicon films," *J. Appl. Phys.*, vol. 91, no. 8, pp. 5079–5088, 2002. doi: 10.1063/1.1458057.

[18] A. Stranz, J. Kähler, A. Waag, and E. Peiner, "Thermoelectric properties of high-doped silicon from room temperature to 900 K," *J. Electron. Mater.*, vol. 42, no. 7, pp. 2381–2387, Jul. 2013. doi: 10.1007/s11664-013-2508-0.

[19] G. Masetti, M. Severi, and S. Solmi, "Modeling of carrier mobility against carrier concentration in arsenic-, phosphorus-, and boron-doped silicon," *IEEE Trans. Electron Devices*, vol. ED-30, no. 7, pp. 764–769, Jul. 1983. doi: 10.1109/T-ED.1983.21207.

[20] *Resistivity & Mobility Calculator/Graph for Various Doping Concentrations in Silicon*. Accessed: Oct. 16, 2019. [Online]. Available: http://www.cleanroom.byu.edu/ResistivityCal

[21] L. Shi, D. Yao, G. Zhang, and B. Li, "Size dependent thermoelectric properties of silicon nanowires," *Appl. Phys. Lett.*, vol. 95, no. 6, Aug. 2009, Art. no. 063102. doi: 10.1063/1.3204005.

[22] X. Zianni, "Monte Carlo simulations on the thermoelectric transport properties of width-modulated nanowires," *J. Electron. Mater.*, vol. 45, no. 3, pp. 1779–1785, Mar. 2016. doi: 10.1007/s11664-015-4217-3.

[23] S. Karg, P. Mensch, B. Gotsmann, H. Schmid, P. D. Kanungo, H. Ghoneim, V. Schmidt, M. T. Björk, V. Troncale, and H. Riel, "Measurement of thermoelectric properties of single semiconductor nanowires," *J. Electron. Mater.*, vol. 42, no. 7, pp. 2409–2414, Jul. 2013. doi: 10.1007/s11664-012-2409-7.