Field-Plated Ga$_2$O$_3$ Trench Schottky Barrier Diodes with a BV^2/$R_{on,sp}$ of up to 0.95 GW/cm^2

Wenshen Li, *Student Member, IEEE*, Kazuki Nomoto, *Member, IEEE*, Zongyang Hu, Debdeep Jena, *Senior Member, IEEE*, and Huili Grace Xing, *Senior Member, IEEE*

Abstract—We report the realization of field-plated vertical Ga$_2$O$_3$ trench Schottky barrier diodes (SBDs). The trench SBDs show significantly lower leakage current than regular SBDs. With employment of field plate, a breakdown voltage (BV) of 2.89 kV is achieved, which is ~500 V higher than those without field plate. Trench sidewall depletion is observed, and the average depletion width is extracted using an analytical model. The trench SBDs have a differential specific on-resistance ($R_{on,sp}$) of 10.5 (8.8) mΩ·cm^2 from DC (pulsed) measurements, which leads to a Baliga's figure-of-merit (BV^2/$R_{on,sp}$) of 0.80 (0.95) GW/cm^2 — the highest among Ga$_2$O$_3$ power devices to date.

Index Terms—Ga$_2$O$_3$, Schottky diodes, Power semiconductor devices, HVPE, Wide band gap semiconductors, MIS devices

I. Introduction

BETA-GA$_2$O$_3$ is seen as a promising ultra-wide-bandgap material for power semiconductor devices. On top of the ultra-high critical electric-field (E_c) of ~8 MV/cm [1][2], which leads to a projected Baliga's figure-of-merit (FOM) higher than those of SiC and GaN [1], β-Ga$_2$O$_3$ enjoys readily available melt-grown substrates [3], which enable high-quality homoepitaxy as well as a potentially low-cost device platform [4]. The device performance is rapidly progressing in recent years in both lateral and vertical topologies. Over 2 kV breakdown voltage (BV) has been achieved in both lateral Schottky barrier diodes (SBDs) [5] and lateral transistors [6][7]. For high voltage and high current applications, vertical power devices are typically preferred over lateral devices. To date, normally-off vertical fin transistors have been demonstrated with a BV up to 1.6 kV [8][9], alongside with a number of
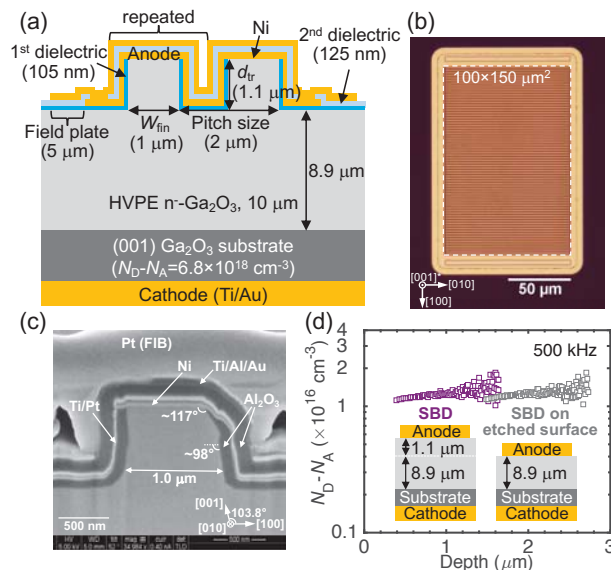
Fig. 1. (a) Schematic cross-section of the field-plated Ga$_2$O$_3$ trench SBDs. (b) Top-view optical image of a fabricated device, where the active device region is outlined by a white dashed rectangle with an area of 100×150 μm^2. (c) Cross-sectional SEM image of a fin channel. (d) Extracted N_D-N_A profile from *C-V* measurements on regular diodes with a diameter of 200 μm. Inset: schematic cross-section of the two types regular diodes.

reports on vertical SBDs with a BV exceeding 1 kV [10-18].

Despite the encouraging demonstrations of high BV, the Baliga's FOM (BV^2/$R_{on,sp}$, $R_{on,sp}$ being the differential specific on-resistance of the device) of the present Ga$_2$O$_3$ power devices is still much lower than the material limit, with a highest value of 0.6 GW/cm^2 reached in vertical Schottky barrier diodes [16][17]. To reach the projected high FOM in Ga$_2$O$_3$, a high parallel-plane electric-field close to E_c has to be sustained. In the case of vertical SBDs with a typical barrier height of <1.5 eV, however, the surface electric field has to be suppressed to a value much lower than E_c; otherwise the leakage current will be excessive [19]. These seemingly conflicting requirements can be fulfilled by the trench MOS barrier Schottky (TMBS) structure (here referred to as trench SBD) [20], which possesses the much-needed charge-coupling effect for surface field reduction without requiring p-type doping. Effective leakage reduction in Ga$_2$O$_3$ trench SBDs has been demonstrated [21,13-16], as well as an increase of the BV with respect to the regular SBDs, with a highest BV of 2.44 kV [15].

Through the analysis of our previous trench SBDs, we found that the BV is limited by field crowding at either the trench
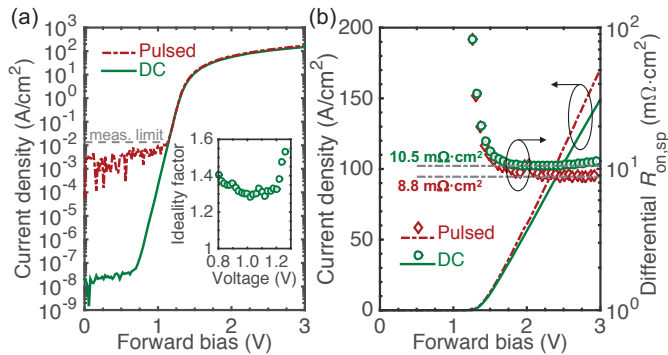
Fig. 2. Forward *I-V* characteristics in (a) log scale and (b) linear scale of the trench SBDs with an active area of 100×150 μm^2 (also see Fig. 1b for the definition of the device active area). Both DC and pulsed measurements are taken. Inset in (a): extracted ideality factor from DC measurements. The differential $R_{on,sp}$ is shown in (b). A base voltage of 0 V, a pulse width of 1 μs and a duty cycle of 0.1% is used in the pulsed measurements.

Fig. 3. (a) Comparison of the forward *I-V* characteristics under the pulsed condition between trench SBDs and regular SBDs without and with mesa. Insets show the schematic cross-section of the devices. The same pulsed condition as in Fig. 2 is used. (b) Extracted differential $R_{on,sp}$ of the trench SBDs under the pulsed condition *vs.* the fin width (W_{fin}). Dashed and solid line correspond to the calculated $R_{on,sp}$ with and without sidewall depletion, respectively.

corners [15] or the device edge [22], and the $R_{on,sp}$ is influenced by the fin area ratio (*A.R.*) [15]. To mitigate the field crowding at trench corners, a smaller fin width (W_{fin}) can be designed, since the peak electric field is found to decrease with reducing fin width [15]. The field crowding at trench corners is caused by the positive space charge inside the fin channels. By reducing the fin channel width, the total space charge inside the fin channels is decreased, leading to a reduction of the field crowding at trench corners. To address the field crowding at the device edge, adding a field plate (FP) at the device periphery is a viable technique.

In this work, we improved upon the previous devices by adopting both of these aforementioned approaches: a 1-μm fin width is designed with a high area ratio of 50%, together with the implementation of a field plate. With such improvements, a BV of 2.89 kV and a record-high Baliga's FOM of 0.8 (0.95) GW/cm^2 are achieved under DC (pulsed) condition.

II. DEVICE FABRICATION

The schematic device cross-section is shown in Fig. 1(a). The 10-μm epitaxial layer is grown by halide vapor phase epitaxy (HVPE) on a (001) n-type Ga_2O_3 substrate. The default fin width and pitch sizes are 1 μm and 2 μm, respectively, leading to a fin area ratio of 50%. The trench depth (d_{tr}) is reduced from 1.55 μm in our previous design [15] to 1.1 μm. The fin channels are designed along [010] direction, which is found to result in the highest forward current due to the lowest interface charge density on the (100)-like fin sidewalls [22]. The length of the field plate is designed to be 5 μm.

The fabrication process flow prior to the addition of the field plate is largely the same as reported previously [15]. After the formation of the fin channel by dry etching, the wafer was soaked in HF for 35 min under ultrasonication to remove the dry etch damage, during which the Ti/Pt (40/60 nm) etching mask was simultaneously removed. Then, Ti/Au (75/150 nm) cathode ohmic contact was formed, followed by the deposition of the 1st Al_2O_3 dielectric of 105 nm by atomic layer deposition (ALD). After opening of the Al_2O_3 on top of the fin channel by dry etching, Ni (30 nm) Schottky contact and then Ti/Pt (40/40 nm) sidewall coverage were deposited by electron-beam
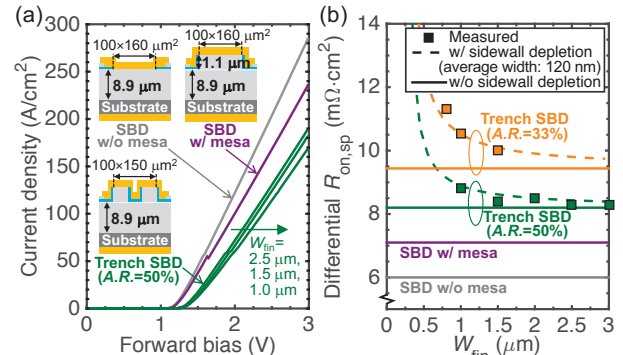
evaporation and sputtering, respectively. To form the field plate, a 2nd ALD Al_2O_3 dielectric layer of 125 nm was deposited. Then, contact holes were formed by dry etching to expose the anode metal. Lastly, the Ti/Al/Cu/Au (10/70/10/60 nm) field-plate metal stack was deposited. Figure 1(b) shows the top-view optical image of a fabricated device with an active region area of 100×150 μm^2, which includes both the fins and the regions between fins and is used to calculate the current density and $R_{on,sp}$. Figure 1(c) shows the cross-section of a fin channel imaged by scanning electron microscopy (SEM). A slanted facet is observed at the upper half of the right sidewall. This is likely a result of metal-assisted chemical etching by HF before the complete removal of the Ti/Pt dry-etch mask [23].

III. RESULTS AND DISCUSSION

Capacitance-voltage measurements were performed on the co-fabricated regular SBDs. As shown in Fig. 1(d), the net doping concentration N_D-N_A is extracted to be 1.25×10^{16} cm^{-3}.

Figure 2 shows the forward *I-V* characteristics from both DC and pulsed measurements of the trench SBDs with an active area of 100×150 μm^2. An apparent Schottky barrier height of 1.38 eV and an ideality factor of ~1.3 is extracted from the thermionic emission model. The pulsed measurements show a higher current density than DC measurements, especially at higher forward bias. This is likely due to the reduction of self-heating and sidewall trapping effect under pulsed conditions [14][24]. The differential $R_{on,sp}$ is extracted to be 10.5 mΩ·cm^2 from DC and 8.8 mΩ·cm^2 from pulsed measurements.

Figure 3(a) shows the comparison of the forward *I-V* characteristics under pulsed condition among three types of devices: regular SBDs with and without mesa, and trench SBDs. Similar with our previous observations [15], the current density is highest in SBDs without mesa and lowest in trench SBDs as a result of the extra conduction path in the 1.1-μm upper drift region as well as the restriction of the current path due to the fin channels. In addition, we observed that the current density is slightly lower in trench SBDs with smaller W_{fin}, even with the same fin area ratio. We ascribe it to sidewall depletion in the fin channels due to negative interface charges [22]. Considering an average sidewall depletion width of W_d, the $R_{on,sp}$ of trench SBDs ($R_{on,sp,trench}$) can be generically modeled by

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LED.2019.2953559, IEEE Electron Device Letters

First Author *et al.*: Title   1

$$R_{\mathrm{on,sp,trench}} = R_1 + \frac{R_2}{\left(1 - \dfrac{2W_d}{W_{\mathrm{fin}}}\right) \cdot A.R.},$$

where R_1 is the $R_{\mathrm{on,sp}}$ of all the components *below* the fin channels, including the drift layer (8.9-μm thick, also see Fig. 1a), the substrate and the back contact, while R_2 is the $R_{\mathrm{on,sp}}$ of the fin channel (1.1-μm tall in the trench SBDs). Since the device active area is nearly the same in the three types of devices shown in Fig. 3(a), the current spreading effect below the 1.1-μm upper drift region should be similar. Thus, R_1 can be approximated with $R_{\mathrm{on,sp}}$ of the SBD without mesa. If $A.R.$ is taken to be 100%, the trench SBD will become the SBD with mesa, thus R_2 can be obtained by the difference in $R_{\mathrm{on,sp}}$ between the SBDs with and without mesa.

Figure 3(b) shows the measured $R_{\mathrm{on,sp}}$ of the trench SBDs with 2 different $A.R.$ and a few W_{fin} values, all fabricated on the same wafer. If there is no depletion or accumulation in the fin channel, $W_d=0$ thus $R_{\mathrm{on,sp,trench}}$ should be independent of the fin width W_{fin}. The increase of $R_{\mathrm{on,sp}}$ with decreasing W_{fin} suggests that sidewall depletion does exist and impact the $R_{\mathrm{on,sp}}$ negatively. With the analytical model above, an average depletion width W_d of 120±30 nm is extracted. Detailed study of the interface charge responsible for the sidewall depletion is beyond the scope of this letter and will be presented in our future papers. In these devices, the interface-state density (D_{it}) on the fin sidewall is estimated to be $\sim 8\text{-}9 \times 10^{11}$ $\mathrm{cm^{-2} eV^{-1}}$, and the total interface-charge density as a function of the stress voltage behaves similarly with our previous devices [14]. Without the sidewall depletion, the $R_{\mathrm{on,sp,trench}}$ is expected to be 8.2 $\mathrm{m\Omega \cdot cm^2}$ for an $A.R.$ of 50% based on the model. If accumulation condition at the MIS-interface can be reached, the $R_{\mathrm{on,sp,trench}}$ can be even lower, comparable to that of regular SBDs.

Figure 4(a) shows the reverse *I-V* characteristics of the trench SBDs. In comparison with the regular SBDs with mesa and FP, the field-plated trench SBDs have much lower leakage current as well as a much higher BV of 2.89 kV. The breakdown of the trench SBDs is destructive, with visible breakdown craters near the device edge. To investigate the breakdown mechanism of
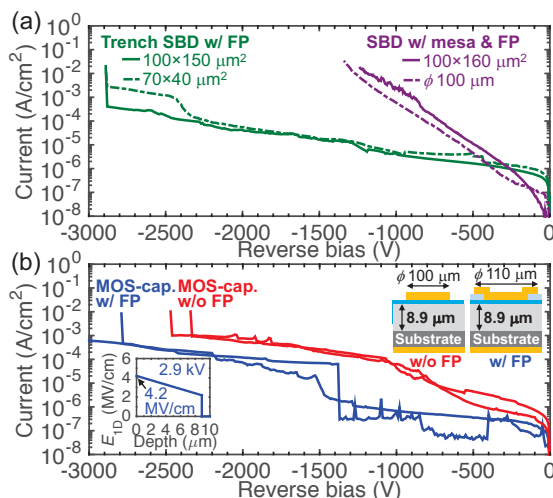

Fig. 5. Benchmark plot of state-of-the-art β-Ga₂O₃ SBDs, including lateral [5][25], vertical [10-12,17,18,26,27] and trench SBDs [21,14-16].

the trench SBDs, breakdown tests were also performed on MOS-capacitors without and with field plate, which are co-fabricated on the same wafer and have the same dielectric thickness and field-plate structure as the trench SBDs. As shown in Fig. 4(b), with addition of the field plate, the destructive BV of MOS-capacitors increases from ~2.4 kV to ~2.9 kV. The observed trend in BV also suggests that the breakdown is at the device edge, evidenced by the breakdown craters observed near the edge of the MOS-capacitors. The increase in BV with the addition of the field plate confirms its effectiveness in alleviating the edge field crowding, as also shown in our previously reported Ga₂O₃ transistors [9] and SBDs [16]. Since the BV of trench-SBDs is very close to that of field-plated MOS-capacitors, the breakdown of the trench SBDs is most-likely limited by the edge field crowding, which is found to be quite prominent despite the presence of the field plate [16]. In field-plated MOS-capacitors, the parallel-plane one-dimensional electric field (E_{1D}) at the Ga₂O₃ surface is calculated to be 4.2 MV/cm at 2.9 kV (see inset in Fig. 4(b)), which is higher than the E_c of SiC and GaN, but still much lower than the E_c of Ga₂O₃. With a more ideal edge termination structure, a higher E_{1D} can be reached.

Figure 5 shows the benchmark plot of reported β-Ga₂O₃ lateral SBDs [5][25], vertical SBDs [10-12,17,18,26,27] and trench SBDs [21,14-16]. The field-plated trench SBD in this work achieves a FOM ($\mathrm{BV^2}/R_{\mathrm{on,sp}}$) of 0.80 GW/cm² from DC measurements, which is the highest among all Ga₂O₃ power devices to date. From pulsed measurements, the FOM is even higher at 0.95 GW/cm² as a result of the slightly lower $R_{\mathrm{on,sp}}$ of 8.8 $\mathrm{m\Omega \cdot cm^2}$. As shown in Ref. 17, at a FOM higher than 0.6 GW/cm², the performance of Ga₂O₃ SBDs is already comparable with the state-of-the-art GaN SBDs. The gap between the present device performance and the material limit can be bridged with better electric field managements.

Fig. 4. Comparison of the reverse *I-V* characteristics between (a) field-plated trench SBDs and SBDs with mesa, (b) MOS-capacitors with and without field plate. Insets in (b) shows the schematic structures of the MOS-capacitors and the calculated one-dimensional electric field profile along the vertical direction at 2.9 kV in the MOS-capacitors.
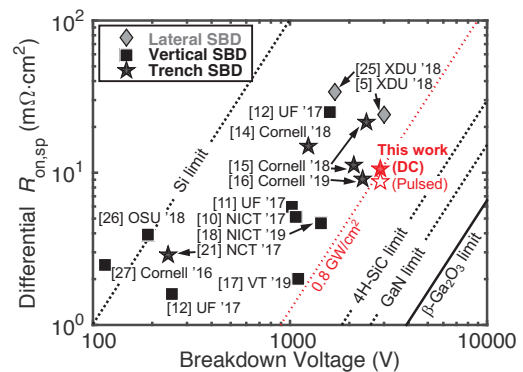
IV. CONCLUSION

We demonstrated field-plated Ga₂O₃ vertical trench Schottky barrier diodes. The addition of field plate is found to increase the breakdown voltage by ~500 V. We observed the existence of sidewall depletion with an extracted average width of 120±30 nm. The field-plated trench SBDs have a $R_{\mathrm{on,sp}}$ of 10.5 (8.8) $\mathrm{m\Omega \cdot cm^2}$ from DC (pulsed) measurements and a breakdown voltage of 2.89 kV, corresponding to a record-high Baliga's figure-of-merit of 0.80 (0.95) GW/cm².

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LED.2019.2953559, IEEE Electron Device Letters

First Author *et al.*: Title   1

REFERENCES

[1] M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Gallium oxide (Ga2O3) metal-semiconductor field-effect transistors on single-crystal β-Ga2O3 (010) substrates", *Appl. Phys. Lett.*, vol. 100, no. 1, p. 013504, 2012. doi: 10.1063/1.3674287.

[2] K. Ghosh, and U. Singisetti, "Impact ionization in β-Ga2O3", *J. Appl. Phys.*, vol. 124, no. 8, p.085707, 2018. doi: 10.1063/1.5034120.

[3] A. Kuramata, K. Koshi, S. Watanabe, Y. Yamaoka, T. Masui, and S. Yamakoshi, "High-quality β-Ga2O3 single crystals grown by edge-defined film-fed growth", *Jpn. J. Appl. Phys.*, vol. 55, no. 12, p.1202A2, 2016. doi: 10.7567/JJAP.55.1202A2.

[4] M. Higashiwaki, and G. H. Jessen, "Guest Editorial: The dawn of gallium oxide microelectronics", *Appl. Phys. Lett.*, vol. 112, no. 6, p. 060401, 2018. doi: 10.1063/1.5017845.

[5] Z. Hu, H. Zhou, Q. Feng, J. Zhang, C. Zhang, K. Dang, Y. Cai, Z. Feng, Y. Gao, X. Kang, and Y. Hao, "Field-Plated Lateral β-Ga2O3 Schottky Barrier Diode With High Reverse Blocking Voltage of More Than 3 kV and High DC Power Figure-of-Merit of 500 MW/cm2", *IEEE Electron Device Lett.*, vol. 39, no. 10, pp.1564-1567, 2018. doi: 10.1109/LED.2018.2868444.

[6] K. Zeng, A. Vaidya, and U. Singisetti, "A field-plated Ga2O3 MOSFET with near 2-kV breakdown voltage and 520 mΩ·cm2 on-resistance", *Appl. Phys. Express*, vol. 12, no. 8, p.081003, 2019. doi: 10.7567/1882-0786/ab2e86.

[7] J. K. Mun, K. Cho, W. Chang, H. W. Jung, and J. Do, "2.32 kV Breakdown Voltage Lateral β-Ga2O3 MOSFETs with Source-Connected Field Plate", *ECS J. Solid State Sci. Technol.*, vol. 8, no. 7, pp.Q3079-Q3082, 2019. doi: 10.1149/2.0151907jss.

[8] Z. Hu, K. Nomoto, W. Li, N. Tanen, K. Sasaki, A. Kuramata, T. Nakamura, D. Jena, and H. G. Xing, "Enhancement-mode Ga 2 O 3 vertical transistors with breakdown voltage >1 kV", *IEEE Electron Device Lett.*, vol. 39, no. 6, pp.869-872, 2018. doi: 10.1109/LED.2018.2830184.

[9] Z. Hu, K. Nomoto, W. Li, R. Jinno, T. Nakamura, D. Jena, and H. Xing, 2019, May. "1.6 kV Vertical Ga2O3 FinFETs With Source-Connected Field Plates and Normally-off Operation", in *Proc. Int. Symp. Power Semicond. Devices IC' s (ISPSD)*, May 2019, pp. 483-486. doi: 10.1109/ISPSD.2019.8757633.

[10] K. Konishi, K. Goto, H. Murakami, Y. Kumagai, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "1-kV vertical Ga2O3 field-plated Schottky barrier diodes", *Appl. Phys. Lett.*, vol. 110, no. 10, p.103506, 2017. doi: 10.1063/1.4977857.

[11] J. Yang, S. Ahn, F. Ren, S. J. Pearton, S. Jang, J. Kim, and A. Kuramata, "High reverse breakdown voltage Schottky rectifiers without edge termination on Ga2O3", *Appl. Phys. Lett.*, vol. 110, no. 19, p.192101, 2017. doi: 10.1063/1.4983203.

[12] J. Yang, S. Ahn, F. Ren, S. J. Pearton, S. Jang, and A. Kuramata, "High Breakdown Voltage (−201) β-Ga2O3 Schottky Rectifiers", IEEE Electron Device Lett., vol. 38, no. 7, pp. 906-909, 2017. doi: 10.1109/LED.2017.2703609.

[13] W. Li, K. Nomoto, Z. Hu, N. Tanen, K. Sasaki, A. Kuramata, D. Jena, and H. G. Xing, "1.5 kV Vertical Ga2O3 Trench-MIS Schottky Barrier Diodes", in *Proc. Device Res. Conf. (DRC)*, Jun. 2018, pp. 1-2. doi: 10.1109/DRC.2018.8442245.

[14] W. Li, Z. Hu, K. Nomoto, Z. Zhang, J. Y. Hsu, Q. T. Thieu, K. Sasaki, A. Kuramata, D. Jena, and H. G. Xing, "1230 V β-Ga2O3 trench Schottky barrier diodes with an ultra-low leakage current of <1 μ A/cm2", *Appl. Phys. Lett.*, vol. 113, no. 20, p.202101, 2018. doi: 10.1063/1.5052368.

[15] W. Li, Z. Hu, K. Nomoto, R. Jinno, Z. Zhang, T. Q. Tu, K. Sasaki, A. Kuramata, D. Jena, and H. G. Xing, "2.44 kV Ga2O3 vertical trench Schottky barrier diodes with very low reverse leakage current", in *2018 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2018, pp. 8-5. doi: 10.1109/IEDM.2018.8614693.

[16] W. Li, K. Nomoto, Z. Hu, D. Jena, D. and H. G. Xing, "Field-plated Ga2O3 Trench Schottky Barrier Diodes with a Record High Figure-of-merit of 0.78 GW/cm2", in *Proc. Device Res. Conf. (DRC)*, Jun. 2019, to be published.

[17] N. Allen, M. Xiao, X. Yan, K. Sasaki, M. J. Tadjer, J. Ma, R. Zhang, H. Wang, and Y. Zhang, 2019. "Vertical Ga2O3 Schottky Barrier Diodes with Small-Angle Beveled Field Plates: a Baliga's Figure-of-Merit of 0.6 GW/cm2", *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1399-1402, 2019. doi: 10.1109/LED.2019.2931697.

[18] C. H. Lin, Y. Yuda, M. H. Wong, M. Sato, N. Takekawa, K. Konishi, T. Watahiki, M. Yamamuka, H. Murakami, Y. Kumagai, and M. Higashiwaki, "Vertical Ga2O3 Schottky Barrier Diodes with Guard Ring Formed by Nitrogen-Ion Implantation", *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1487-1490, 2019. doi: 10.1109/LED.2019.2927790.

[19] B. J. Baliga, "Junction Barrier Controlled Schottky Rectifiers," in *Advanced Power Rectifier Concepts*, New York, NY, USA: Springer-Science, 2009, pp. 29-30.

[20] M. Mehrotra, and B. J. Baliga, "The trench MOS barrier Schottky (TMBS) rectifier", in *IEDM Tech. Dig.*, Dec. 1993, pp. 675-678. doi: 10.1109/IEDM.1993.347222.

[21] K. Sasaki, D. Wakimoto, Q. T. Thieu, Y. Koishikawa, A. Kuramata, M. Higashiwaki, and S. Yamakoshi, "First demonstration of Ga2O3 trench MOS-type Schottky barrier diodes", *IEEE Electron Device Lett.*, vol. 38, no. 6, pp.783-785, 2017. doi: 10.1109/LED.2017.2696986.

[22] W. Li, K. Nomoto, Z. Hu, D. Jena, and H. G. Xing, 2019. "Fin-channel orientation dependence of forward conduction in kV-class Ga2O3 trench Schottky barrier diodes", *Appl. Phys. Express*, vol. 12, no. 6, p.061007, 2019. doi: 10.7567/1882-0786/ab206c.

[23] H. C. Huang, M. Kim, X. Zhan, K. Chabak, J. D. Kim, A. Kvit, D. Liu, Z. Ma, J. M. Zuo, and X. Li, "High Aspect Ratio β-Ga2O3 Fin Arrays with Low Interface Charge Density by Inverse Metal-Assisted Chemical Etching", *ACS Nano*, vol. 13, no. 8, pp. 8784-8792, 2019. Doi: 10.1021/acsnano.9b01709.

[24] M. A. Bhuiyan, H. Zhou, R. Jiang, E. X. Zhang, D. M. Fleetwood, P. D. Ye, and T. P. Ma, "Charge Trapping in Al2O3/β-Ga2O3-Based MOS Capacitors", *IEEE Electron Device Lett.*, vol. 39, no. 7, pp.1022-1025, 2018. doi: 10.1109/LED.2018.2841899.

[25] Z. Hu, H. Zhou, K. Dang, Y. Cai, Z. Feng, Y. Gao, Q. Feng, J. Zhang, and Y. Hao, "Lateral β-Ga2O3 Schottky barrier diode on sapphire substrate with reverse blocking voltage of 1.7 kV", *IEEE J. Electron Devices Society*, vol. 6, pp.815-820, 2018. doi: 10.1109/JEDS.2018.2853615.

[26] C. Joishi, S. Rafique, Z. Xia, L. Han, S. Krishnamoorthy, Y. Zhang, S. Lodha, H. Zhao, and S. Rajan, "Low-pressure CVD-grown β-Ga2O3 bevel-field-plated Schottky barrier diodes", *Appl. Phys. Express*, vol. 11, no. 3, p.031101, 2018. doi: 10.7567/APEX.11.031101.

[27] B. Song, A. K. Verma, K. Nomoto, M. Zhu, D. Jena, and H. G. Xing, "Vertical Ga2O3 Schottky barrier diodes on single-crystal β-Ga2O3 (−201) substrates", in *Proc. Device Res. Conf. (DRC)*, Jun. 2016, pp. 1-2. doi: 10.1109/DRC.2016.7548440.