GaN HEMTs on Si with Regrown Contacts and Cutoff/Maximum Oscillation Frequencies of 250/204 GHz

Lei Li, Kazuki Nomoto, *Member, IEEE*, Ming Pan, *Member, IEEE*, Wenshen Li, Austin Hickman, Jeffrey Miller, Kevin Lee, Zongyang Hu, Samuel James Bader, Soo Min Lee, James C.M. Hwang, *Life Fellow, IEEE,* Debdeep Jena, *Senior Member, IEEE,* and Huili Grace Xing, *Senior Member, IEEE*

***Abstract*—This work demonstrates the high-frequency and high-power performance capacity of GaN high electron mobility transistors (HEMTs) on Si substrates. Using a T-gate and n^{++}-GaN source/drain contacts, the InAlN/GaN HEMT with a gate length of 55 nm and a source-drain spacing of 175 nm shows a maximum drain current $I_{D,MAX}$ of 2.8 A/mm and a peak transconductance g_m of 0.66 S/mm. The same HEMT exhibits a forward-current-gain cutoff frequency f_T of 250 GHz and a maximum frequency of oscillation f_{MAX} of 204 GHz. The $I_{D,MAX}$, peak g_m and f_T-f_{MAX} product are among the best reported for GaN HEMTs on Si, which are very close to the state-of-the-art depletion-mode GaN HEMTs on SiC without a back barrier. Given the low cost of Si and the high compatibility with CMOS circuits, GaN HEMTs on Si prove to be particularly attractive for cost-sensitive applications.**

***Index Terms*—HEMTs, millimeter wave transistors, T-gate, gallium nitride, silicon.**

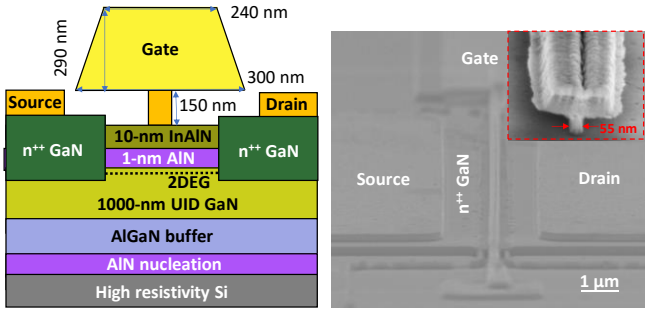
I. Introduction

GaN high electron mobility transistors (HEMTs) have high breakdown voltages, high two-dimensional electron gas (2DEG) densities, and a high electron saturation velocity. These properties make them ideal for high-power and high-frequency applications, such as switches in power systems and amplifiers in wireless communication systems. To date, the highest speed GaN HEMTs are demonstrated on SiC substrates, all of which employ regrown ohmic contacts to minimize source/drain resistances.

For double-heterostructure HEMTs on SiC, a forward current gain cutoff frequency f_T of 454 GHz and a maximum frequency of oscillation f_{MAX} of 444 GHz were realized in D-mode AlN/GaN/AlGaN HEMTs with a 20-nm T-gate and an ultra-scaled source-drain distance L_{SD} of 120 nm [1]. These devices show an average electron velocity as high as 2.8×10^7 cm/s, benefiting from enhanced velocity overshoot. Given the large electron-phonon interaction in GaN [2], it is necessary to scale the drain-gate distance below 70 nm in order to observe velocity overshoot, thus termed as ultra-scaled L_{SD} [3].

For HEMTs on SiC without a back barrier, the highest f_T of 400 GHz was reported with a f_{MAX} of 33 GHz at room temperature (f_T/f_{MAX} increased to 430/36 GHz at 77 K) in D-mode InAlN/GaN HEMTs employing a 30-nm I-gate and a L_{SD} of 270 nm [4]; the highest balanced f_T/f_{MAX} of 230/300 GHz in un-scaled HEMTs were reported employing a quaternary barrier InAlGaN with a 40-nm T-gate and a long L_{SD} of 800 nm [5], showing an average electron velocity of 1.36×10^7 cm/s; the highest balanced f_T/f_{MAX} of 302/301 GHz were realized in D-mode InAlN/GaN HEMTs with a 27-nm T-gate and an ultra-scaled L_{SD} of 140 nm [6].

Although GaN HEMTs on SiC have shown excellent performance, their large-scale applications are limited by the high cost and small size (typically 100-mm or 4-inch in diameter) of SiC. In comparison, GaN HEMTs on Si can reduce the cost with a moderate penalty on performance. For example, GaN HEMTs on up to 12-inch (300-mm) Si substrates promise much lower cost than GaN on SiC, yet much better performance



(a) (b)

Fig. 1. (a) Schematic HEMT cross section, no back barrier is employed. (b) SEM image of a completed GaN HEMT on Si. Inset shows details of the T gate.

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L. Li, K. Nomoto, A. Hickman, K. Lee, J. Miller, Z. Hu, and W. Li are with the School of Electrical and Computer Engineering, Cornell University, Ithaca, NY 14853 USA (e-mail: ll886@cornell.edu).

M. Pan and S. M. Lee are with Veeco Instruments Inc., Somerset, NJ 08873 USA (e-mail: mpan@veeco.com).

S. J. Bader is with the School of Applied and Engineering Physics, Cornell University, Ithaca, NY 14853 USA.

J. C. M. Hwang is with the Department of Materials Science and Engineering, Cornell University, Ithaca, NY 14853 USA.

D. Jena and H. G. Xing are with the School of Electrical and Computer Engineering, Department of Materials Science and Engineering, and Kavli Institute for Nanoscience, Cornell University, Ithaca, NY 14853 USA.

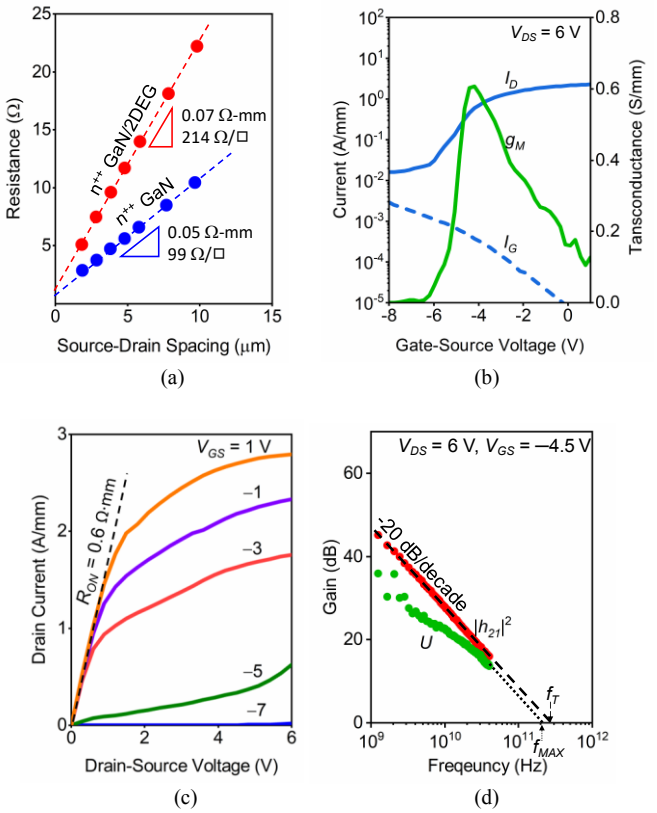

Fig. 2. (a) TLM measurement results. (b) Transfer characteristics, (c) output characteristics, and (d) cutoff frequencies measured on the same GaN HEMT on Si with a 55-nm T-gate and L_{SD} of 175 nm (HEMT A in Table I).

than laterally-diffused metal-oxide semiconductor (LDMOS) Si-FETs.

To this end, high-speed GaN HEMTs on Si have been pursued, nearly all of which use device structures without a back barrier. Marti et al. reported a balanced f_T /f_{MAX} of 141/232 GHz employing 50-nm T-gate [7]. Since both f_T and f_{MAX} are critical to high-frequency and high-power performance, the combined figure of merit $(f_T \cdot f_{MAX})^{1/2}$ = 181 GHz serves as a convenient gauge for the performance of GaN HEMTs on Si. Recently, there are reports of higher f_T for GaN HEMTs on Si [8]–[10]. However, their $(f_T \cdot f_{MAX})^{1/2}$ values are actually lower than 181 GHz because f_{MAX} is suppressed by high gate resistances.

In this work, by using a T-shaped gate and regrown n^{++}-GaN source and drain contacts, we reduced gate and source/drain resistances thus improving f_{MAX} to 204 GHz with a gate length of 55 nm, while keeping f_T at 250 GHz for GaN HEMTs on Si without a back barrier. This amounts to a record $(f_T \cdot f_{MAX})^{1/2}$ of 226 GHz among GaN HEMTs on Si, showing that the performance of GaN HEMTs on Si is approaching that of GaN HEMTs on SiC without a back barrier [5], where the HEMTs exhibit a $(f_T \cdot f_{MAX})^{1/2}$ of 262 GHz with a 40-nm T-gate and 227 GHz with a 60-nm T-gate. The biggest challenge in further reducing the gate length thus improving speed is the short-channel effect (SCE). The SCE can be best curbed in double heterostructures, where an effective back barrier is present to confine the electrons in the channel but not degrade the electron mobility. However, such GaN double-heterostructure epitaxy is yet to be developed on Si substrates.

TABLE I
GAN HEMTS ON SI OF DIFFERENT GEOMETRIES

HEMT	Gate Length L_G (nm)	S-D Spacing L_{SD} (nm)	Peak Trans-conductance g_M (S/mm)	Maximum Current I_{MAX} (A/mm)	Unity-Gain Frequency f_T (GHz)	Max Freq. Oscillat. f_{MAX} (GHz)
A	55	175	0.66	2.8	250	204
B	55	175	0.76	2.8	248	193
C	55	280	0.62	2.6	235	196
D	60	175	0.56	2.8	230	170
E	65	280	0.50	2.0	200	176
F	60	1000	0.71	1.73	150	155

L_G refers to the length of the T gate stem.

II. EXPERIMENTS

Figure 1(a) shows that the present GaN HEMTs on a high-resistivity Si substrate have no back barrier, comprising an AlN nucleation layer, an AlGaN buffer, a 1-μm unintentionally doped GaN channel, a 1-nm AlN spacer, and a 10-nm $In_{0.17}Al_{0.83}N$ barrier. The layers are grown by metal-organic chemical vapor deposition (MOCVD) on 200-mm-diameter 725-μm -thick high-resistivity (3000 Ω·cm) Si substrates in a Propel® HVM system at Veeco Instruments. Despite the large substrate, the grown layers are very uniform with a surface roughness of 0.72 nm and a standard deviation of 1.5% in the sheet resistance R_{SH}. The surface roughness is mapped by a Bruker Icon atomic force microscope over a randomly chosen 5 μm × 5 μm area. R_{SH} is mapped by a Lehighton contactless system across the entire 200-mm diameter substrate. The average R_{SH} of 206.4 Ω/□ is consistent with the Hall measurement, which shows that the 2DEG has a density of 2.27 × 10^{13} cm^{-2} and a mobility of 1430 $cm^2/V \cdot s$.

Device fabrication follows a previously established process flow [11]. First, to facilitate low-resistance ohmic contacts, the source and drain contact regions of the HEMTs are patterned by photolithography and plasma etching using a Cr/SiO_2 hard mask. Second, the etched regions are backfilled with 80-nm-thick Si-doped n^{++} GaN using molecular beam epitaxy (MBE) at 750 °C. Limited by the MBE reactor size, the 200-mm Si wafer is diced into 3.7 × 3.7 cm^2 chips. The Si doping density is on the order of 10^{20} cm^{-3}, consistent with the $R_{SH,n++GaN}$ of 99 Ω/□ as measured by the transfer length method (TLM). Defining the n^{++}-GaN regions through the Cr/SiO_2 hard mask, the source-drain spacing L_{SD} is purposely varied by electron-beam lithography (EBL) between 175 nm and 1 μm . Then, 40-nm-thick Ti and 200-nm-thick Au are sequentially deposited on n^{++} GaN to form ohmic contacts without annealing. The Ti/Au contacts are pulled back by 1 μm from the n^{++}-GaN edge as shown in Fig. 1(b). A contact resistance R_C of 0.05 Ω·mm is measured between the metal and the n++GaN (Fig. 2).

Last, T gates are defined by EBL with evaporation and liftoff of 50-nm-thick Ni and 240-nm-thick Au. As shown in Fig. 1(b), the trapezoid hat of the T gate has a height of 290 nm, a length of 300 nm on the bottom and 240 nm on the top, whereas the stem of the T gate has a height of 150 nm; the gate length L_G has been varied to be 55, 60 or 65 nm. With two parallel gate fingers, the total gate width is 2 × 25 μm.

The fabricated HEMTs were characterized on a Cascade Technologies Summit 9000 probe station with Infinity GSG microwave wafer probes. DC characterization is performed by using a Keithley 4200 semiconductor characterization system;

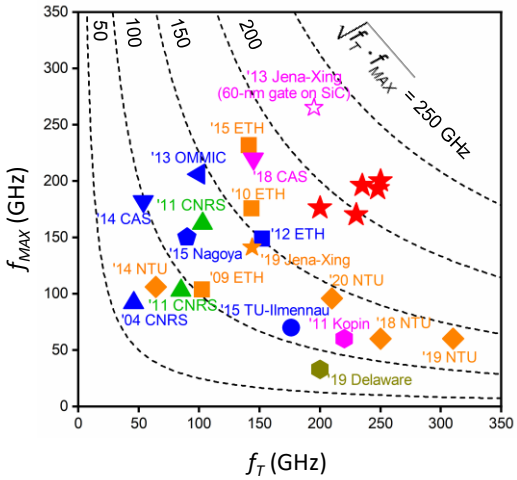

Fig. 3. Comparison of f_T and f_{MAX} of GaN HEMTs on Si from [7]–[10], [17]–[31], and this work (★). Hollow star (☆) is a GaN HEMT on SiC [5] with similar structures as this work. Different colors represent different top barriers: orange for InAlN, blue for AlGaN, green for AlN, magenta for InAlGaN, Olive green for InAlN/InGaN (top/back).

RF characterization is performed by using an Agilent Technologies 8722ES network analyzer. For RF characterization, scattering parameters are measured from 50 MHz to 40 GHz. The measurements are calibrated using short, open, load, and through impedance standards on an alumina substrate. The parasitics are de-embedded using open and short test structures on the same chip as the HEMTs [12]. After de-embedding, f_T is extrapolated from the current gain $|h_{21}|^2$, whereas f_{MAX} is extrapolated from the unilateral gain U. In both cases, the gain is assumed to follow -20 dB/dec.

III. Results and Discussion

TLM test structures, 100-μm wide and fabricated on the same chip as the HEMTs, reveal excellent ohmic contact to the 2DEG. Figure 2(a) shows an extracted R_C of 0.07 Ω·mm between the ohmic metal and the 2DEG and a 2DEG channel R_{SH} of 214 Ω/□. Furthermore, the 2DEG R_{SH} on processed chips is very close to that measured before device fabrication. These R_C and R_{SH} values are significantly lower than the state of the art GaN HEMTs on Si [7], [8], which contribute to the high speed observed in these InAlN/GaN on Si HEMTs. The low R_C is ascribed to the regrown n^{++}-GaN contacts and the high 2DEG concentration [13], whereas the low R_{SH} is mainly attributed to the minimal degradation in the 2DEG density and mobility thanks to the regrown contact process [14], [15].

Figures 2 show the transfer and output characteristics, and cutoff frequencies measured on HEMT A in Table I with L_G = 55 nm and L_{SD} = 175 nm. The observed maximum drain current $I_{D,MAX}$ of 2.8 A/mm and the on resistance R_{ON} of 0.6 Ω·mm, along with the peak transconductance g_m of 0.66 S/mm, are among the best in GaN HEMTs on Si, comparable to GaN HEMTs on SiC without a back barrier. HEMT A shows a high output conductance, suggesting it suffers from severe SCE. This is confirmed in Fig. 2(b), where I_D under off-state is higher than the gate leakage, i.e. a residue current flowing between source and drain that can't be turned off by the gate voltage. At low V_{DS}, these HEMTs typically exhibit a decent I_{ON}/I_{OFF} ratio ~10^5; HEMT A has the highest gate leakage among all the tested

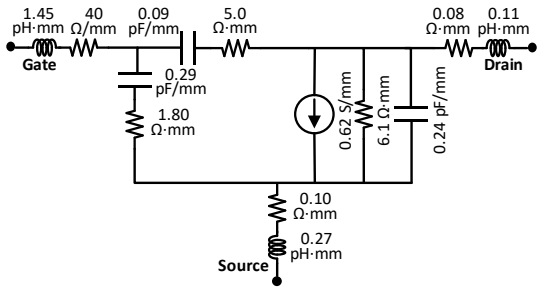

Fig. 4. Small-signal equivalent-circuit model of HEMT A under V_{GS} = −4.5 V and V_{DS} = 6 V.

devices, most likely due to processing non-uniformity. The gate leakage can be further reduced by adopting a plasma treatment [4], [9, [16]. Also adversely influenced by the SCE, i.e. high drain leakage, the device breakdown voltage is ~12 V. In HEMTs without a back barrier, the SCE sensitively depends on the quality of the gate definition and GaN buffer. A more straightforward design is to implement a back barrier such as InGaN, AlGaN, InAlN or AlN back barrier technologies.

The f_T /f_{MAX} of 250/204 GHz are obtained after de-embedding in HEMT A; in comparison, neglecting the short de-embedding test structure renders similar f_T/f_{MAX} values of 245/187 GHz. Table I lists f_T and f_{MAX} measured on HEMTs of different geometries on the same chip. In general, HEMTs with longer L_G and L_{SD} have lower f_T and f_{MAX}. In Fig. 3, the f_T and f_{MAX} values achieved in this work are compared to other reported GaN HEMTs on Si, as well as the state-of-the-art GaN HEMTs on SiC with similar epi-structures and device dimensions [5] (gate length, barrier materials, and its thickness, no back barrier). It can be seen the present HEMTs are clustered near the upper right corner as desired, with $(f_T \cdot f_{MAX})^{1/2}$ very close to that of the GaN HEMTs on SiC with a comparable gate length.

To help explain the high f_{MAX}, Fig. 4 shows the small-signal equivalent-circuit model of HEMT A with the model parameters extracted by a standard procedure [32]. The extracted AC g_m is similar to its DC value, indicating little dispersion, also confirmed by the pulsed I-V measurement (not shown), which is consistent with our prior learnings on InAlN HEMTs with the non-alloyed regrown contact process [14]. The maximum errors between the simulated and measured S_{11}, S_{12}, S_{21}, and S_{22} are 1%, 90% (S_{12} is a very small number thus a higher error margin), 2%, and 5%, respectively. Using the small-signal model, the simulated f_T and f_{MAX} are 248 GHz and 197 GHz, respectively, which are very close to the measured values. Had n^{++} GaN not been used, assuming R_S=R_D=0.5 Ω·mm, f_T/f_{MAX} would have reduced to 202/171 GHz. Similarly, any increase in R_G would reduce f_{MAX}. Thus, the small-signal analysis confirms the benefits of n^{++} GaN and T gate, especially in increasing f_{MAX}.

IV. Conclusion

GaN HEMTs on Si with different geometries were fabricated, measured, and analyzed. The analysis confirms the benefits of n^{++}-GaN source/drain contacts and T-shaped gates, especially in achieving both high f_{MAX} and f_T. With the state-of-the-art regrown ohmics, scaled source-drain separation and T-gates, GaN HEMTs on Si achieve comparable metrics with that on SiC in terms of DC and small-signal performance.

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