

# Degradation mechanisms of GaN-based vertical devices: a review

M. Meneghini<sup>1</sup>, E. Fabris<sup>1</sup>, M. Ruzzarin<sup>1</sup>, C. De Santi<sup>1</sup>, K. Nomoto<sup>2</sup>, Z. Hu<sup>2</sup>, W. Li<sup>2</sup>, X. Gao<sup>3</sup>, D. Jena<sup>2</sup>, H. G. Xing<sup>2</sup>, M. Sun<sup>3</sup>, T. Palacios<sup>3</sup>, G. Meneghesso<sup>1</sup>, E. Zanoni<sup>1</sup>

<sup>1</sup>Department of Information Engineering, University of Padua, 35131 Padua, Italy (e-mail: [matteo.meneghini@dei.unipd.it](mailto:matteo.meneghini@dei.unipd.it))

<sup>2</sup>Cornell University, Ithaca, NY, USA

<sup>3</sup>IQE RF LLC, Somerset, New Jersey 08873, USA

<sup>4</sup>Massachusetts Institute of Technology, Cambridge, MA, USA

**Keywords:** GaN, vertical, degradation, reliability, defects

**Abstract:** This paper reviews our most recent results on the reliability of vertical GaN-based devices, by presenting a few case studies focused on the stability and degradation of high-voltage GaN-on-GaN diodes and of GaN-based FETs. With regard to diodes, two relevant stress conditions are investigated: the first is operation at high forward current, that can induce a degradation of the electrical properties of the devices, mostly consisting in an increase in the operating voltage, well correlated to a decrease in the electroluminescence signal emitted by the diodes. This degradation process is ascribed to the diffusion of hydrogen from the highly p-type doped regions towards the junction, with consequent compensation of the acceptor (Mg) dopant. The second stress regime investigated on diodes is avalanche: specifically, it is shown that polarization-doped GaN devices may show avalanche capability, and the stability of diodes in avalanche regime is investigated in detail. With regard to transistors, the analysis is focused on GaN-on-GaN vertical Fin-FETs. First, the stability of the threshold voltage under positive gate stress is analyzed, and the role of interface/oxide traps is discussed by experimental characterization. Then, the degradation under positive gate or high-drain stress is investigated, to provide information on the dominant degradation processes.

This article has been accepted for publication and undergone full peer review but has not been through the copyediting, typesetting, pagination and proofreading process, which may lead to differences between this version and the [Version of Record](#). Please cite this article as [doi: 10.1002/pssa.201900750](https://doi.org/10.1002/pssa.201900750).

## 1. Introduction

Over the last decade, the research in the field of GaN-based power devices has shown impressive advancements. Thanks to the heteroepitaxial growth on silicon substrates, GaN-based high-electron mobility transistors (HEMTs) can reach a high performance, while having a relatively low cost. Currently, industrial efforts are mainly focused towards GaN lateral FETs, since they can be easily fabricated by using a CMOS compatible process. In addition, the use of an AlGaN/GaN heterostructure – in presence of large polarization fields – allows to maximize channel conductivity and electron density. GaN lateral devices are now commercially available, and target voltages up to 900 V <sup>[1]</sup>, thus competing with Si- and SiC-based components for consumer and industrial electronics, and for the automotive field. The high breakdown field (11 times higher than silicon) and the wide energy gap (3.4 eV) allow high voltage and high temperature operation, thus ensuring a high reliability to this technology.

Despite the great potential of GaN lateral devices, they have some limitations, that may slow their applicability in the >1 kV range. First, the breakdown voltage of a lateral transistor scales with the gate-drain spacing, i.e. with device area. Reaching high breakdown voltages is technically feasible, but results in an increase in device area and cost. Increasing device size can also impact on parasitic resistance. A second factor that needs to be considered is that lateral devices are very sensitive to surface effects. The 2-dimensional electron gas (2DEG) is very close to the surface, and trapping processes at the AlGaN/passivation interface may significantly impact on the dynamic performance of the devices <sup>[2]</sup>. In addition, in most cases the electric field in lateral devices is not uniform, across the gate drain spacing, and has peaks at the edge of the gate and of each field plate. Field can be minimized through the use of field plates; however, the addition of field plates may impact on device capacitance, and an accurate design must be carried out in order to ensure simultaneously low-field and high device performance <sup>[3][4]</sup>. Finally, lateral GaN HEMTs are typically based on an AlGaN/GaN heterostructure, which is intrinsically normally-on. To reach normally-off operation, a p-type gate can be used <sup>[5]</sup>, and threshold voltages above 1 V can be obtained <sup>[6]</sup>. If higher threshold voltages are required (e.g. 3-5 V, see <sup>[7]</sup> and references therein), different approaches can be considered, such as the use of a MIS/MOS structure or the adoption of a cascoded configuration.

Several Si- and SiC power transistors are based on a vertical configuration: the flow of current is controlled by a gate placed on the top of the transistor, and electrons flow through a thick drift-region, over which most the potential drops in off-state. The vertical approach allows to increase the breakdown strength of the transistors, without impacting on device area, provided that

sufficiently thick drift regions are fabricated. Also, vertical devices are almost insensitive to surface trapping effects, since current flow takes place in the bulk semiconductor. As was the case for Si and SiC, also GaN is now ready for the transition to vertical configuration. GaN vertical diodes and transistors have already been demonstrated, grown on free-standing GaN substrates with dislocation densities

up to  $10^6 \text{ cm}^{-2}$

[7][8][9][10][11][12][13][14][15][16][17][18][19][20][21][22][23][24][25][26][27][28][29][30][31][32][33][34][35][36][37][38][39][40][41][42][43][44][45][46][47][48][49][50][51][52][53][54][55][56][57][58][59][60].

In several cases, the breakdown voltage of these devices is higher than 1 kV, thus clearing the way to the application in the power semiconductor field. Recent reports also demonstrated the possibility of growing GaN vertical devices on foreign substrates (see for instance [60][61][62][63][64][41][52][65][66]). Both the quasi-vertical and the fully-vertical approaches have been implemented, in order to ensure an effective extraction of current from the drain. The research on vertical GaN-on-Si is mainly driven by the need of reducing the cost of GaN vertical devices: a recent paper [63] evaluated the cost of wafer and epitaxy for different vertical GaN technologies, and indicated that vertical GaN-on-Si devices can allow a 10 to 100 times cost reduction. Another advantage of vertical GaN-on-Si is that it is compatible with 8-inch production lines, thus being suitable for effective industrial production. Obviously, the development of vertical GaN-on-Si technology is slowed by the higher dislocation density and by the difficulty of growing thick drift regions on a silicon substrate: these aspects are currently under investigation, and quasi-vertical vertical and fully-vertical GaN power diodes on foreign substrate (Si) with breakdown voltages near 1 kV have already been demonstrated [35][67].

With regard to GaN vertical diodes, both Schottky-barrier diodes and pn diodes have been investigated and fabricated. In both cases, improvements in breakdown voltage were obtained through the optimization of the growth conditions (see for instance [10]), a careful design of the drift region [41], or the use of guard rings [39]. With regard to vertical transistors, several approaches have been proposed: (i) the Current Aperture Vertical Electron Transistor (CAVET) uses a combination of 2DEG channel and vertical drift region. Current blocking layers are used to create a barrier for electrons, that can only flow through a current aperture at the center of the device [43]. Another approach is the vertical trench MOSFET (see [39][60] for recent examples), where a MOS structure is used in combination with a trench in order to control the flow of current through the device. A third approach is the vertical power FINFET [68]: here current flow is controlled through the use of nanometer size fins, typically composed only of n-type material. Finally, vertical 3D GaN nanowire MOSFETs and PolarMOS have also been proposed [68][69][70].

All the structures described above are of high interest for the development of GaN-based vertical devices. Each of them has intrinsic advantages and potential drawbacks, that represent interesting research challenges, rather than fundamental limits. Previous reports preliminarily investigated the stability of vertical GaN-based components (see for instance Ref. [71]), suggesting that these devices can have a good ruggedness, and a good potential for high voltage applications.

Over the last few years, we have analyzed several GaN vertical devices, both diodes and transistors [69][49][50][70][72][73][74][75][76], identifying and describing the most relevant degradation mechanisms and related processes. The aim of this article is to present a summary of our most recent results in this field, by describing a number of case studies carried out in our laboratories on GaN-based vertical devices.

More specifically, the first case study that we present here deals with the stability of pn diodes under high current stress, and is relevant for the development of reliable diodes. In fact, GaN-based vertical diodes are expected to be operated at high current and current density ( $>kA/cm^2$ ). Under such stressful conditions, the stability of the resistivity and turn-on voltage must be carefully evaluated. To this aim, we carried out a set of stress experiments at high current density on pn diodes, and investigated the electrical degradation of the devices during stress time. The results collected within this study suggest that during operation at high current densities, a diffusion process leads to an increase in the operating voltage and to a decrease in the electroluminescence signal emitted by the devices. The results are interpreted by considering the diffusion of hydrogen from the top p-doped layer towards the junction.

The second case study described below deals with the operation of GaN pn diodes in avalanche regime. We analyzed polarization-induced pn diodes, that are the basic units of PolarMOS. First, we show that polarization-doped pn diodes have avalanche capability; second, we investigate the stability of the avalanche voltage with stress time, and discuss the origin of the “breakdown-walkout” and its relation with traps within the drift region.

The third case study deals with GaN-based vertical FinFETs. On these devices, we investigated the threshold voltage instabilities induced by operation at positive gate stress, demonstrating the existence of two different trapping processes: the de-trapping of electrons from the gate insulator, that takes place at low stress voltages ( $<2$  V), and results in a negative threshold voltage shift, and the injection of electrons from the channel into the gate insulator, that occurs at higher stress bias (up to 5-6 V) and results in a positive threshold shift.

Finally, we analyzed the robustness of GaN-based vertical FETs under high electric field, suggesting that the quality of the gate oxide and the minimization of the field are necessary steps for the optimization of the reliability of the devices.

## 2. Degradation of GaN-on-GaN vertical diodes submitted to high current stress

The degradation of impurity-doped vertical GaN pn diodes stressed at high current density was investigated by means of electro-optical measurements<sup>[72]</sup>.

The structure of the analyzed devices consists of a Si-doped n-GaN layer (10  $\mu\text{m}$ ) with a doping  $N_D \sim 2 \times 10^{16} \text{ cm}^{-3}$ , a Mg-doped p-GaN layer (0.4  $\mu\text{m}$ ) with a doping higher than  $10^{19} \text{ cm}^{-3}$ , and a Mg-doped p<sup>+</sup> GaN layer (0.02  $\mu\text{m}$ ) with a doping higher than  $10^{20} \text{ cm}^{-3}$  grown by metal-organic chemical vapour deposition (MOCVD) on a GaN substrate<sup>[77][78][79]</sup>. The devices have a diameter of 110  $\mu\text{m}$  and were optimized for high voltage operation through the use of a field plate<sup>[78]</sup>.

To study the physical mechanism responsible for the degradation of the impurity-doped pn diodes under forward bias condition, a high current density of 0.7 kA  $\text{cm}^{-2}$  was applied for 36000 seconds and the electrical and optical parameters were monitored during the stress.

**Figure 1** shows the behaviour of the I-V and L-I characteristics at different stress times. We found that the stress at high current density resulted in an increase in turn-on voltage (and on-resistance) (Figure 1 (a)) and in a decrease in the electroluminescence (EL) signal (Figure 1 (b)). In particular, the changes in the I-V curves for increasing stress time were characterized by three main phenomena, as can be noticed in Figure 1 (a); the first phenomenon was the increase in the turn-on voltage and it was visible after 300 seconds of stress, the second one was the increase in the generation-recombination current in the low forward region and it was visible after 6300 seconds, and the third one was the increase in the leakage current in the reverse bias region and it was visible after 31500 seconds.

On the other hand, by analysing the EL vs current characteristics in Figure 1 (b), a gradual degradation in the optical performance of the device was visible up to 13500 seconds, and then, for longer stress times, a further degradation process took place. This latter could be related to the generation of non-radiative defects within the depletion region, as suggested by the fact that the slope of the log-log L-I curves increased from nearly 1 towards 1.7 for stress times longer than 13500 seconds<sup>[78][80]</sup>.

It is worth noting that the decrease in the optical power was linearly correlated with the increase in on-resistance for increasing stress times, as can be seen in Figure 2 (a), suggesting a common origin of the degradation of the electrical and optical performance. This common origin could be related to the presence of hydrogen in the device.

Hydrogen is introduced within the p-GaN layers during the growth and typically it has concentration similar to Mg<sup>[81]</sup>. The H-atoms tend to create Mg-H bonds, which may be broken by temperature and current flow, leaving H interstitial in the lattice that can diffuse from the highly-doped p-GaN layer towards the pn junction, following the concentration gradient. The H-atoms can therefore passivate Mg-atoms near the junction, resulting in a lower hole injection due to the acceptor compensation; a lower hole concentration can explain both the decrease in the EL signal and the increase in turn-on voltage.

The hypothesis that the physical mechanism responsible for the degradation of impurity-doped pn diodes was caused by a diffusion mechanism, possibly involving H-atoms, is supported by the dependence of the variation of both the optical power and the on-resistance on the square root of time (Figure 2 b). In fact, the square-root dependence on stress time of the electrical and optical parameters obeyed the Fick's second law in one dimension (**Equation 1**):

$$N_{\text{diff}}(x, t) = N_0 \text{erfc} \left( \frac{x}{2\sqrt{Dt}} \right) \quad (1)$$

where  $N_{\text{diff}}$  is the number of impurities that can be found at position  $x$  at time  $t$ ,  $N_0$  is the concentration of the impurities at the junction (that is assumed to be constant), erfc is the error function,  $x$  is the distance from the junction,  $D$  is the diffusion coefficient, and  $t$  is the stress time [82][83].

For longer stress times, the degradation mechanism causes a further increase in the slope of the log-log L-I curves. This increase could be explained by the generation of SRH-recombination centers [84].

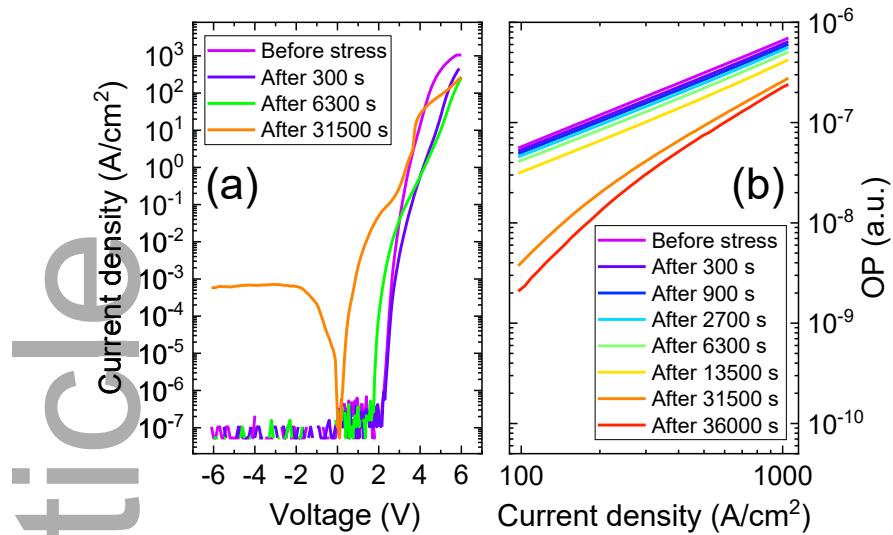


Figure 1. I-V (a) and L-I (b) curves measured before stress and after each step of the stress of an impurity doped pn diode at  $J_{\text{stress}}=0.7 \text{ kA cm}^{-2}$ . Experimental data from [72].

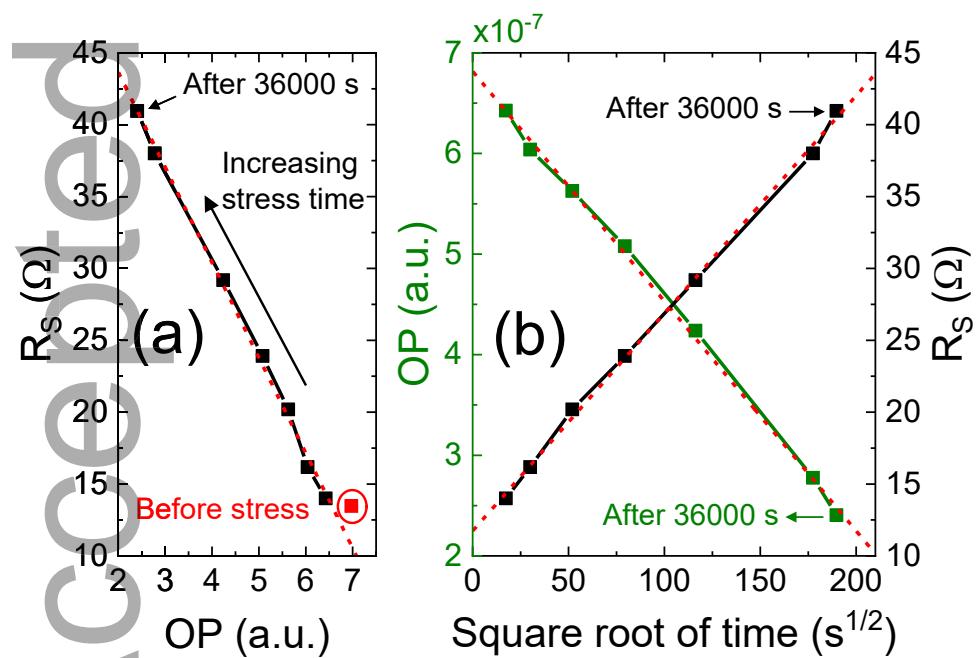


Figure 2. Relation between the increase in the series resistance and the decrease in the optical power during the stress (a). Relation between the variation of the optical power (green curve) and of the series resistance (black curve) and the square root of stress time (b). Experimental data from [72].

### 3. Demonstration of avalanche capability in polarization-doped vertical GaN pn diodes: study of walkout due to residual carbon concentration

Next, we investigated the avalanche capability and the stability of polarization-doped vertical GaN pn diodes in avalanche mode<sup>[49][50]</sup>. The devices are grown by MOCVD and have a GaN substrate, a Si-doped n<sup>-</sup> GaN layer (200 nm) with doping  $N_D \sim 10^{18} \text{ cm}^{-3}$ , a Si-doped n GaN layer (7  $\mu\text{m}$ ) with doping  $N_D \sim 2 \times 10^{16} \text{ cm}^{-3}$ , a n-type linearly graded AlGaN layer with the Al composition graded up from 0% to 5.6% (1  $\mu\text{m}$ ), a p-type linearly graded AlGaN layer with the opposite Al composition gradient (from 5.6% to 0%) (0.4  $\mu\text{m}$ ), and a Mg-doped p GaN layer (20 nm) with a doping higher than  $10^{20} \text{ cm}^{-3}$ <sup>[85]</sup>. A pn junction obtained by grading the Al composition results a) in an enhancement of p-type conductivity compared to the impurity-doped case, b) in a doping level that does not strongly depend on temperature or frequency, c) in the absence of carrier freeze-out, in contrast to what the impurity-doped carriers do when the temperature decreases, and d) in a higher breakdown field, thanks to the larger bandgap of AlGaN<sup>[70]</sup>. The breakdown voltage of the analyzed diodes is significantly improved through the use of a field plate<sup>[77][78][79]</sup>.

Two generations of these polarization-doped pn diodes were characterized and compared: the Gen1 diodes have a high carbon level throughout the device structure, on the order of  $2-3 \times 10^{16} \text{ cm}^{-3}$ ; and the Gen2 diodes have a carbon level below the detection limit of secondary ion mass spectrometry (SIMS)  $< 1 \times 10^{16} \text{ cm}^{-3}$ . It was found that both generations are avalanche capable, and the Gen1 diodes exhibit recoverable breakdown walkout while the Gen2 diodes do not. The summarized study on the Gen1 diodes is presented below while the study on the Gen2 diodes will be reported elsewhere. The avalanche capability of the Gen1 diodes was tested by means of I-V characterizations at different temperatures (inset **Figure 3**). As can be noticed the diodes have a low leakage current up to high breakdown voltage (-1370 V at 30°C), where a sudden increase in the current occurs. By analyzing the reverse voltage for a current density of -10 mA cm<sup>-2</sup>, a positive temperature coefficient with a slope of 0.5 V °C<sup>-1</sup> was found, indicating an avalanche process.

It was therefore necessary to understand if the breakdown voltage was stable, since the stability of pn diodes under avalanche regime is important for high reverse voltage operation. In order to investigate the behavior of the devices when a strong reverse bias was applied, a constant current stress in avalanche mode ( $J_{\text{stress}} = -10 \text{ mA cm}^{-2}$ ) was carried out. Figure 3 shows that the avalanche voltage increases with increasing stress time. This time-dependent shift of the reverse voltage to higher (negative) values is referred to as breakdown walkout<sup>[86][87][88]</sup>, and it was found to be fully recoverable in the analyzed devices after some rest time. Then, we analyzed the transients of the breakdown voltage during the recovery phase carried out after the constant current stress in avalanche mode at different temperatures; the Arrhenius plot reported in **Figure 4** (black symbols) was obtained. A ~~deep level possibly related to carbon on nitrogen sites C<sub>N</sub>~~ was found, as suggested

by comparing By comparing with previous reports the slope of the extracted Arrhenius plot and the region of the plot in which the deep level is located, a deep level possibly related to carbon on nitrogen sites  $C_N$  was found [89][90][91][92]. To confirm the presence of  $C_N$ , C-DLTS (Capacitance-Deep Level Optical Transient Spectroscopy) measurements were carried out at different temperatures. These measurements consist in two phases; in the first phase the defects in the space charge region are filled by applying a filling voltage, and in the second one the de-trapping process from the deep levels are studied by analyzing the capacitance variation at a certain measure voltage [93]. By repeating the measurements at different voltages, it is possible to investigate different active volumes of the device, and by repeating the measurements at different temperatures it is possible to extract an Arrhenius plot. The results of the temperature-dependent measurements are reported in Figure 4 (red symbols); a deep level possibly ascribed to  $C_N$  was found again.

The experimental data therefore suggest that the breakdown walkout process could be related to the presence of residual carbon in the polarization-doped pn diodes. A model able to explain these experimental results was proposed, by considering that, when a strong reverse bias is applied,  $C_N$  behaves as a deep acceptor and is ionized. This leads to an increase in the Coulomb and phonon scattering in the lattice (due to the higher number of ionized impurities), and consequently to a decrease in the mean free path of carriers. To trigger impact ionization, the electrons need to gain enough energy to create an additional electron-hole pair, and the density of electron that have sufficient energy depends on the mean free path, as can be seen in **Equation 1**:

$$n^* = n \cdot \exp\left(-\frac{d}{\lambda}\right) \quad (1)$$

where  $n^*$  is the density of electrons that have the energy required to start the avalanche process,  $n$  is the total electron density,  $d$  is the distance necessary to gain sufficient energy for the impact ionization, and  $\lambda$  is the mean free path. Therefore, a decrease in the mean free path corresponds to a decrease in the density of electrons that have sufficient energy to create additional electron-hole pairs. Therefore, once more and more  $C_N$  is ionized, it will be necessary a higher negative voltage to start the avalanche multiplication.

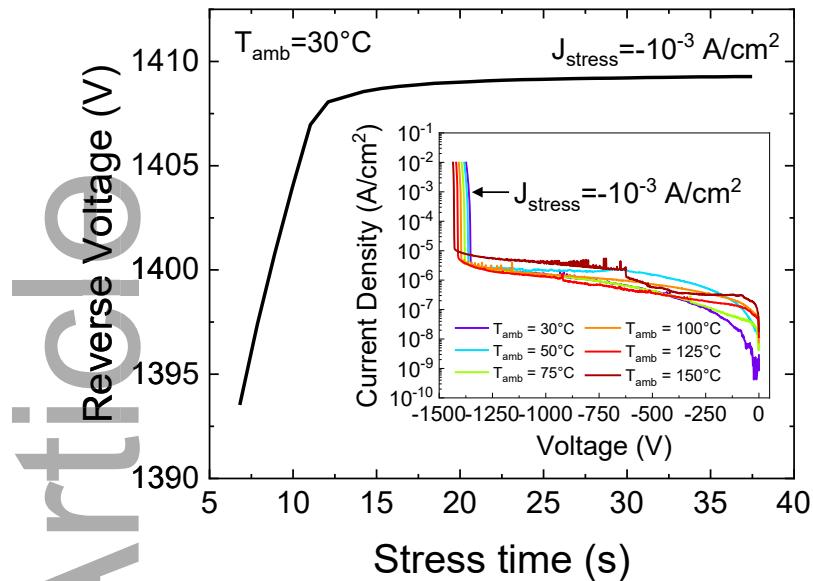


Figure 3. Time-dependence of breakdown walkout. The breakdown voltage increases during the stress time in avalanche mode. Inset: I-V curves at different temperatures of the diode under reverse bias condition. Experimental data from <sup>[49][50]</sup>.

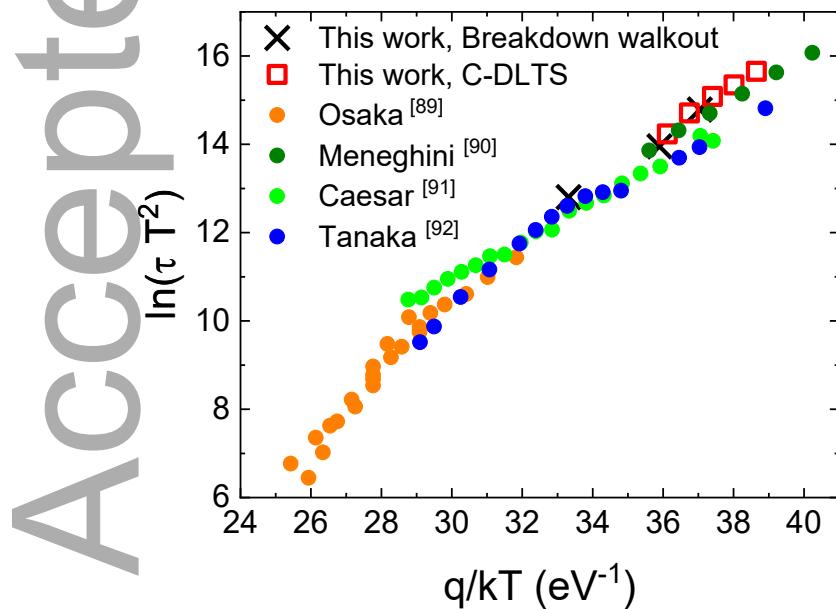


Figure 4. Comparison between defects identified in the literature and the Arrhenius plot obtained by analyzing the breakdown walkout process (black symbols) and the C-DLTS measurements (red symbols). Experimental data from <sup>[49][50]</sup>.

#### 4. Analysis of the trapping mechanisms and degradation on GaN-on-GaN Vertical Field Effect Transistors

Among vertical GaN devices, the Vertical Fin Field Effect Transistors (VFETs) has recently demonstrated to be an excellent candidate for next generation power converters<sup>[23][94]</sup>. The VFET epitaxial layers are grown on a 2-inch GaN substrate. The epitaxial layers consist of 8-μm-thick n-GaN channel and n<sup>-</sup>-GaN drift layer doped  $2 \times 10^{16} \text{ cm}^{-3}$  and 0.3-μm-thick n<sup>+</sup>-GaN. In order to obtain MOS gate stacks on sidewalls a combined dry-wet etching technique is used and a 15 nm Al<sub>2</sub>O<sub>3</sub> layer was deposited by ALD using H<sub>2</sub>O and TMA at 250 °C as gate dielectric. Gate metal (molybdenum) was sputtered immediately after ALD. In VFETs the current flows vertically through sub-micrometer channels formed by carrier accumulation at the Oxide/GaN interface; the cross section of one channel-device is reported in Figure 5 (a). The channel electron density simulations at different gate voltage are reported in Figure 5 (b)<sup>[73]</sup>. Below the threshold voltage ( $V_{GS} = 0 \text{ V} < 1 \text{ V}$ ) the device is in the off-state and the channel is depleted. For gate voltages higher than the threshold, the channel is fully formed, and the electron density peaks at the Al<sub>2</sub>O<sub>3</sub>/GaN interface, and in the center of the GaN layer it becomes equal to the dopant concentration. The VFET structure consists in the repetition of gate – GaN channel – gate modules in which multiple channels operate in parallel in order to obtain sufficient current.

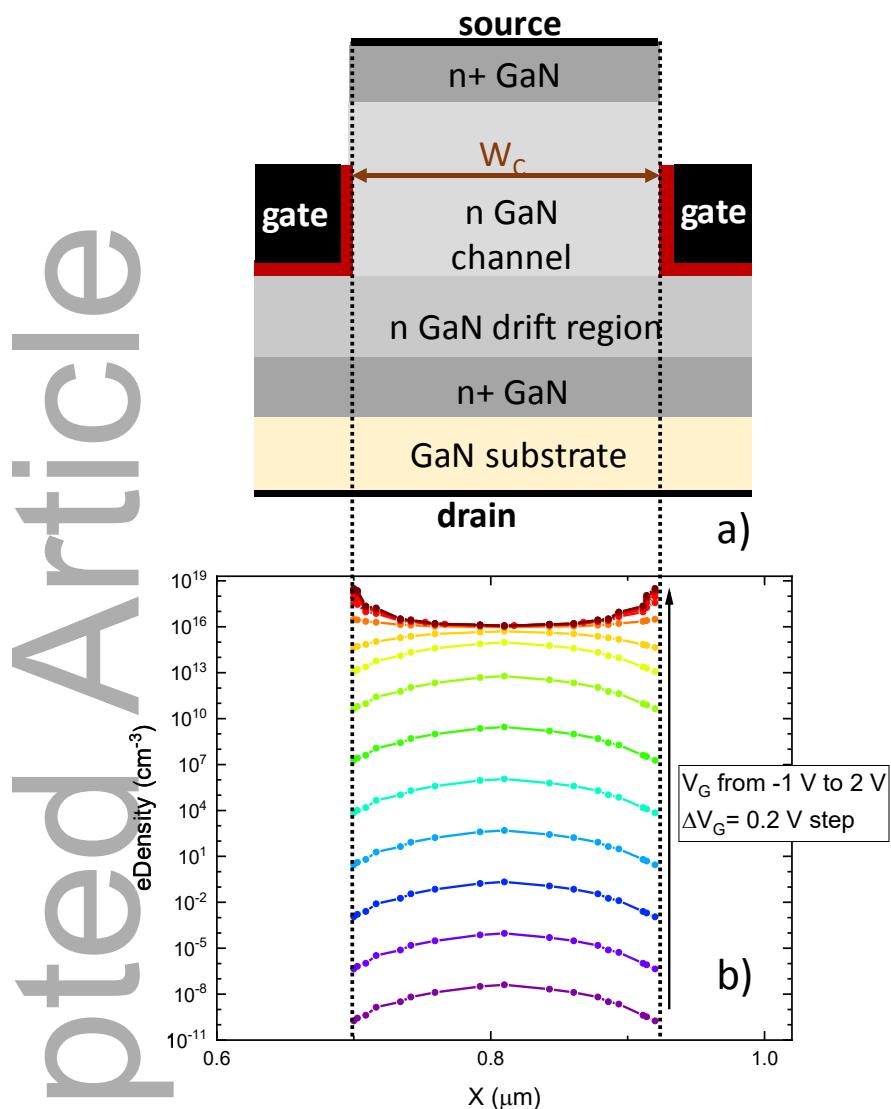


Figure 5. Simulation of electron density in a VFET for different gate voltages.

#### 4.1. Instability of Threshold Voltage in GaN-on-GaN Vertical Field Effect Transistors submitted to positive gate bias

In [73] the first analysis on the dynamic performance and on the gate stability of these devices has been reported. To study trapping effects on the dynamic parameters of the devices, double pulses have been applied to the drain and gate terminals starting from a trapping condition (positive gate voltage and zero drain bias) to a measurement condition to monitor the variation in the on-

resistance and threshold voltage. The results are reported in Figure 6. When VFETs are subjected to pulsed positive gate bias, the on-resistance slightly decreases due to a change in the interface scattering (not reported here):  $R_{on}$  is determined both by carrier concentration and carrier mobility; when the device is submitted to positive  $V_G$ , the trapped charge may change the total interface scattering, thus increasing the mobility near the interface<sup>[95]</sup>. In addition, the devices show a negative threshold voltage shift for low positive gate bias ( $0 \text{ V} < V_{GS} \leq 2 \text{ V}$ ), while for high trapping bias ( $V_{GS} \geq 3 \text{ V}$ ) a positive shift of the threshold voltage is observed. At low gate bias the negative threshold voltage shift is ascribed to the de-trapping of electrons from the  $\text{Al}_2\text{O}_3$  insulator (see mechanism 1 Figure 7 (a)); on the other hand, high gate voltages induce the injection of electrons from the accumulation region (channel) towards the dielectric, leading to a positive shift of the threshold voltage (see mechanism 2 Figure 7 (a,b)).

The stability of VFETs was investigated with by  $I_DV_D$  and fast  $I_DV_G$  measurements performed during a constant voltage stress test of 100 s at different  $V_{G\text{stress}}$ , followed by 100 s of recovery with gate, source and drain terminals at 0 V. With positive gate bias, the on-resistance decreases in time and the threshold voltage shows a fully recoverable negative shift for low gate voltages, and a positive shift (non-recoverable in thousands of seconds) for higher gate voltages ( $>3 \text{ V}$ ). The gate leakage at low and high gate bias for 100 s has been monitored in order to confirm the hypotheses: the gate leakage becomes relevant only at high gate voltages. The positive threshold voltage shift is correlated with the gate leakage (injection of electrons from the channel towards the insulator) and the mechanism has a slow recovery time.

Constant voltage stress tests were carried out at different temperatures (25 °C, 50 °C, 75 °C) in order to study the effect of the temperature on the trapping-detrapping kinetics. At low stress voltages ( $V_{GS} \leq 2 \text{ V}$ ), temperature does not significantly affect the trapping kinetics, confirming that the negative threshold shift is ascribed to an electrostatic process (emission of electrons from insulator to metal). On the other hand, at high gate bias ( $V_{GS} \geq 3 \text{ V}$ ), the total gate current increases

with temperature. In conclusion, both the gate voltage (stronger band bending), and the high temperature (increase in the average energy of electrons in the channel) favor the injection of carriers towards the insulator (see Figure 7 (b)).

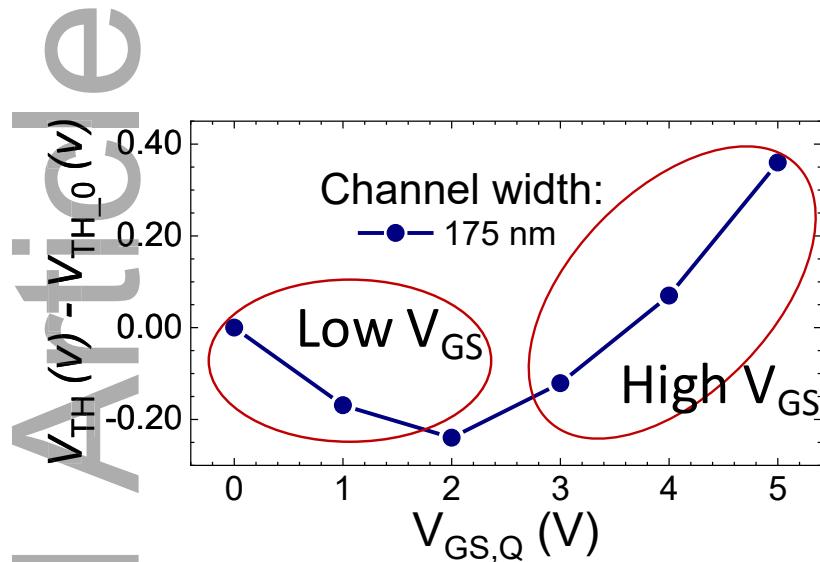


Figure 6. Variation of the threshold voltage as obtained from pulsed  $I_DV_G$  performed for different trapping conditions at  $V_{GS,Q} = 0$  V, 1 V, 2 V, 3 V, 4 V, 5 V,  $V_{DS,Q} = 0$  V. The threshold voltage has an initial negative shift for low gate voltage ( $V_{GS} < 2$  V), then a positive shift for higher gate voltages.

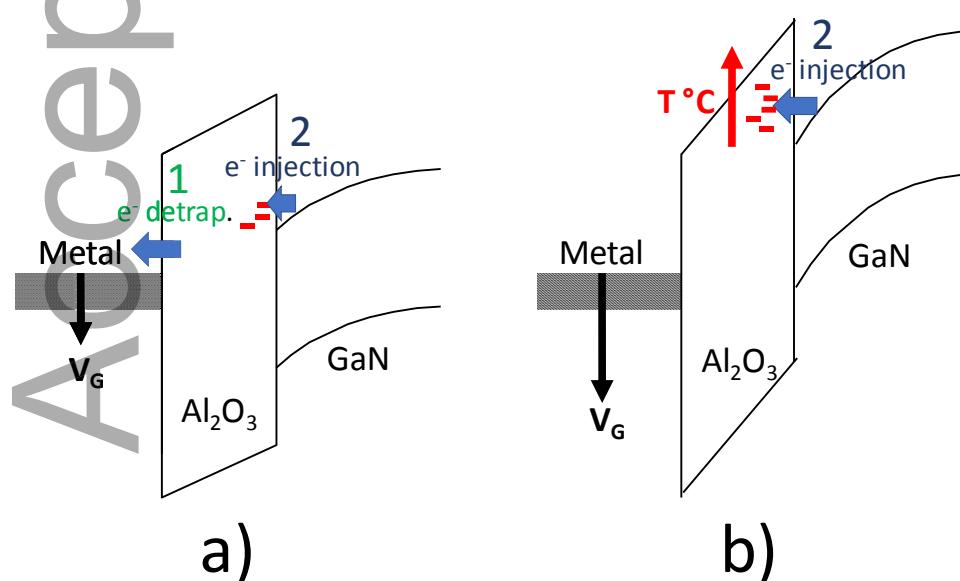


Figure 7. Pictorial representation of the trapping mechanisms under positive gate bias. a) mechanism 1: at low gate bias, electrons already trapped inside the insulator are de-trapped leading

to a negative shift of the threshold voltage; mechanism 2: electrons in the channel are injected towards the insulator; b) At high gate bias, mechanism 2 is dominant. Two factors contribute to the second mechanism: the high gate bias, i.e. the strong band bending, and the high temperature (high electron energy).

An extensive analysis of the mechanism 2 (see Figure 7) occurring at high positive gate voltage is reported in [76]. This mechanism is observable for longer stress times, and it is predominant for higher voltages (see Figure 8). Moreover, mechanism 2 is found to be recoverable only when the device is exposed to UV-light (see Figure 9). A possible explanation is that electrons trapped in a specific level in the oxide acquire the energy necessary to be de-trapped and reach the n-type GaN<sup>[76][96]</sup>, through hopping. Another possibility is that under UV-light the recovery is assisted by the holes accumulated at the Al<sub>2</sub>O<sub>3</sub>/GaN interface. The UV-exposure induces a negative shift of the threshold voltage by increasing the conductive electrons either by electron detrapping from oxide, or by generation of carriers, in good agreement to previous reports on different MOS structures<sup>[97][98]</sup>. The instability of the threshold voltage in Vertical Fin FETs is correlated with the presence of interface-states. In order to quantify the interface states, the changes in the gate-source capacitance as a function of voltage in trapping and de-trapping conditions have been evaluated. Gate-source capacitance curves have been performed as a function of the gate voltage, after biasing the device in depletion under UV-light (at -3 V) and accumulation (at 5 V). The C-V curve (Figure 10) performed after UV-exposure in OFF-state (red line) shows a negative shift of the threshold voltage and a change in the slope at the turn-on in respect of the C-V performed after accumulation (black line). The rigid shift in C-V is ascribed to charges (oxide traps) that are not influenced by the electron quasi-Fermi level, the change in slope is ascribed to interface states, and can be used to calculate the amount of interface states that changed occupancy with V<sub>G</sub> [99]. With this method a peak interface state density of  $4 \cdot 10^{13} \text{ cm}^{-3} \text{ eV}^{-1}$  at V<sub>GS</sub> = 2 V has been calculated.

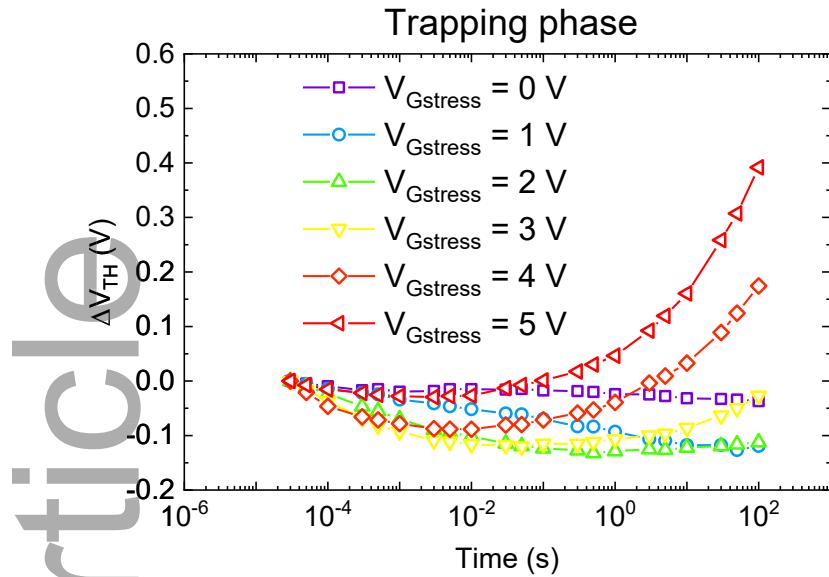


Figure 8. Threshold voltage transients during a constant bias experiment at different gate voltages and  $V_{DS} = 0$  V. For short stress times the negative shift is dominant, then the second mechanism, i.e. trapping of electrons in the oxide, occurs (earlier for higher gate bias) leading to a positive shift of the threshold voltage.

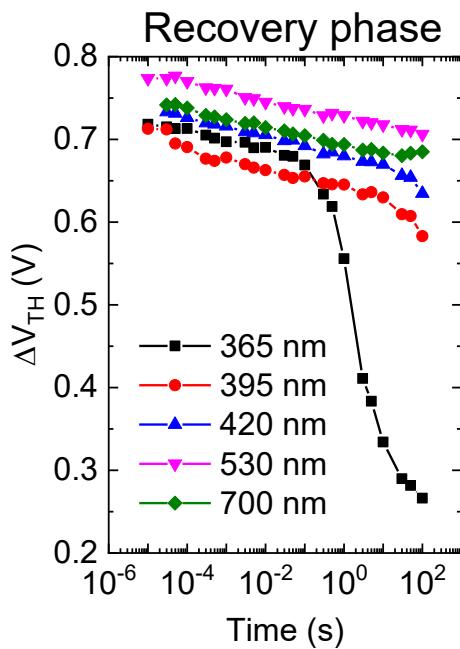


Figure 9. Threshold voltage transients performed during a recovery phase under LED light at different wavelengths, after stress at  $V_{GS}=4$  V: a strong recovery is observed only when the device is illuminated with UV light at 365 nm (corresponding to energy gap of GaN).

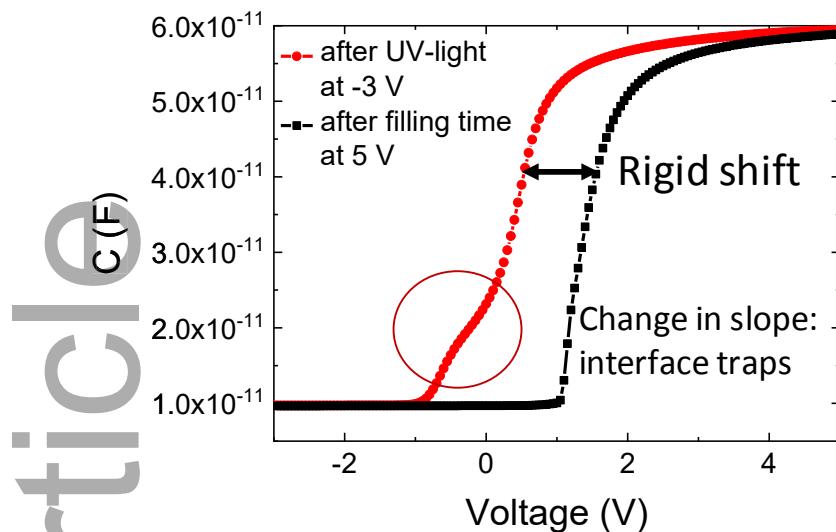


Figure 10. Gate-Source Capacitance plots measured on a VFET with a channel width of 125 nm by sweeping the gate voltage from -3 V to 5 V after illuminating the device with UV-light and from 5 V to -3 V after biasing the device at 5 V in dark condition for 1000 s.

#### 4.3 Degradation of vertical GaN-on-GaN fin transistors under positive gate or high-drain stress.

To evaluate the robustness of GaN-on-GaN fin transistors, we carried out step stress experiments; the devices were submitted to a forward gate voltage for 120 s with drain and source biased to 0 V, then the gate voltage was sequentially increased by 0.25 V/step, and the device transfer characteristics were monitored at each step. With this technique it is possible to investigate the mechanisms that lead the device to failure. The results of the step stress are reported in Figure 11: the gate current monitored during the stress increases at each step of stress, and for  $V_{GS} = 7.25$  V an abrupt increase of more than 4 decades is observed due to the dielectric breakdown. From the plot of the  $I_DV_G$  in semi-logarithmic scale (Figure 12), a positive shift of the threshold voltage is observed for low stress voltages (in good agreement with the previous work<sup>[73]</sup>). Moreover, the

positive gate bias induces a significant increase of subthreshold slope at  $I_{DS} = 10^{-3}$  A/cm<sup>2</sup>. This can be explained by considering another mechanism (mechanism 3 Figure 12): at very high gate stress voltages (up to 7.75 V), the electrons injected from the channel to the insulator may promote the generation of traps. Electron traps are depleted during stress, thus giving higher current at turn-on and an increase in subthreshold slope.

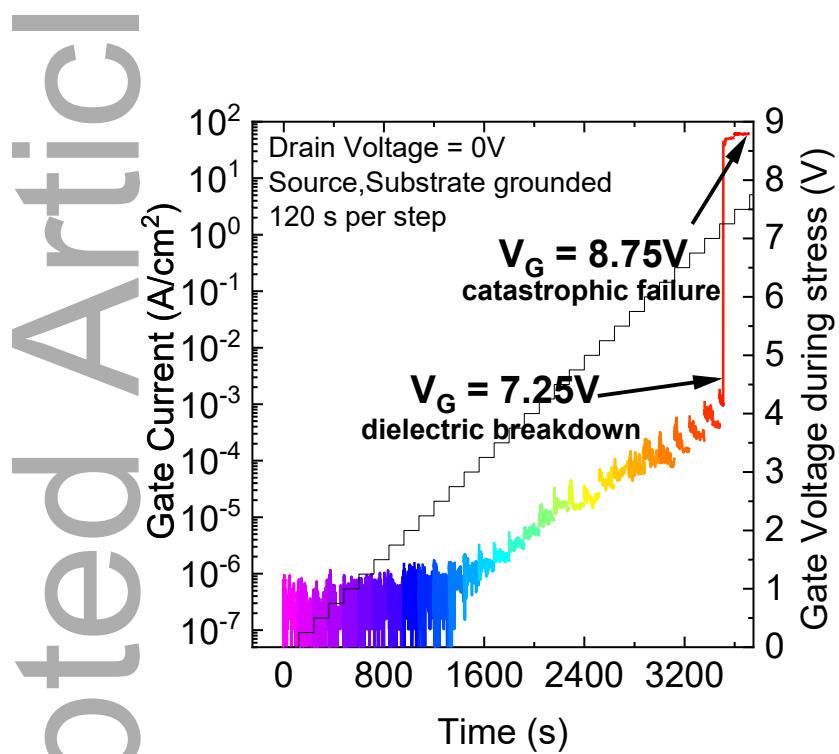


Figure. 11 Step stress performed with  $V_{D\text{stress}} = 0$  V and by increasing the  $V_{G\text{stress}}$  by 0.25 V each 120 s of stress. The breakdown of the dielectric occurs at 7.25 V

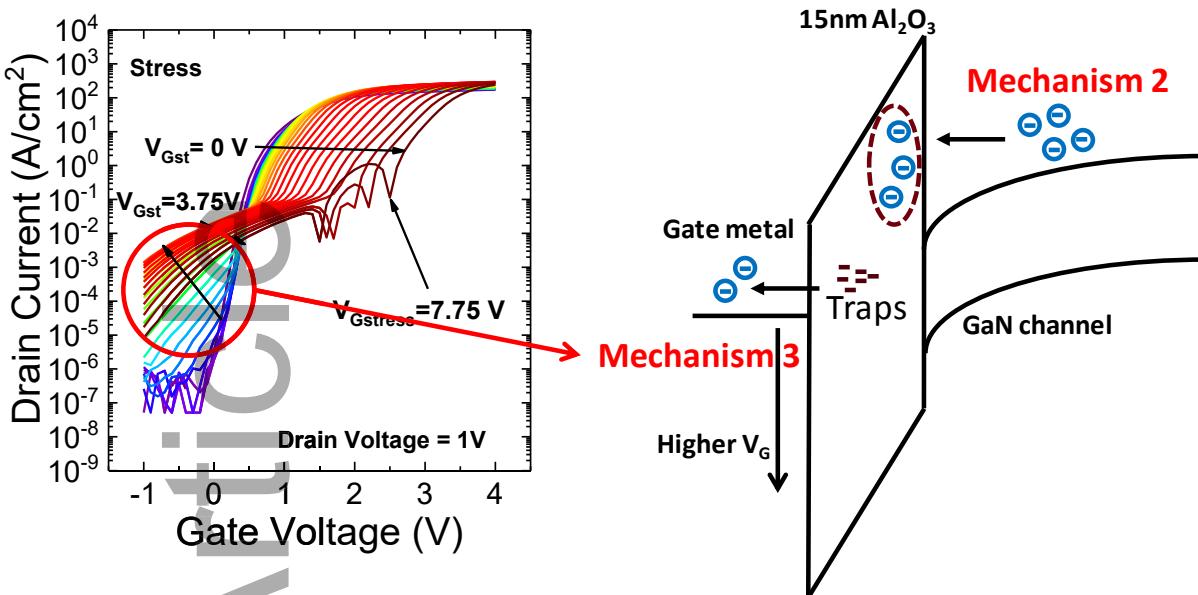


Figure. 12. Stressing at increasing gate voltages induces an increase in the subthreshold slope due to trap generation in the oxide (left): traps are depleted during stress, thus giving higher current near turn-on (right).

We also investigated the prolonged stress under positive gate bias on VFETs with different gate width<sup>[74]</sup>. In order to analyze the degradation mechanism responsible of the catastrophic failure when the VFETs are submitted to positive gate bias, step stress tests have been performed. It is demonstrated that the trend of gate current during stress depends on the gate voltage (Figure 13). For low gate voltages (up to  $V_{Gstress}=0.5$  V), the gate current slightly decreases during stress. In this range of voltages, the mechanism 1 (de-trapping of electrons) and 2 (injection of electron from the accumulation channel to the oxide) occur simultaneously and the fact that one of the two dominates (increasing or decreasing of the gate current) is device-dependent.

For higher gate voltages, mechanism 2 (see Figure 13) occurs, leading to a decrease of the gate current during each stage of the stress experiment: the newly trapped electrons have a repulsive action, preventing further electrons from being trapped in the oxide, thus inducing a decrease/stabilization in gate leakage. At  $V_{Gstress} > 5.5$  V, the creation of percolation/shunt paths leads to the consequent breakdown of the dielectric.

9 devices with 70 nm of channel width and 8 devices with 280 nm were stressed at constant voltage ( $V_{GS} = 5$  V) until failure. The degradation trend of the gate current shows an abrupt increase of the gate current due to a time-dependent defect generation/percolation through the oxide. The corresponding Weibull plots are reported in Figure 14: the failure rate decreases with time ( $\beta < 1$ ) and this is in good agreement with the hypothesis of dielectric breakdown. 2D simulations (see Figure 15) indicate that the failure point is located at the corner of the insulator, where the electric field is maximum.

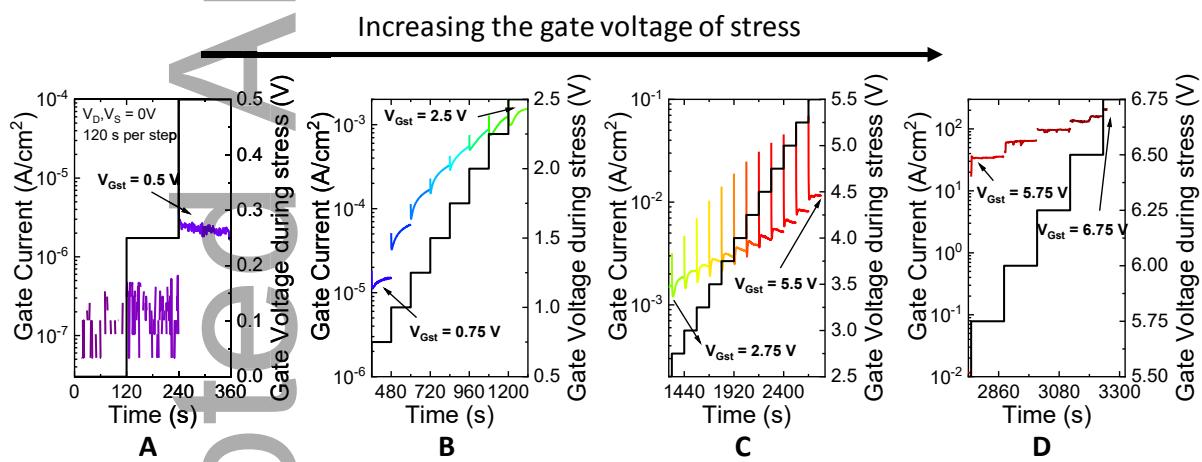


Figure. 13. Trend of the gate current for each step of the gate stress on one of the analyzed VFETs. (A) At  $V_{G\text{stress}} = 0.5$  V, the gate current slightly decreases during 120 s of stress due to slight trapping of electrons inside the insulator. (B) For  $0.75 \text{ V} < V_{G\text{stress}} < 2.5$  V a fast initial decrease followed by a slow increase of the gate current is observed (C) For  $2.75 \text{ V} < V_{G\text{stress}} < 4.5$  V the gate current starts to decrease at long stress times. (D) For  $V_{G\text{stress}} > 5.5$  V percolation/shunt paths have been created leading to the breakdown of the dielectric.

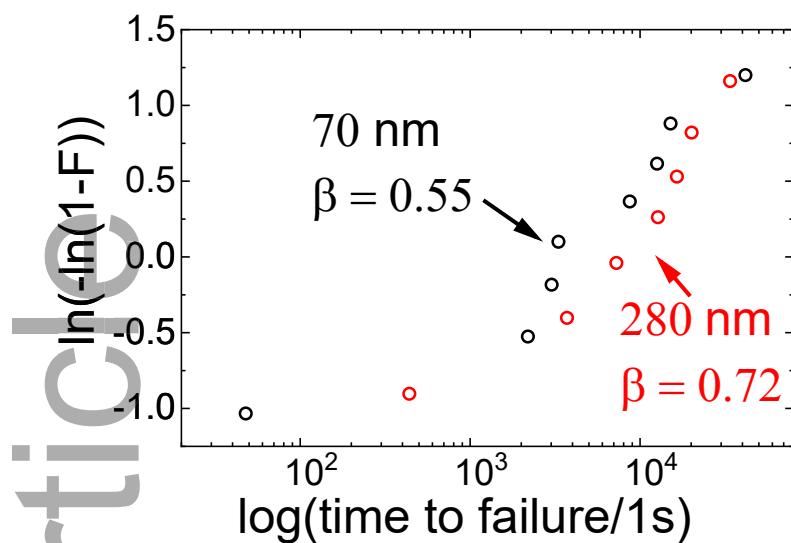


Figure. 14. Comparison of the Weibull plots at 99% of confidence level for VFETs with 70 nm channel (black curve) and 280 nm channel (red curve).

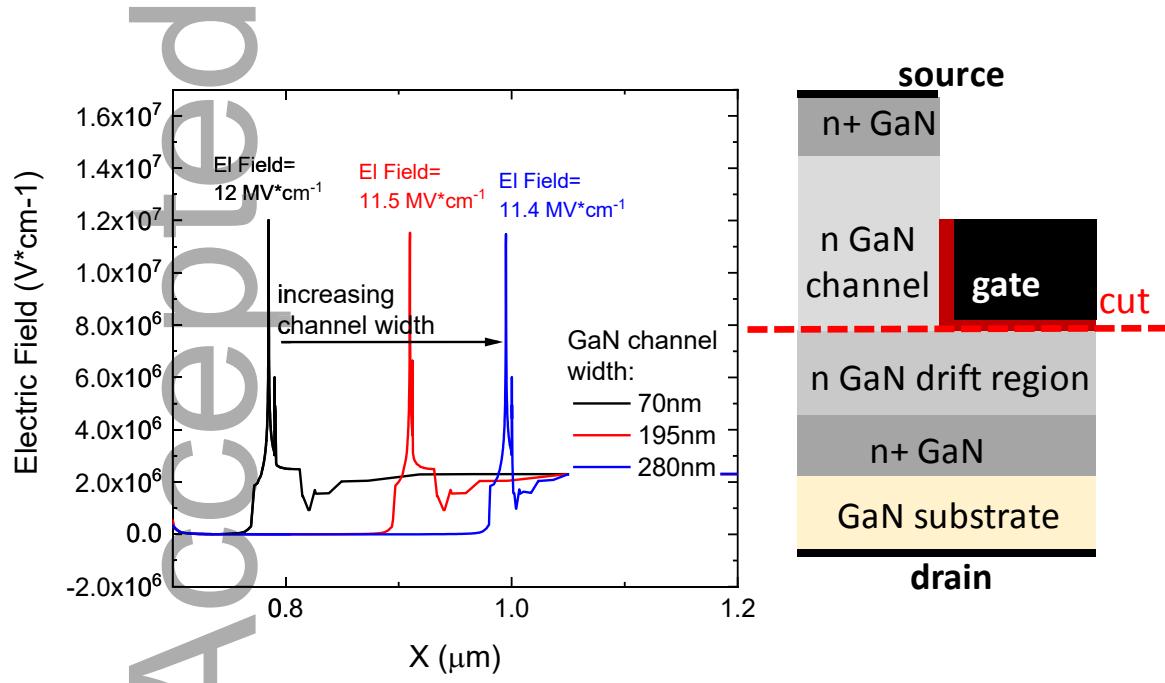


Figure. 15 Simulation of the electric field when the device is at 5 V. The peak of the electric field is located at the corner of the dielectric independently of the channel width. Devices with shorter channel width have higher peak of the electric field. Values of the field may be overestimated due to the fact that square corners were used in the simulations.

The degradation of VFETs under high drain voltage has been also investigated<sup>[75]</sup>. The device was submitted to a step stress test in which the drain voltage has been increased by 20 V every 120 s, with  $V_{GS}=0$  V. At the end of each step a DC characterization was performed. The results are shown in Figure 16: a small positive  $V_{TH}$  shift and negligible variations in on-resistance are induced by high drain bias. The VFET shows a good stability up to 280 V (the device under test is optimized for 200 V operation).

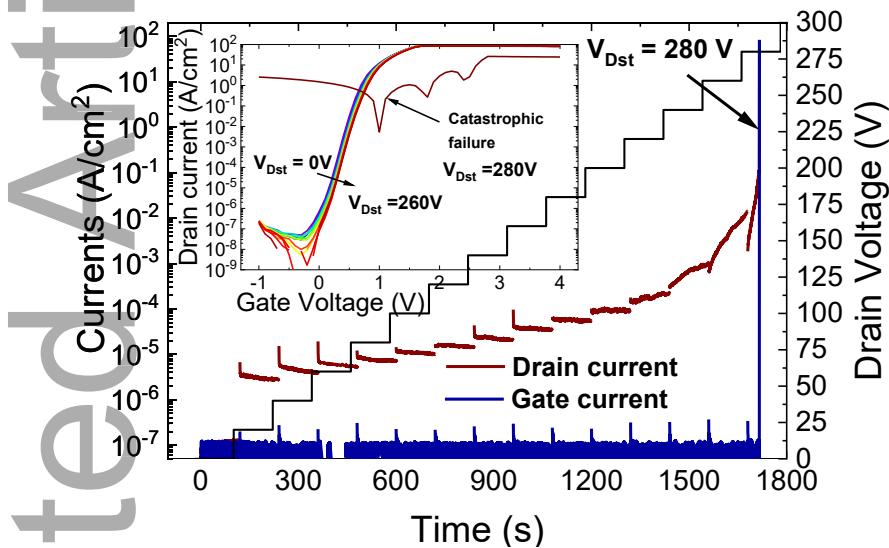


Figure. 16 Gate and drain currents measured during the step stress at high drain voltage. (inset)  $I_DV_G$  performed at each step of the drain step stress.

Ruzzarin et al.<sup>[74]</sup> reported the analysis of the degradation process that occurs when the VFETs are submitted to high drain voltage in off-state ( $V_{GS}=0$  V). The gate current has been monitored during a constant voltage stress experiments at 300 V: a catastrophic failure was reached after 2 hours of stress, and consists in a rapid increase in the gate leakage current. By means of 2D simulations of the electric field within the device submitted to high drain voltage, the peak of the electric field was found again to be located at the edge of the gate.

## 5. Conclusions

In conclusions, we have summarized recent case studies in the field of GaN vertical power devices. The results indicate the existence of a set of degradation processes, that do not constitute fundamental limits, and can be solved through a careful optimization of device structure. The study of GaN vertical devices is still at the early phase: a significant progress in this field will be possible through extensive research, and will open the way to this revolutionary technology.

Accepted Article

## Acknowledgments

This research activity was partly funded by project “Novel vertical GaN-devices for next generation power conversion”, NoveGaN (University of Padova), through the STARS CoG Grants call. T.P. and M.S. acknowledge the partial funding support of the ARPA-E Switches program. The GaN p-n diodes were developed under the ARPA-E SWITCHES project at Cornell University, which made use of the Cornell Nanoscale Science and Technology Facilities (CNF) sponsored by the NSF NNCI program (ECCS-1542081), and the Cornell Center for Materials Research Shared Facilities which are supported through the NSF MRSEC program (DMR-1719875) as well as NSF MRI-1338010

## REFERENCES

- [1] available online at <https://www.transphormusa.com/en/document/datasheet-tp90h180ps-900v-gan-fet/>.
- [2] G. Meneghesso, M. Meneghini, D. Bisi, I. Rossetto, A. Cester, U. K. Mishra, and E. Zanoni, *Semiconductor Science and Technology*, **2013**, vol. 28, no. 7.
- [3] S. Karmalkar, M. S. Shur, G. Simin, and M. A. Khan, *IEEE Transactions on Electron Devices*, **2005**, vol. 52, no. 12, pp. 2534–2540.
- [4] T. Mizoguchi, T. Naka, Y. Tanimoto, Y. Okada, W. Saito, M. Miura-Mattausch, and H. J. Mattausch, *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, **2016**, vol. 2016-July, pp. 267–270.
- [5] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka, and D. Ueda, *IEEE Transactions on Electron Devices*, **2007**, vol. 54, no. 12, pp. 3393–3399.
- [6] [https://industrial.panasonic.com/content/data/SC/ds/ds8/c2/FLY000074\\_EN.pdf](https://industrial.panasonic.com/content/data/SC/ds/ds8/c2/FLY000074_EN.pdf).
- [7] T. Oka, *Japanese Journal of Applied Physics*, **2019**, vol. 58, no. SB.
- [8] I. C. Kizilyalli, A. P. Edwards, H. Nie, D. Bour, T. Prunty, and D. Disney, *IEEE Electron Device Letters*, **2014**, vol. 35, no. 2, pp. 247–249.
- [9] I. C. Kizilyalli, A. P. Edwards, O. Aktas, T. Prunty, and D. Bour, *IEEE TRANSACTIONS ON ELECTRON DEVICES*, **2015**, vol. 62, no. 2, pp. 414–422.

[10] I. C. Kizilyalli, T. Prunty, and O. Aktas, *IEEE Electron Device Letters*, **2015**, vol. 36, no. 10, pp. 1073–1075.

[11] N. Man, Y. Yee, Y. Li, and E. Yi, *Vacuum*, **2015**, vol. 118, pp. 59–63.

[12] I. C. Kizilyalli, P. Bui-quang, D. Disney, H. Bhatia, and O. Aktas, *Microelectronics and Reliability*, **2015**, vol. 55, no. 9–10, pp. 1654–1661.

[13] M. Sun, Y. Zhang, and T. Palacios, *Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, **2016**.

[14] A. M. Armstrong, A. A. Allerman, A. J. Fischer, M. P. King, M. S. Van Heukelom, M. W. Moseley, R. J. Kaplar, J. J. Wierer, M. H. Crawford, and J. R. Dickerson, *ELECTRONICS LETTERS*, **2016**, vol. 52, no. 13, pp. 1170–1171.

[15] X. Zou, X. Zhang, S. Member, X. Lu, C. W. Tang, and K. M. Lau, *IEEE Electron Device Letters*, **2016**, vol. 37, no. 5, pp. 636–639.

[16] T. Oka, T. Ina, Y. Ueno, and J. Nishii, *Proceedings of the 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, **2016**, pp. 459–462.

[17] W. Li and S. Chowdhury, *Phys. Status Solidi A*, **2016**, vol. 2720, no. 10, pp. 2714–2720.

[18] T. J. Anderson, J. D. Greenlee, B. N. Feigelson, J. K. Hite, F. J. Kub, and K. D. Hobart, *ECS Journal of Solid State Science and Technology*, **2016**, vol. 5, no. 6, pp. 176–178.

[19] M. Ueno, S. Yoshimoto, K. Ishihara, M. Okada, K. Sumiyoshi, H. Hirano, F. Mitsuhashi, Y. Yoshizumi, T. Ishizuka, and M. Kiyama, *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, **2014**, pp. 309–312.

[20] J. R. Dickerson, A. A. Allerman, B. N. Bryant, A. J. Fischer, M. P. King, M. W. Moseley, A. M. Armstrong, R. J. Kaplar, I. C. Kizilyalli, O. Aktas, J. J. Wierer, and S. Member, *IEEE TRANSACTIONS ON ELECTRON DEVICES*, **2016**, vol. 63, no. 1, pp. 419–425.

[21] J. Du, D. Liu, Z. Bai, N. Chen, and Q. Yu, *J Comput Electron (2016)*, **2016**, pp. 1334–1339.

[22] K. M. L. Xu Zhang, Ximbo Zou, Xing Lu, Chak Wah Tang, *IEEE Trans. on Electron Devices*, **2017**, vol. 64, no. 3, pp. 809–815.

[23] M. Sun, S. Member, Y. Zhang, S. Member, and X. Gao, *IEEE Electron Device Letters*, **2017**, vol. 38, no. 4, pp. 509–512.

[24] Y. Zhang, S. Member, D. Piedra, S. Member, M. Sun, S. Member, J. Hennig, and A. Dadgar, *IEEE Electron Device Letters*, **2017**, vol. 38, no. 2, pp. 248–251.

[25] Z. Guo, C. Hitchcock, and T. sing P. Chow, *Physica Status Solidi (A) Applications and Materials Science*, **2017**, vol. 214, no. 12, pp. 1–7.

[26] H. Fu, X. Huang, H. Chen, Z. Lu, X. Zhang, and Y. Zhao, *IEEE Electron Device Letters*,

2017, vol. 38, no. 6, pp. 763–766.

- [27] C. Gupta, C. Lund, S. H. Chan, A. Agarwal, J. Liu, Y. Enatsu, S. Keller, and U. K. Mishra, *IEEE Electron Device Letters*, **2017**, vol. 38, no. 3, pp. 353–355.
- [28] D. Ji, W. Li, and S. Chowdhury, *IEEE Transactions on Electron Devices*, **2018**, vol. 65, no. 10, pp. 4271–4275.
- [29] J. Hu, Y. Zhang, M. Sun, D. Piedra, N. Chowdhury, and T. Palacios, *Materials Science in Semiconductor Processing*, **2018**, vol. 78, no. July 2017, pp. 75–84.
- [30] T. Oka, Y. Ueno, T. Ina, and K. Hasegawa, *Applied Physics Express*, **2014**, vol. 7, p. 021002.
- [31] E. B. Treidel, O. Hilt, J. Stöver, V. Hoffmann, F. Brunner, K. Ickert, S. Hochheim, F. Naumann, H. Gargouri, B. Martinez, M. Weyers, and J. Würfl, *Physica Status Solidi (A) Applications and Materials Science*, **2018**, vol. 215, no. 8.
- [32] W. Li, K. Nomoto, K. Lee, S. Islam, Z. Hu, M. Zhu, X. Gao, M. Pilla, D. Jena, and H. G. Xing, *IEEE Transactions on Electron Devices*, **2018**, vol. 65, no. 6, pp. 2558–2564.
- [33] W. Li, K. Nomoto, K. Lee, S. M. Islam, Z. Hu, M. Zhu, X. Gao, J. Xie, M. Pilla, D. Jena, and H. G. Xing, *Applied Physics Letters*, **2018**, vol. 113, no. 6, pp. 1–6.
- [34] S. Kotzea, A. Debal, M. Heuken, H. Kalisch, and A. Vescan, *IEEE Transactions on Electron Devices*, **2018**, vol. 65, no. 12, pp. 5329–5336.
- [35] R. A. Khadar, C. Liu, L. Zhang, P. Xiang, K. Cheng, and E. Matioli, *IEEE Electron Device Letters*, **2018**, vol. 39, no. 3, pp. 401–404.
- [36] O. Slobodyan, T. Smith, J. Flicker, S. Sandoval, C. Matthews, M. Van Heukelom, R. Kaplar, and S. Atcitty, *MRS Communications*, **2018**, pp. 1–5.
- [37] D. Ji, A. Agarwal, H. Li, W. Li, S. Keller, and S. Chowdhury, *IEEE Electron Device Letters*, **2018**, vol. 39, no. 6, pp. 863–865.
- [38] R. Tanaka, S. Takashima, K. Ueno, H. Matsuyama, M. Edo, and K. Nakagawa, *Proc. International Symposium on Growth of III-Nitrides ISGN-7*, **2018**, no. August, p. 2018.
- [39] H. Ohta, K. Hayashi, F. Horikiri, T. Nakamura, and T. Mishima, *Japanese J. Appl. Physics*, **2018**, vol. 57, p. 04FG09.
- [40] Y. Zhang, M. Sun, J. Perozek, Z. Liu, A. Zubair, D. Piedra, N. Chowdhury, X. Gao, K. Shepard, and T. Palacios, *IEEE Electron Device Letters*, **2019**, vol. 40, no. 1, pp. 75–78.
- [41] H. Ohta, N. Kaneda, F. Horikiri, Y. Narita, and T. Yoshida, *IEEE ELECTRON DEVICE LETTERS*, **2015**, vol. 36, no. 11, pp. 1180–1182.
- [42] W. Li, M. D. Brubaker, B. T. Spann, K. A. Bertness, and P. Fay, *IEEE Electron Device Letters*, **2018**, vol. 39, no. 2, pp. 184–187.

[43] D. Ji, A. Agarwal, W. Li, S. Keller, and S. Chowdhury, *IEEE Transactions on Electron Devices*, **2018**, vol. 65, no. 2, pp. 483–487.

[44] D. Shibata, R. Kajitani, H. Handa, N. Shiozaki, S. Ujita, M. Ogawa, K. Tanaka, S. Tamura, T. Hatsuda, M. Ishida, and T. Ueda, *Gallium Nitride Materials and Devices XIII*, **2018**, vol. 1053211, no. February 2018, p. 36.

[45] W. Li, M. Zhu, K. Nomoto, Z. Hu, X. Gao, M. Pilla, D. Jena, and H. G. Xing, *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, **2018**, vol. 2018-May, pp. 228–231.

[46] C. Liu, R. A. Khadar, and E. Matioli, *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, **2018**, vol. 2018-May, pp. 240–243.

[47] J. Wang, L. Cao, J. Xie, E. Beam, R. McCarthy, C. Youtsey, and P. Fay, *Applied Physics Letters*, **2018**, vol. 113, no. 2, pp. 1–6.

[48] H. Fukushima, S. Usami, M. Ogura, Y. Ando, A. Tanaka, M. Deki, M. Kushimoto, S. Nitta, Y. Honda, and H. Amano, *Applied Physics Express*, **2019**, vol. 12, no. 2, pp. 8–12.

[49] C. De Santi, E. Fabris, K. Nomoto, Z. Hu, W. Li, X. Gao, D. Jena, H. G. Xing, G. Meneghesso, M. Meneghini, and E. Zanoni, *Technical Digest - International Electron Devices Meeting, IEDM*, **2019**, vol. 2018-Decem, pp. 30.2.1-30.2.4.

[50] E. Fabris, C. De Santi, A. Caria, K. Nomoto, Z. Hu, W. Li, X. Gao, D. Jena, H. G. Xing, G. Meneghesso, E. Zanoni, and M. Meneghini, *IEEE Transactions on Electron Devices*, **2019**, vol. 66, no. 11, pp. 4597–4603.

[51] Y. Zhang, M. Sun, D. Piedra, J. Hu, Z. Liu, Y. Lin, X. Gao, K. Shepard, and T. Palacios, *2017 IEEE International Electron Devices Meeting (IEDM)*, **2017**, pp. 9.2.1-9.2.4.

[52] M. Xiao, X. Gao, T. Palacios, and Y. Zhang, *Applied Physics Letters*, **2019**, vol. 114, no. 16, pp. 2–7.

[53] Y. Zhang, S. Member, M. Sun, S. Member, H. Wong, Y. Lin, S. Member, P. Srivastava, C. Hatem, M. Azize, D. Piedra, S. Member, L. Yu, and S. Member, *IEEE Trans. on Electron Devices*, **2015**, vol. 62, no. 7, pp. 2155–2161.

[54] E. B. Treidel, O. Hilt, M. Wolf, L. Schellhase, A. Thies, and J. Würfl, *Materials Science in Semiconductor Processing*, **2019**, vol. 91, no. November 2018, pp. 146–150.

[55] A. Sandupatla, S. Arulkumaran, G. I. Ng, K. Ranjan, M. Deki, S. Nitta, Y. Honda, and H. Amano, *AIP Advances*, **2019**, vol. 9, no. 4.

[56] R. M. Abdul Khadar, C. Liu, R. Soleimanzadeh, and E. Matioli, *IEEE Electron Device Letters*, **2019**, vol. 40, no. 3, pp. 443–446.

[57] D. Ji and S. Chowdhury, *IEEE TRANSACTIONS ON ELECTRON DEVICES*, **2015**, vol. 62, no. 8, pp. 2571–2578.

[58] O. Aktas and I. C. Kizilyalli, *IEEE ELECTRON DEVICE LETTERS*, **2015**, vol. 36, no. 9, pp. 890–892.

[59] T. Kachi, *IEEE Electron Device Meeting IEDM 2015 Technical Digest*, **2015**, no. V, pp. 410–413.

[60] T. J. Anderson, J. D. Greenlee, B. Feigelson, J. K. Hite, K. D. Hobart, and F. J. Kub, *ECS Transactions*, **2015**, vol. 69, no. 11, pp. 99–103.

[61] Y. Saitoh, K. Sumiyoshi, M. Okada, T. Horii, T. Miyazaki, H. Shiomi, M. Ueno, K. Katayama, M. Kiyama, and T. Nakamura, *Applied Physics Express*, **2010**, vol. 3, no. 8, p. 081001.

[62] K. Nomoto, T. Nakamura, Y. Hatakeyama, H. Katayose, N. Kaneda, and T. Mishima, *Physica Status Solidi (A) Applications and Materials Science*, **2011**, vol. 208, no. 7, pp. 1535–1537.

[63] Y. Zhang, A. Dadgar, and T. Palacios, *Journal of Physics D: Applied Physics*, **2018**, vol. 51, p. 273001.

[64] Y. Zhang, M. Sun, D. Piedra, M. Azize, X. Zhang, T. Fujishima, and T. Palacios, *IEEE Electron Device Letters*, **2014**, vol. 35, no. 6, pp. 618–620.

[65] C. Liu, R. Abdul Khadar, and E. Matioli, *IEEE Electron Device Letters*, **2018**, vol. 39, no. 7, pp. 1034–1037.

[66] C. Liu, R. Abdul Khadar, and E. Matioli, *IEEE Electron Device Letters*, **2018**, vol. 39, no. 1, pp. 71–74.

[67] Y. Zhang, M. Yuan, N. Chowdhury, K. Cheng, and T. Palacios, *IEEE Electron Device Letters*, **2018**, vol. 39, no. 5, pp. 715–718.

[68] F. Yu, K. Strempel, M. F. Fatahilah, H. Zhou, F. Romer, A. Bakin, B. Witzigmann, H. W. Schumacher, H. S. Wasisto, and A. Waag, *IEEE Transactions on Electron Devices*, **2018**, vol. 65, no. 6, pp. 2439–2445.

[69] H. G. Xing, B. Song, M. Zhu, Z. Hu, M. Qi, K. Nomoto, and D. Jena, *2015 73rd Annual Device Research Conference (DRC)*, **2015**, pp. 51–52.

[70] W. Li, K. Nomoto, A. Sundar, K. Lee, M. Zhu, Z. Hu, E. Beam, J. Xie, M. Pilla, X. Gao, S. Rouvimov, D. Jena, and H. G. Xing, *Japanese Journal of Applied Physics*, **2019**, vol. 58, no. SC, p. SCCD15.

[71] X. Zou, X. Zhang, X. Lu, C. W. Tang, and K. M. Lau, *IEEE Electron Device Letters*, **2016**,

vol. 37, no. 9, pp. 1158–1161.

- [72] E. Fabris, M. Meneghini, C. De Santi, Z. Hu, W. Li, K. Nomoto, X. Gao, D. Jena, H. G. Xing, G. Meneghesso, and E. Zanoni, *Microelectronics Reliability*, **2018**, vol. 90, no. June, pp. 568–571.
- [73] M. Ruzzarin, M. Meneghini, D. Bisi, M. Sun, T. Palacios, G. Meneghesso, and E. Zanoni, *IEEE Transactions on Electron Devices*, **2017**, vol. 64, no. 8.
- [74] M. Ruzzarin, M. Meneghini, C. De Santi, M. Sun, T. Palacios, G. Meneghesso, and E. Zanoni, *Microelectronics Reliability*, **2018**, vol. 88–90, no. June, pp. 620–626.
- [75] M. Ruzzarin, M. Meneghini, C. De Santi, G. Meneghesso, E. Zanoni, M. Sun, and T. Palacios, *IEEE International Reliability Physics Symposium Proceedings*, **2018**, vol. 2018-March, pp. 4B.11-4B.15.
- [76] M. Ruzzarin, C. De Santi, F. Chiocchetta, M. Sun, T. Palacios, E. Zanoni, G. Meneghesso, and M. Meneghini, *Microelectronics Reliability*, **2019**, p. 113488.
- [77] K. Nomoto, B. Song, Z. Hu, M. Zhu, M. Qi, N. Kaneda, T. Mishima, T. Nakamura, D. Jena, and H. G. Xing, *IEEE Electron Device Letters*, **2016**, vol. 37, no. 2, pp. 161–164.
- [78] Z. Hu, K. Nomoto, B. Song, M. Zhu, M. Qi, M. Pan, X. Gao, V. Protasenko, D. Jena, and H. G. Xing, *Applied Physics Letters*, **2015**, vol. 107, no. 24.
- [79] K. Nomoto, Z. Hu, B. Song, M. Zhu, M. Qi, R. Yan, V. Protasenko, E. Imhoff, J. Kuo, N. Kaneda, T. Mishima, T. Nakamura, D. Jena, and H. G. Xing, *Technical Digest - International Electron Devices Meeting, IEDM*, **2015**, vol. 2016-Febru, pp. 9.7.1-9.7.4.
- [80] M. Meneghini, L. R. Trevisanello, G. Meneghesso, and E. Zanoni, *IEEE Transactions on Device and Materials Reliability*, **2008**, vol. 8, no. 2, pp. 323–331.
- [81] A. Castiglia, J. F. Carlin, and N. Grandjean, *Applied Physics Letters*, **2011**, vol. 98, no. 21, pp. 1–4.
- [82] K. Orita, M. Meneghini, H. Ohno, N. Trivellin, N. Ikeda, S. Takigawa, M. Yuri, T. Tanaka, E. Zanoni, and G. Meneghesso, *IEEE Journal of Quantum Electronics*, **2012**, vol. 48, no. 9, pp. 1169–1176.
- [83] S. Tomiya, T. Hino, S. Goto, M. Takeya, and M. Ikeda, *IEEE Journal on Selected Topics in Quantum Electronics*, **2004**, vol. 10, no. 6, pp. 1277–1286.
- [84] C. E. Dreyer, A. Alkauskas, J. L. Lyons, J. S. Speck, and C. G. Van De Walle, *Applied Physics Letters*, **2016**, vol. 108, no. 14.
- [85] M. Qi, K. Namoto, M. Zhu, Z. Hu, Y. Zhao, B. Song, G. Li, P. Fay, H. Xing, and D. Jena, *Device Research Conference - Conference Digest, DRC*, **2015**, vol. 2015-Augus, pp. 31–32.

[86] W. L. An Guo, R. S. Huang, L. Z. Zheng, and Y. C. Song, *IEEE Transactions on Electron Devices*, **1987**, vol. 34, no. 8, pp. 1788–1794.

[87] P. C. Chao, M. Shur, M. Y. Kao, and B. R. Lee, *IEEE Transactions on Electron Devices*, **1992**, vol. 39, no. 3, pp. 738–740.

[88] W. Bin Tang and Y. M. Hsin, *IEEE Transactions on Device and Materials Reliability*, **2006**, vol. 6, no. 1, pp. 42–44.

[89] J. Osaka, Y. Ohno, S. Kishimoto, K. Maezawa, and T. Mizutani, *Applied Physics Letters*, **2005**, vol. 87, no. 22, pp. 1–3.

[90] M. Meneghini, C. De Santi, T. Ueda, T. Tanaka, D. Ueda, E. Zanoni, and G. Meneghesso, *IEEE Electron Device Letters*, **2012**, vol. 33, no. 3, pp. 375–377.

[91] M. Caesar, M. Dammann, V. Polyakov, P. Waltereit, W. Bronner, M. Baeumler, R. Quay, M. Mikulla, and O. Ambacher, *IEEE International Reliability Physics Symposium Proceedings*, **2012**, p. CD 6.1-CD 6.5.

[92] K. Tanaka, M. Ishida, T. Ueda, and T. Tanaka, **2013**, vol. 52, pp. 1–5.

[93] D. V. Lang, *Journal of Applied Physics*, **1974**, vol. 45, no. 7, pp. 3023–3032.

[94] M. Sun, M. Pan, X. Gao, and T. Palacios, *Device Research Conference - Conference Digest*, *DRC*, **2016**, vol. 2016-Augus, no. 1100, pp. 3–4.

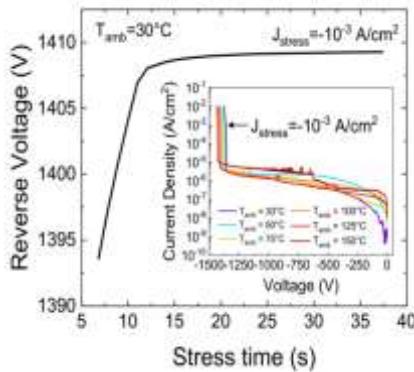
[95] A. Pérez-Tomás, M. Placidi, X. Perpiñà, A. Constant, P. Godignon, X. Jordà, P. Brosselard, and J. Millán, *Journal of Applied Physics*, **2009**, vol. 105, no. 11.

[96] D. M. Fleetwood, P. S. Winokur, R. A. Reber, T. L. Meisenheimer, J. R. Schwank, M. R. Shaneyfelt, and L. C. Riewe, *Journal of Applied Physics*, **1993**, vol. 73, no. 10, pp. 5058–5074.

[97] J.-M. Kim, S. J. Lim, T. Nam, D. Kim, and H. Kim, *Journal of The Electrochemical Society*, **2011**, vol. 158, no. 5, p. J150.

[98] B. L. Swenson and U. K. Mishra, *Journal of Applied Physics*, **2009**, vol. 106, no. 6, pp. 1–6.

[99] R. Yeluri, X. Liu, B. L. Swenson, J. Lu, S. Keller, and U. K. Mishra, *Journal of Applied Physics*, **2013**, vol. 114, no. 8.



This paper reviews recent results on the reliability of vertical GaN-based devices, by presenting a number of case studies focused on the stability and degradation of high-voltage GaN-on-GaN diodes and of GaN-based vertical FETs. These results are of high interest for the optimization of high-reliability vertical GaN devices.



Matteo Meneghini received his Laurea in Electronic Engineering (summa cum laude) and the PhD in Electronic and Telecommunication Engineering (University of Padova), working on the optimization of GaN-based LED and laser structures. He is now associate professor at the Department of Information Engineering at the University of Padova. His main interest is the characterization, reliability and simulation of compound semiconductor devices (LEDs, Laser diodes, HEMTs) and solar cells. Within these activities, he has published more than 300 journal and conference proceedings papers.